REDUCING THE COMPUTATION COMPLEXITY IN SIGNAL PROCESSING APPLICATIONS BY COMMON SUB-EXPRESSION SHARING METHOD (CSS)

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Abstract:

In order to record and recover audio signals, audio signal processing is required. In the Digital Signal Processing (DSP) of audio data, digital filters are widely employed as key components. Computational requirements, memory, and finite word length are all major elements that influence the design of a good digital filter. To achieve these objectives, the digital filter's order must be maintained as minimal as feasible by using the proper filter design process. For all low pass to band stop filters, the FDA tool is used to configure the filter design. Filtering noise from an audio signal is done with a minimal order Finite Impulse Response(FIR) digital filter. The XilinxISE14.5 is used to make it.

Keywords: FIR digital filter. DSP, CSD, FDA tool.

Introduction:-

In many domains of electronics engineering, digital signal processing is used. In today's world, audio signal processing must be extremely quick while consuming minimal power. In audio signal processing, we need to eliminate noise from the signals. As a result, a Digital Filter will be created to effectively remove noise. Calculating acceptable filter coefficients and choosing the order of the Digital Filter is the process of designing a Digital Filter.

A Field Programmable Gate Array (FPGA) can be used to implement the desired filter (FPGA). Fixed and floating point formats are used to express digital filter coefficients. Fixed point implementations are thought to be faster and less expensive in general. Floating point implementations offer a wider dynamic range and do not require scaling, making them appealing for more complex algorithms [1][2][3]. Pipelining, parallel processing, Distributed Arithmetic, folding and other digital filter architectural optimization techniques are used to create efficient digital filter architecture.

A Finite Impulse Response (FIR) filter is designed in this study. This work makes use of the MATLAB-based Filter Design and Analysis (FDA) Tool.

Digital filter:-

The transfer function of a *N*-point FIR filter is given by

$$H(z) = \sum_{n=0}^{N-1} h(n) z^{-n}$$

In most cases, the FIR filter is implemented in a non-recursive manner. Realization and approximation are the two main components of FIR filter design.

The following relationship is used to calculate the unit sample response $h_d(n)$.

$$h_d(n)=\frac{1}{2\pi}\int_{-\pi}^{\pi} H_d(w)\,e^{jwn}dw$$

$$H_d(w)=\sum_{n=-\infty}^{\infty} h_d(n)\,e^{-jwn}$$

$h_d(n)$ is truncated to length M-1 by multiplying it by the rectangular window specified as

$$w(n) = \begin{array}{ll} 1 & 0\le n\le M\text{-}1 \\ 0 & \text{otherwise} \end{array}$$

As a result, the FIR filter's unit sample response becomes

$$\begin{array}{rll} h(n) = & h_d(n)\ w(n) & \\ = & h_d(n) & 0\le n\le M\text{-}1 \\ = & 0 & \text{otherwise} \end{array}$$

The convolution of $H_d(w)$ with W(w) gives the frequency response of the truncated FIR filter H(w) and the frequency response is calculated as follows:

$$H(w)=\frac{1}{2\pi}\int_{-\pi}^{\pi} H_d(v)W(w-v)dw$$

$$H(w)=\sum_{n=0}^{M-1} h(n)e^{-jwn}$$

To implement a FIR filter with variable precision coefficient, the algorithm provided in this work can be utilized to compute the number of bits required for each coefficient. Furthermore, the non-uniform distribution of the CSD coefficient set is compensated by CSD representation [4]. Signed2's complement number system can be used to express Digital Filter coefficients. Filter coefficient can be represented using the CSD format. It reduces the number of 1's in the filter coefficient, lowering calculation complexity.

The Look Up Table (LUT), which contains the pre-computed data and can be read out conveniently, is the most important aspect of DA-based computation. FPGA implementation is highly suited to DA-based computation. Pipe lined topologies are designed for high-speed FIR filter implementation. When compared to Q16.14 representation, filters implemented with Q8.7 representation result in roughly 53 percent fewer slice LUTs [5]. [6] describes the design and implementation of a serial and parallel distributed FIR filter algorithm. The implementation's results are examined in terms of area and speed. The parallel DA design is three times faster than the standard FIR filter for high order filters.

FIR Filter design fundamentals:

Because of its stability, FIR filters are utilized. In general, the convolution sum of a FIR filter is given by

$$y(n) = \sum_{K=0}^{M-1} b_k\, x(n-k) \quad \text{.....1}$$

The FIR filter coefficient is represented by bk. Figure 1 depicts the implementation of equation (1) for a M-tap FIR filter. Multiplier, adder, and delay blocks are used. The window technique is the most basic method for creating FIR filters. Choosing the proper window is an important part of window usage. Some windows, such as rectangular, have a fast frequency domain roll off yet lack attention in the stop band and have poor group delay characteristics. Other windows, such as Blackman, have a wider transition band but superior stopband attenuation and group delay. Any Digital Filter's planned frequency response is periodic in frequency and can be described using equation.

$$H_d e^{(jw)} \sum_{n=-\infty}^{\infty} h_d(n)\, e^{-j\omega n}$$

$$h_d(n) = \frac{1}{2\pi}\int_0^{2\pi} H(e^{j\omega}) e^{-j\omega n} dw$$

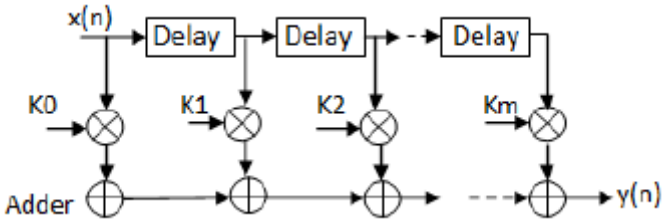

Figure 1 Realization of M-Taped FIR Filter

Proposed Method:

The filter is configured for FPGA devices in the proposed technique, and the filter configuration can be changed from low pass to bandpass and from low pass to band stop by changing the FDA in the system generator.

The method of encoding a binary integer in such a way that it has the fewest amount of non-zero bits is known as Canonic Signed Digit (CSD). A number is mapped to a ternary system (-1, 0, 1) rather than a binary system (0, 1). In a CSD number, no two consecutive bits are nonzero. A number's CSD representation has the smallest number of non-zero bits feasible.

The average number of non-zero bits among n-bit CSD numbers in the range [-1, 1] is N/3 + 1/9 + O. (2-N). As a result, CSD numbers have around 33% fewer non-zero bits on average than 2's complement number representation. A = a'W-1. a'W-2... a'1 a'0 = 2's complement number and its CSD representation is aW-1.aW-2... a1 a0 = 2's complement number and its CSD representation is aW-1.aW-2... a1 a0 = 2's complement number and its CSD representation is aW-1.aW-2... a1 a0 = 2's complement number and its CSD Before implementing the filter, look for the common sub-expression in coefficient terms and share them to reduce the number of computations and complexity. This removes the need for additional computing complexity. This is referred to as Common Sub-expression Sharing (CSS).

Simulation Results:-

Figure 2 depicts the FCSD architecture. For the target device, Xilinx ISE 9.1 is used to synthesize Distributed Arithmetic and FCSD designs.

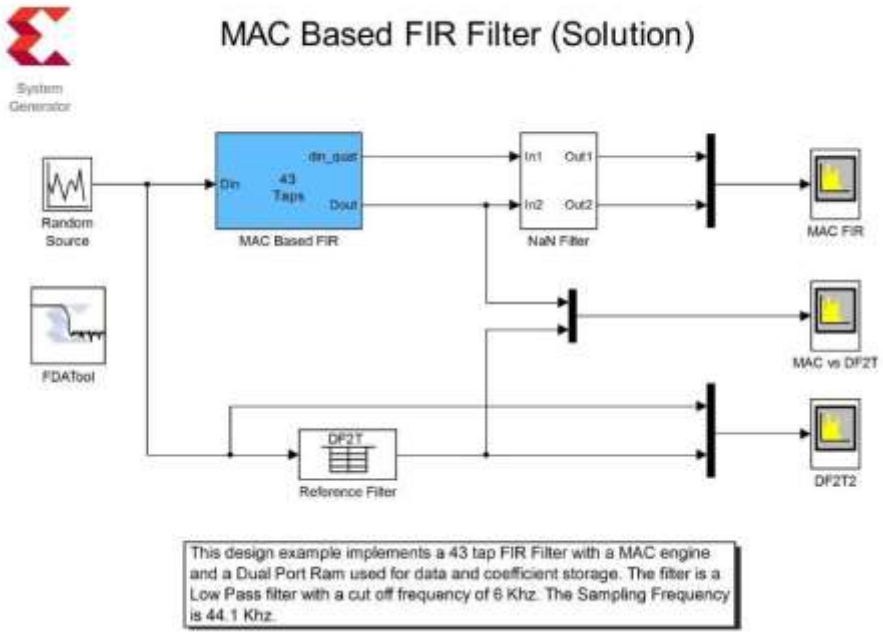

Figure 2 Showing MAC based FIR filter

The filter is set up with a low pass signal filter, which attenuates signals with frequencies higher than the reference frequency. Figures 3 and 4 illustrate this.

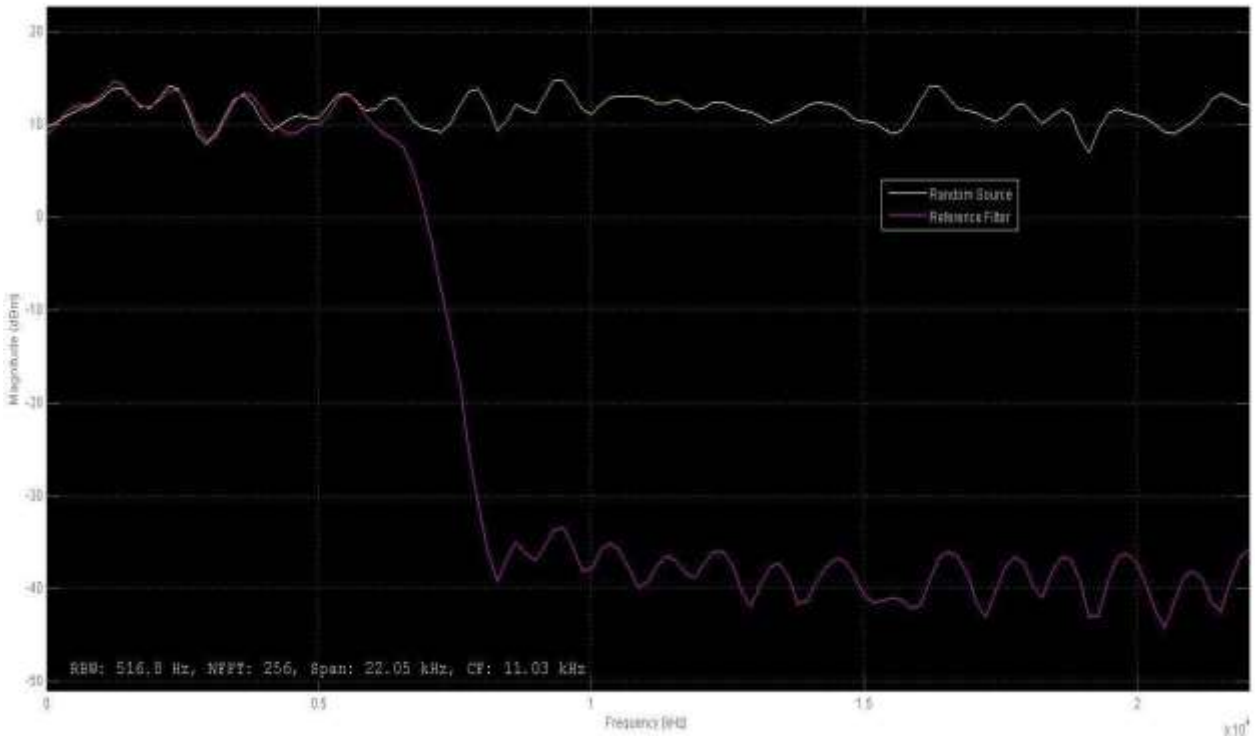

Figure 3 Normal Filter characteristics with reference signal

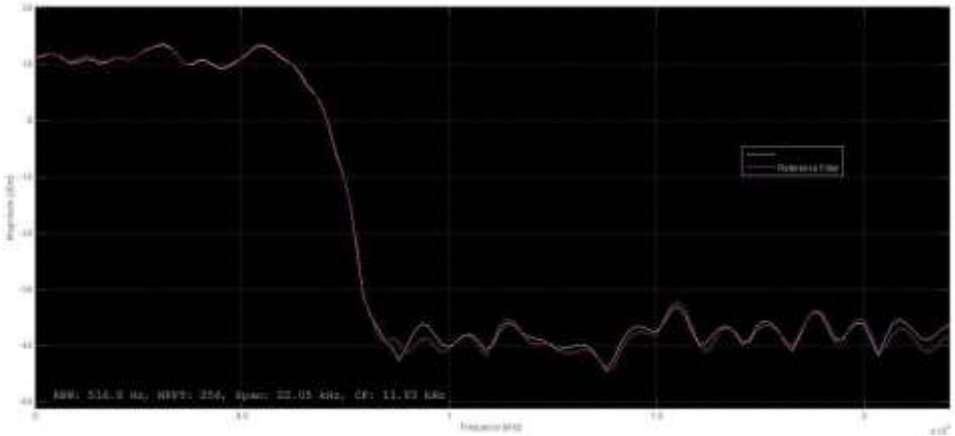

Figure 4 Proposed Filter Characteristics

Conclusion:-

This updated method produces a minimum order equi-ripple FIR filter that is equivalent to other standard optimum and windowing design methods. The FCSD architecture cuts down on power consumption. The calculation complexity is considerably reduced as a result of this. The filter can be tuned for desired characteristics for low pass to band stop filter designs, making it suitable for a wide range of communications applications.

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