Seven Level Cascaded H Bridge Inverter In closed Loop Using PWM Inverter

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Abstract : Now days Multilevel inverters are widely used for high-voltage applications due to lesser harmonic distortion, lower electromagnetic interference and larger DC link voltages. Due to this their performance is profoundly better than regular two-level inverters. Nonetheless certain drawbacks as adding in number of components and voltage balancing problems are faced. To overcome these factors, a seven-level hybrid inverter has been proposed. This topology requires lesser power controls which helps in the drop or lessening of its adroit nature, also using PWM generator hence amount to the price and mass of the inverter. The new topology can produce near sinusoidal potentials and better fundamental frequency switching. The simulation and the experimental results of a modified cascaded seven level H bridge inverter one with and one with no LC filter are presented for validation.

IndexTerms **- Cascaded H-bridge inverter (CHBI), seven level hybrid inverter, asymmetrical DC sources, Total harmonic distortion (THD), Pulse Width modulation (PWM), Multi-level Inverter (MLI), Real time Interface (RTI)**

I. INTRODUCTION

When a two-level conventional inverter had been introduced, the output of this conventional inverter is quasi square wave which consisted of lower order as well as higher order harmonics, these harmonics can be eliminated by using the passive filters. But due to the high cost and large size of inductors and capacitors of passive filters it is not advisable to eliminate the lower order harmonics. From the MATLAB representation of a single phase two level square wave inverter, THD of an output voltage is 48.21% [8], [9]. It is not advisable to run the equipment at the presence of higher harmonics as it can reduce the performance and may also decrease the lifespan of the equipment. Minimization of harmonics are performed by various methods, the most notable being PWM and Multilevel inverters. In the PWM method extensive switching takes place as compared to the multi-level inverter.

Presently multilevel inverters drew more attention due to their increased power quality, lower size of harmonics, better stair case wave form quality, reduced dv/dt variations, lower losses due to switching and increased electromagnetic interference[1],[2], they became more reliable and definitive in both research and industry towards the high and medium range voltage operations**.** The popular applications of the multi-level inverters are motor drives, power conditioning devices, electric vehicles, modular Alternate Current transmission systems [7], renewable energy harvesting and distribution.

Basically there are three types of MLI's in the reports.

First one is diode clamped MLI, second one is flying capacitor MLI, third one is cascaded H Bridge MLI. [3]-[5]. The classification in cascade multilevel inverter (CMLI) into two groups namely: 1) Symmetric CMLI - comprising of identical extents of DC potential sources; 2) Asymmetric CMLI - having dissimilar extent of the Direct Current potential sources. Among the above-mentioned types, cascade H-Bridge MLI are given importance primarily because of the factors like reduced complexity and simplicity of operation. Different procedures of modulations may be applied to CHBI, which provides the flexibility of comprising various voltage levels at the output by the adding the required number of H bridges. Although this setup requires multiple switching devices because of the increase in the number of voltage levels at the output hence making the design of MLI more complicated. By using all the uniform and asymmetric structures in CHBI, the foremost advantage is to minimize the usage of capacitors, which is the main factors in deciding the cost of the inverter. On this contrary a number of previously mentioned topologies use the bidirectional devices which pose quite a drawback. But the usage of extra bidirectional power devices (IGBTs) that burdens the inverter in terms of modularity and price poses the main drawback for the asymmetric topology or setup.

II. METHODOLOGY

The MLI setup CHBI addressed in [4] needs eight devices along with two asymmetrical dc sources, to attain seven levels to draw the interference to a THD of 21.69%which is show in the Fig.4. But the same is improvised to propound a customized cascaded H-Bridge inverter through a reduced switch sufficient to get the same output and THD. The lesser amount of switches reduces the losses and improves efficiency and reliability of the equipment to their corresponding power handling system. The essential thought of the switching topology is to isolate the DC sources from the load by using the power electronics switches. Here two DC sources are connected such that lower voltage terminal of source V1 is linked to the higher voltage terminal of other DC source V2. This state is achieved by linking the 2 DC sources in series with IGBT thus making the value chosen is such that V2=2V1.

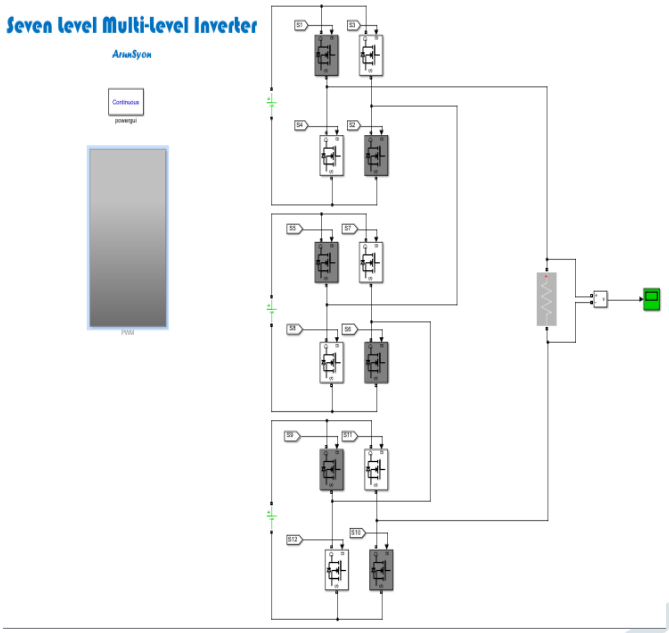

Figure 1 open loop seven level MLI

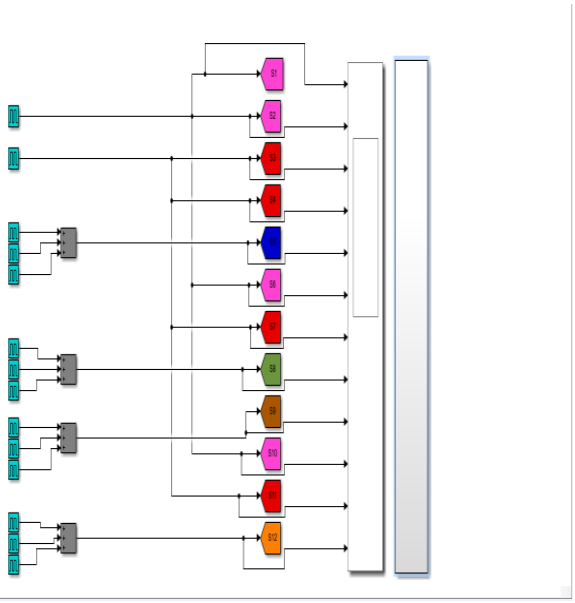

Figure 2 PWM subsystem

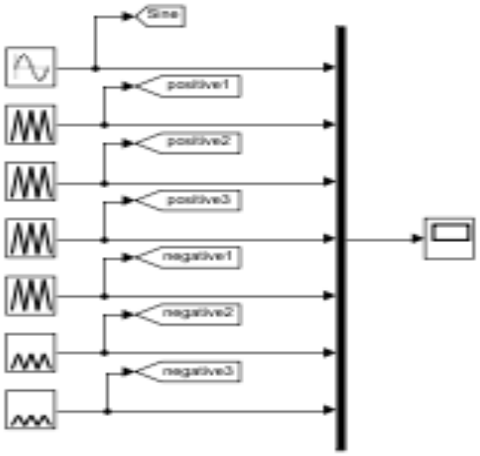

Figure 3 PWM subsystem layout 1

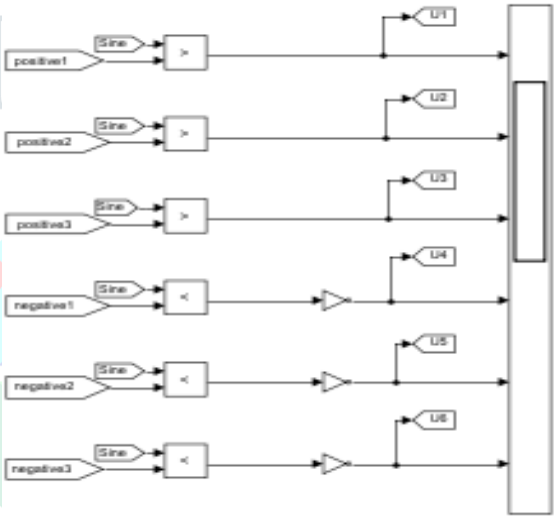

Figure 4 PWM subsystem layout 2

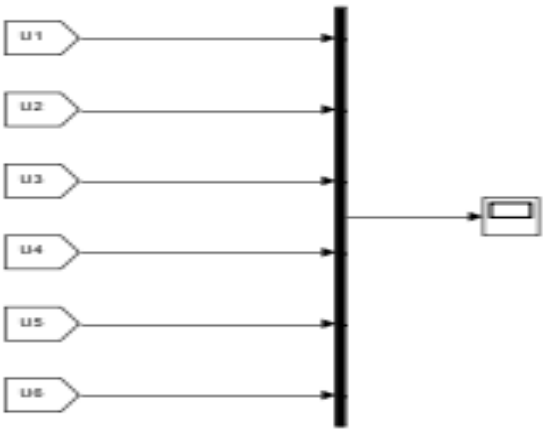

Figure 5 PWM subsystem layout 3

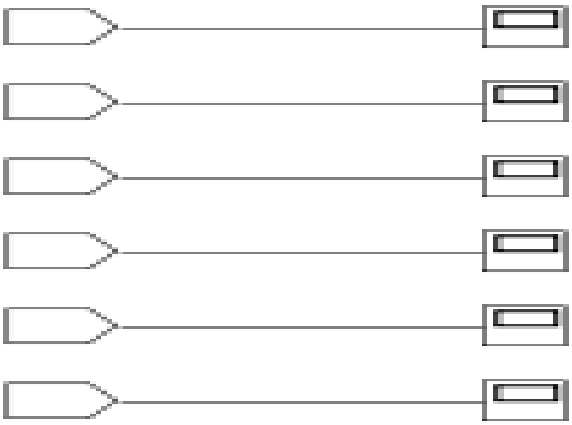

Figure 6 PWM subsystem layout 4

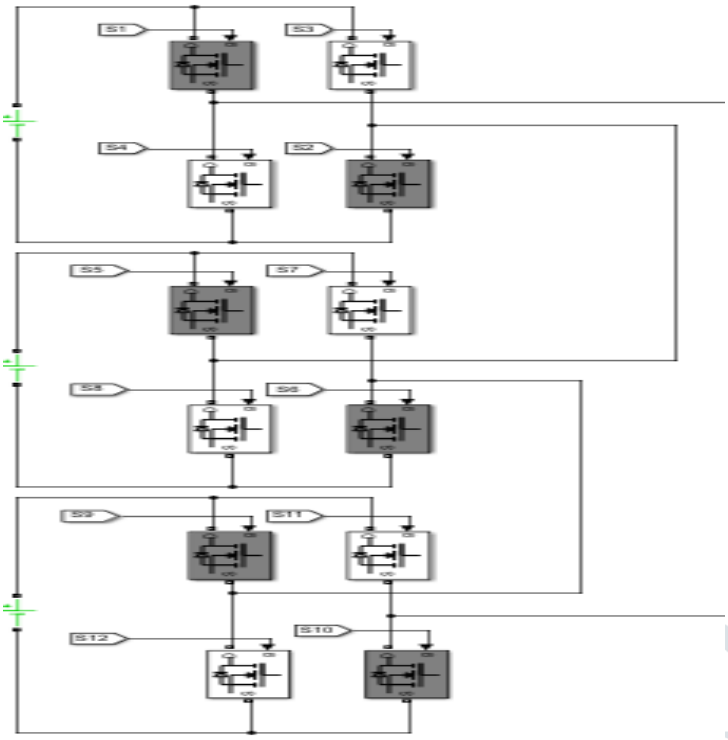

Figure 7 Seven level open loop switches layout

As shown with the help of above simulated phases of the circuit layout, the state switches and its specified potentials are shown as exhibited. The working and procedure of this table can be interpreted with the help of their switching stages as shown in the Fig.3 above table-1. The linked Switches (Sx, Sx') where {x=1, 2, 3} are complimentary activated to each paired switches respectively. There are eight functional conditions designed for the switching setup of switches s1, s2, s3 and are illustrated in Fig.3. State one and state 5 are the zero conditions or states and 6 non-zero conditions or states. Its seen that 3 of the switches conduct concurrently to acquire a particular stage of potential. For producing and incorporating the potential VO(t)=3VDC, switches S1, S2' and S3 are activated and the remaining switches are commutated. The Switch S2' conducts through every stage for the positive half cycle, likewise switch S2 conducts through all the stages for negative half cycle. S2 and S2' takes up the biggest potentials of 3VDC respectively.

III. SIMULATION RESULTS

The viewed 7 level H-BI simulation is processed in MATLAB software as represented in fig.5. The graphical representation of FFTransform of the resultant potential without filter and with filter is displayed in fig.6 and fig.7 respectively. As shown in the output it is declared that, upon using a filter Total Harmonic Distortions is upgraded unlike its counterpart with no filter.

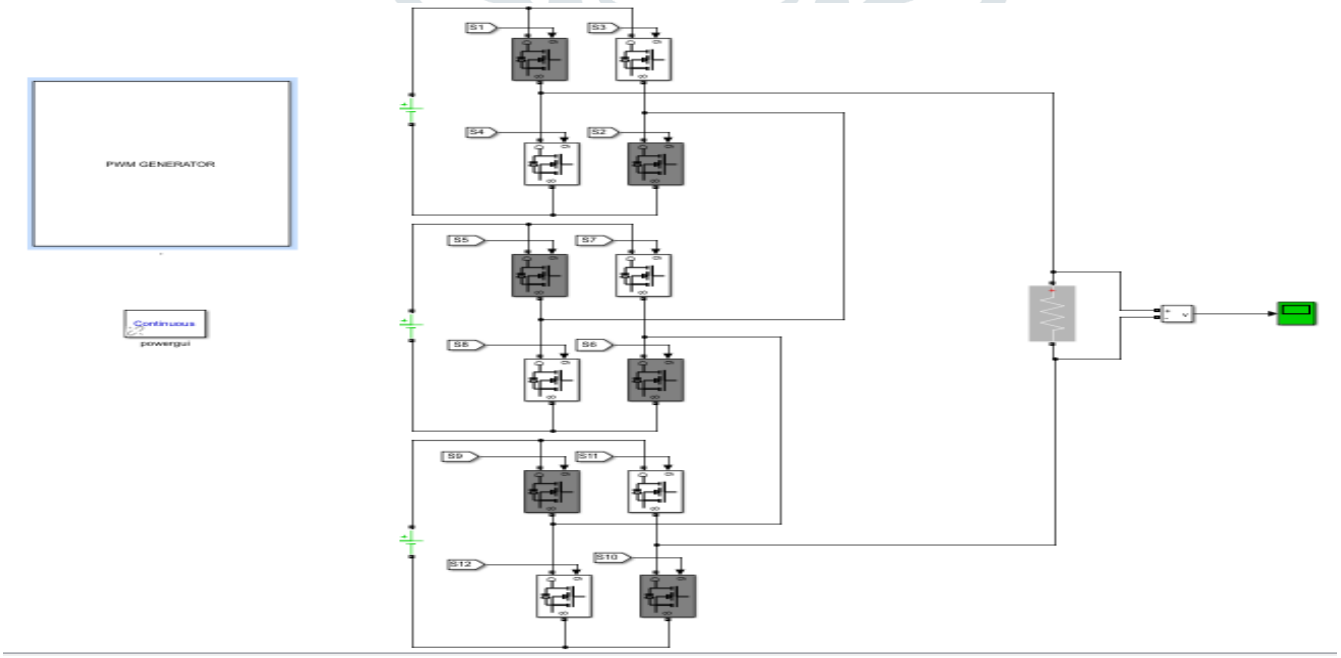

Figure 8 Closed loop H bridge layout

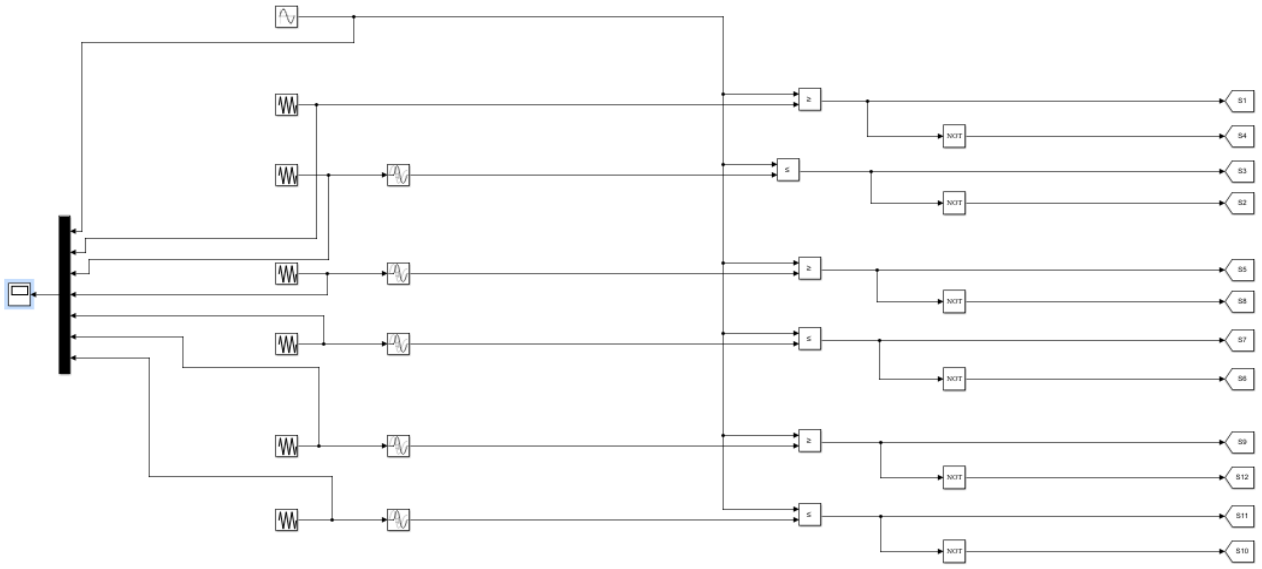

Figure 9 Closed loop PWM layout

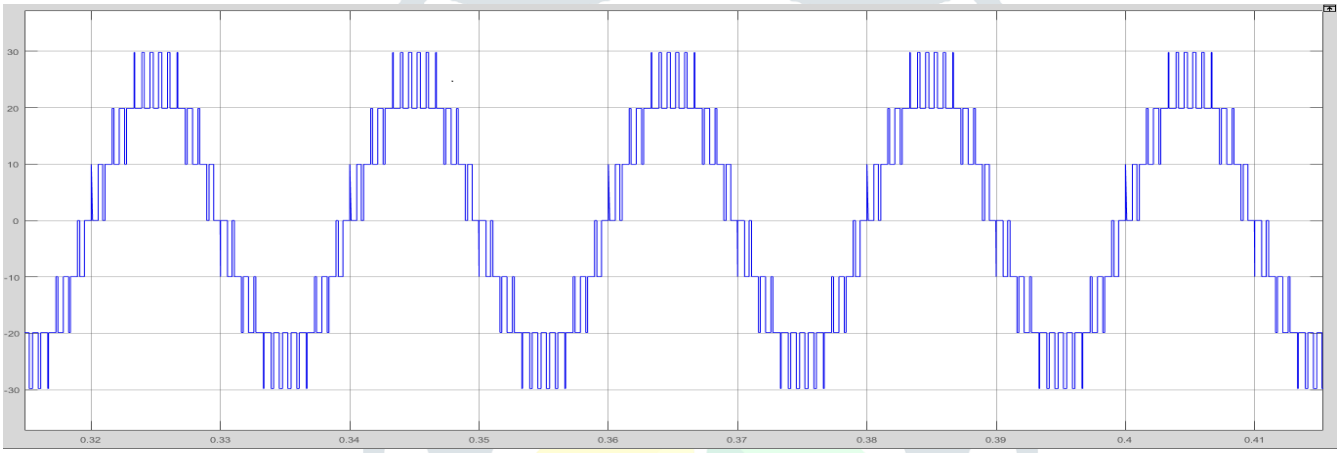

Figure 10 MATLAB results closed loop cascaded H-bridge Inverter model

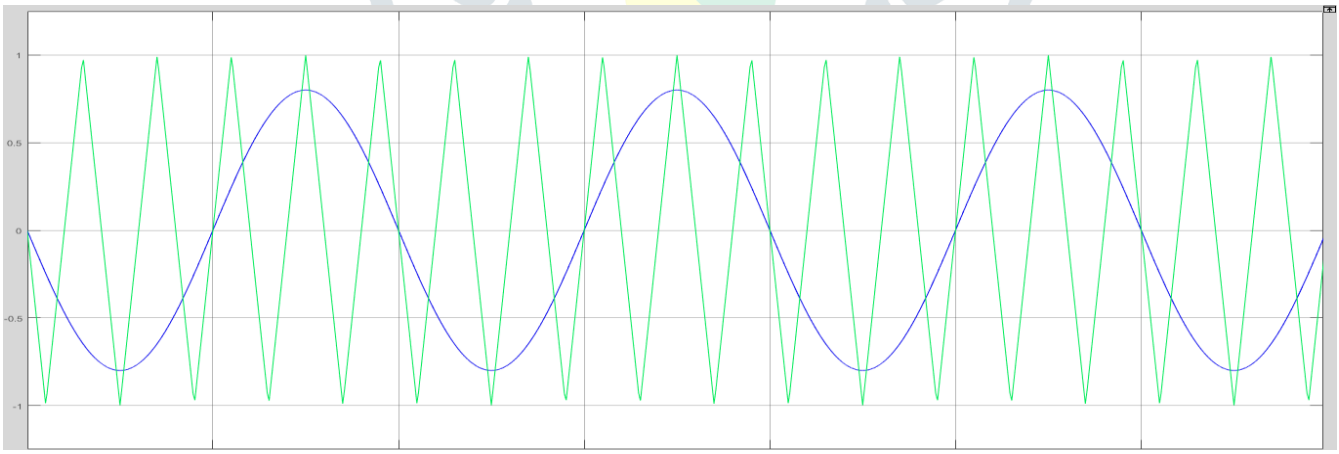

Figure 11 PWM waveform for closed loop H Bridge Inverter

The MATLAB simulation is merged with the hardware component with the help of an Arduino. The six simulated waveforms exhibited Fig.8, are provided to IGBT by employing a Reflectance Transformation Imaging device and Arduino. The 1st (S1) IGBT waveform is drawn from the pin-4, 2nd (S2) waveform from pin-5, 3rd (S3) waveform from pin-6, 4th (S1') waveform from pin-7, 5th (S2') waveform from pin-8, 6th (S3') waveform from pin-9 in the Arduino. So that every provoked waveforms are provided to the IGBT by utilizing an Reflectance Transformation Imaging device or Arduino.

IV. RESULT OF EXPERIMENTATION

To prove and substantiate the viewed topology, a mock-up model of one-phase 7-level inverter is developed on a Hardware setup in the lab. Some IGBT (FGA25N120ANTD) are adopted as switching device, with convenient gate drivers (TLP250), as exhibited Fig.10. 2 batteries are utilised as detached DC sources with potentials v1=2v and v2=4v. 2 isolated DC potential outlets one set at 2 volts and the other at 4 volts are withdrawn from the Regulated power supply (RPS) as exhibited in Fig.13. The MATLAB software codes are typed into the Arduino(UNOR3) which was used to produce switching surge live is exhibited in Fig.8. Switching pulses for the switches S1, S2, S3, S1', S2',S3' are shown in Fig.11,Fig.12 respectively. It can observed that the

switches S1,S1' are triggered at high frequency of switching, and the switches S2,S2' and also the rest of devices operate at the main switching frequency of 50Hz., the switches S3,S3' are operated at a frequency in between the fundamental and carrier frequency.

The inverter was loaded with a 300Ω Rheostat. The output voltage and the THD of the inverter without filter are shown in the Fig.14 (a,b). Output load current of an inverter is 13.8 mA (scale is in mV) as shown in Fig.15. An LC filter was designed to eradicate the higher ordered harmonics, by that the output will get near to the shape of sinusoid voltage. Inductor and capacitor values were chosen using the formulae

$$L = \frac{V_{dc}}{4 f_{sw} \Delta i_{pp}}; \quad f_c = \frac{1}{2\pi\sqrt{LC}} \qquad (1)$$

The specifications for filter design are as follows: DC voltages of 2V and 4V, switching frequency (fsw) of individual switches is in the range of 50Hz to 850Hz, cutofffrequency (fc) is approximately 50Hz, current ripple of 10%.

Using eq. (1) the filter elements are obtained as 18mH, 200μF respectively. The voltage at the output and the THD of sevenlevel-inverter with LC filter as revealed in Fig.16. Output current of an inverter for a Resistive load with LC filter is obtained as 11.9 mA (scale is in mV) shown in the Fig.17.

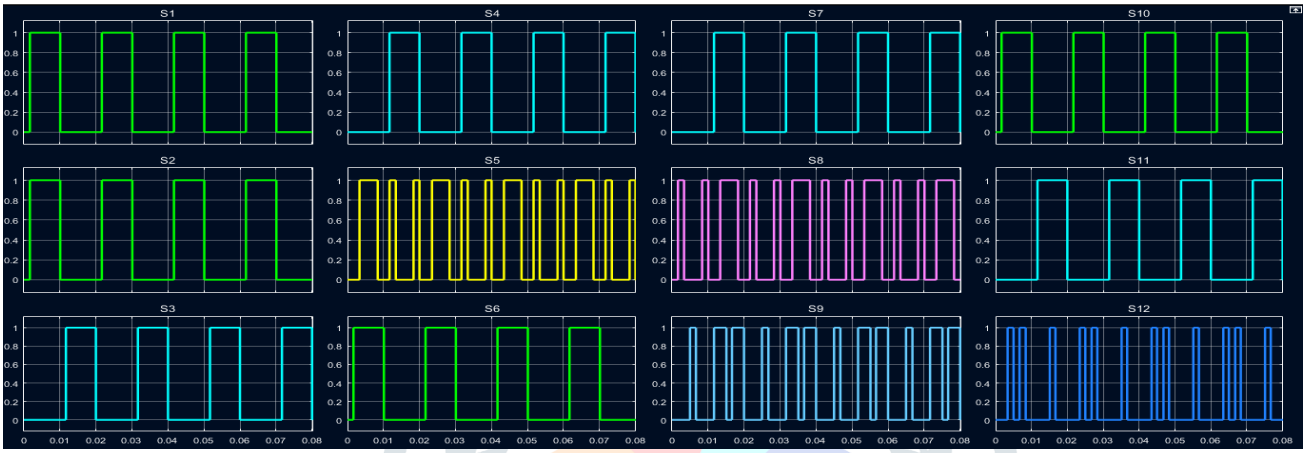

Figure 12 Gate Triggering pulses to the IGBT's(S1,S2,S3)

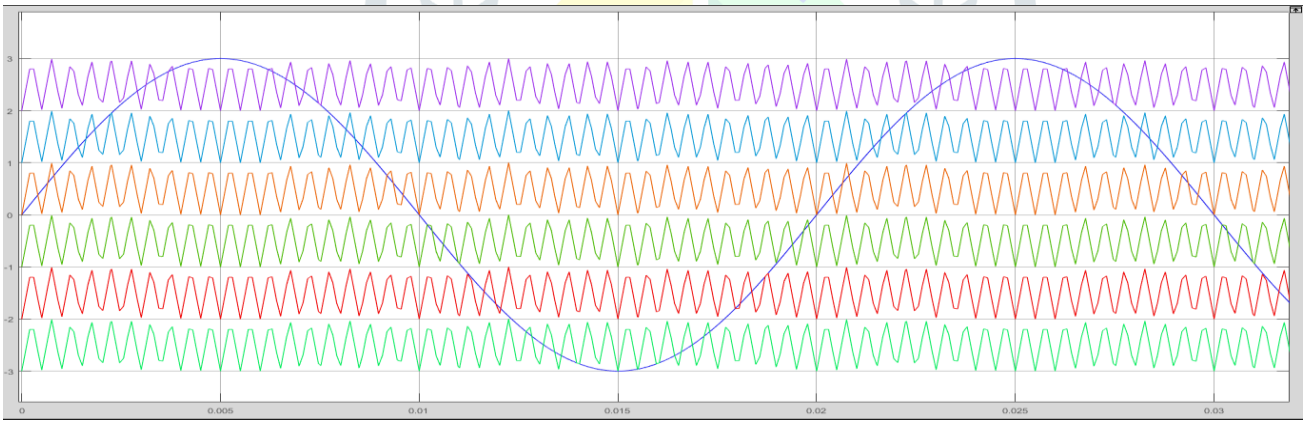

Figure 13 closed loop PWM waveform

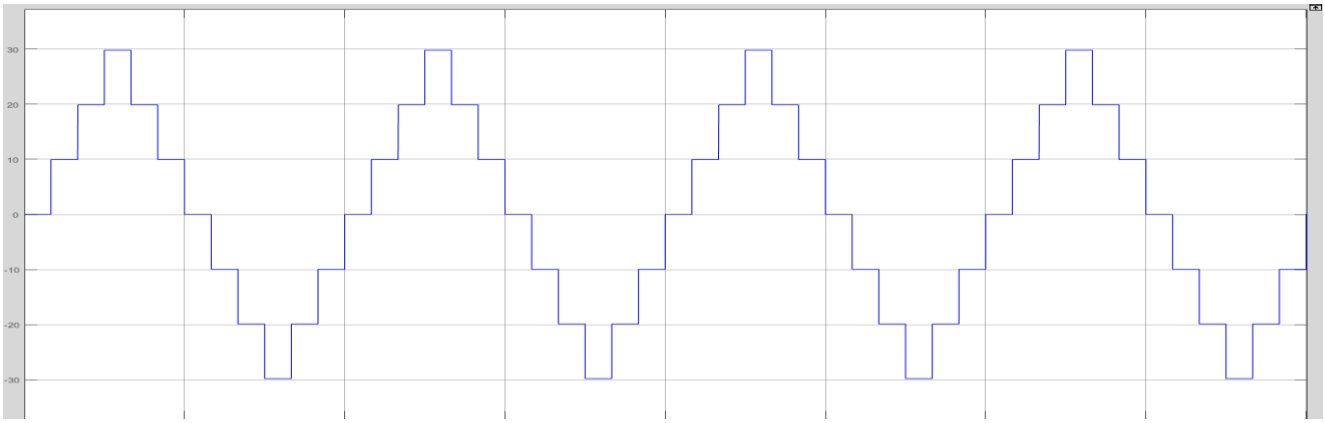

Figure 14 Output voltage open loop

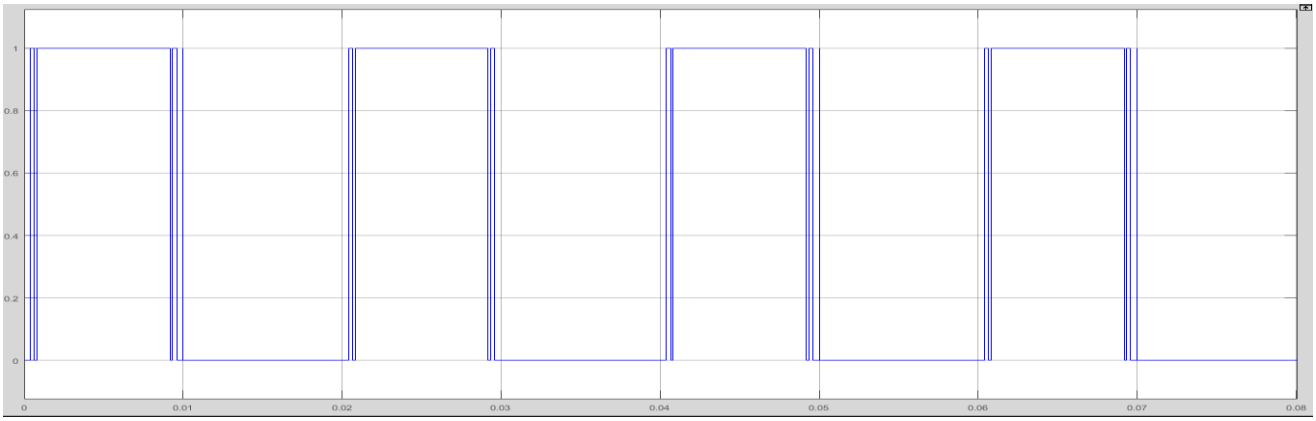

Figure 15 Output voltage and its THD (without LC Filter)

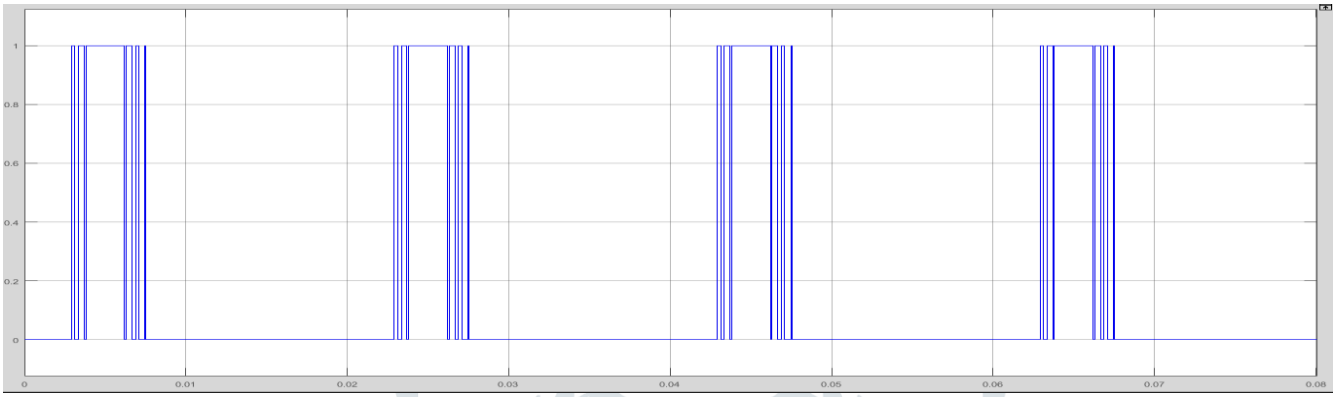

Figure 16 Output current of proposed inverter (without LC Filter)

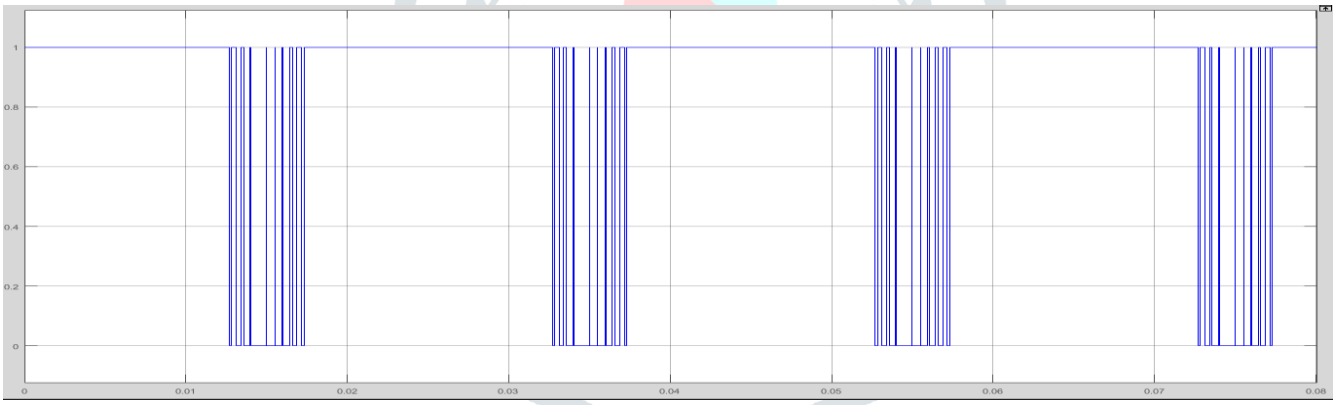

Figure 17 Output current of proposed inverter (with LC Filter)

V. CONCLUSION

A closed loop cascaded H-bridge inverter is made that can help in lower total Harmonic distortion, flexibility, and price in contrast to regular cascaded H-bridge inverter in open loop. Such a layout need reduced number of switches, and lower price and also live interacting device (Arduino) in contrast to Digital Signal Processing, DSPACE, etc., all totally the payments and expenses for building the topology reduces. This paper shows the working of suggested structure. An LC filter is provided that assists in obtaining approximate sinusoidal pulse waveform. The concepts that are showcased here is proved through MATLAB simulation and experimental results. Satisfactory results are obtained and are solved in Table 2.

TABLE 2. MATLAB/SIMULINK AND HARDWARE RESULTS COMPARISON

	SIMULATION		HARDWARE	
	Without LC filter	With LC filter	Without LC filter	With LC filter
RMS value	3.47V	3.87V	2.83V	1.60V
THD	21.69%	4.6%	27.7%	6.71%

VI. REFERENCES

[1] E. Babaei and S.Hosseini, "Charge balance control methods for asymmetrical cascade multilevel converters". In Proc. ICEMS, Seoul, Korea, 2007, pp, 74-79.

[2] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1943–1954,May 2013

[3] J. Napoles, A. J. Watson, and J. J. Padilla, "Selective harmonic mitigation technique for cascaded H-bridge converter with nonequal dc link voltages," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1963–1971, May 2013.

[4] N. Farokhnia, S. H. Fathi, N. Yousefpoor, and M. K. Bakhshizadeh, "Minimisation of total harmonic distortion in a cascaded multilevel inverter by regulating of voltages dc sources," IET Power Electron., vol. 5, no. 1, pp. 106–114, Jan. 2012.

[5] S. Mekhilef, M. N. Abdul Kadir, and Z. Salam, "Digital control of three phase three-stage hybrid multilevel inverter," IEEE Trans. Ind. Informat., vol. 9, no. 2, pp. 719–727, May 2013.

[6] S. Laali, K. Abbaszades, and H. Lesani, "A new algorithm to determine the magnitudesofdcvoltage sources in asymmetrical cascaded multilevel converters capable of using charge balance control methods," in Proc. ICEMS, Incheon, Korea, 2010, pp. 56