VLSI IMPLEMENTATION OF SWITCH FABRIC ARCHITECTURE IN ATM NETWORKS

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Abstract

VLSI (Very Large Scale Integrated) design and implementation of cell-based high-speed multicast switch fabric uses the 0.18 µm CMOS innovation. Using distributed control, multistage interconnection organize structure, and modular design, the multicast adjusted gamma that is also known as Balanced Gamma (BG) switch includes an adaptable, high execution architecture for unicast, multicast and combined traffic under both uniform and non-uniform traffic conditions. The BG switch takes after predominantly a yield supported architecture and utilizes a self-replication mechanism for multicast traffic switching. We are developing ATLAS-I (ATm multi-LAne backpressure Switch One), a single-chip ATM switch with optional credit-based (backpressure) flow control. The present observation has four procedures, which improves the execution of the traffic booking forms for ATM frameworks. The shaper utilizes a parallel date-book based VLSI architecture to accelerate the procedures of observing, registering needs and refreshing pointers. The quantity of components is relative to the number k of needs identified with the traffic profiles of the ATM associations. Every association shows a productive answer for the issue of accelerating the processing of the vacancies for transmitting ATM cells while keeping the required VLSI range little and also disentangling the control. Accordingly, the speediest of the four associations utilizes k handling components it records and registers a timeslot in log 2k ventures when contrasted with the consecutive date-book calculation. This takes a self-assertive large number of steps for this calculation. The whole framework constitutes a part, which can effectively oblige either a switch or a wise cushion.

Keyword: VLSI, ATM, CCITT

Introduction

Amid the 1980s, the idea of ISDN, particularly the NISDN was presented. Around '85 the CCITT think about gathering XVIII began another movement to characterize guidelines for the BISDN. Since BISDN is a more adaptable system and it will be the eventual fate of correspondence, analysts centered their consideration on it. The circuit switching system was the real switching strategy utilized as a part of these networks around then. Amid the year 1988, ITU-T (in the past the CCITT) institutionalized a quick bundle switching idea called Offbeat Exchange Mode (ATM) for the coordinated administrations.

VLSI design and implementation of a new cell-based high-speed multicast switch fabric using the 0.18 mum CMOS technology. Using distributed control, multistage interconnection network structure, and modular design, the multicast balanced gamma (BG) switch features a scalable, high performance architecture for unicast, multicast and combined traffic under both uniform and non-uniform traffic conditions. The BG switch follows predominantly an output-buffered architecture and utilizes a self-replication mechanism for multicast traffic switching. We are developing ATLAS I, a single-chip ATM switch with optional credit-based (backpressure) flow control. The chip has 16 input and 16 output serial gig baud pins, and can be configured as a 16 x 16 switch at 622 Mb/s/link, or a 4 x 4 switch at 2.5 Gb/s/link, or in various combinations thereof. It offers sub-microsecond cut-through latency, multicasting, three priority levels (service classes), a 256-cell on chip shared buffer that contains multiple logical queues organized per-output and per-priority, on-chip VP/VC translation table (4096 entries), and load monitoring support. ATLAS I is a general-purpose building block for high-speed communication in wide (WAN), local (LAN), and system (SAN) area networking, supporting a mixture of services from real-time, guaranteed quality-of-service to best-effort and burst and flooding traffic, in a range of applications from telecom to multimedia and multiprocessor networks of workstations (NOW). The chip can be optionally configured to implement credit-based flow control (multi-lane back-pressure), in hardware, at the individual cell level, at the granularity of 4096 flow groups per link. Network systems can take advantage of this feature in either or both of the following ways. A large switch "box" can be built, with hundreds or thousands of ports, using a switching fabric made of ATLAS I chips, where multi-lane backpressure is used inside the box to provide the high performance of output queuing at the low cost of input queuing; any desired flow control method can be employed outside the box. Networks that employee credit based flow control can be built directly out of ATLAS I chips. In SAN or LAN environments, the low latency and the multi-lane back-pressure of ATLAS I provide ATM networking with the features and performance of wormhole routing. This is an ideal setting for making NOW that provide multi-processor performance at affordable cost.

TYPES OF SWITCHING ARCHITECTURE

The fast pace of innovative change in correspondence and PCs has presented numerous new switching framework ideas to take into account the requirements of the clients. Diverse switch fabric outlines have been proposed and created at different research associations in the course of recent years. Every one of these outlines utilizes a high level of parallelism, dispersed control and the steering capacity.

In the underlying stages, the Quick Circuit Switching (FCS) idea was utilized to utilize the ATM. This thought depends on the quick setting up and bringing down of associations, to such an extent that the framework does not assign any circuit to a client, amid its sit still time. Ross et al (1977) proposed architecture for coordinated impetration/voice with FCS interestingly. The type of dispersed quick circuit switching called burst switching was accounted for by Ahmadhi. H (1989) since the fast packet switching

(FPS) idea is the fundamental switching procedure which underpins an extensive variety of administrations with various piece rates, ATM arrange utilizes this strategy. In this way, the different sorts of switching architecture proposed depend on bundle switching ideas. The sorts of switching architecture are ordered by their inside fabric structures as

1. Banyan and cushioned Banyan
2. Sort Banyan
3. Fabrics with disjoint way topology
4. Crossbar based
5. TDM based
6. Fabrics with Shared medium

Also, as per the way of working, they are arranged into blocking and Non-blocking sorts. The fundamental useful units of a modem switch or switch are line interfaces; organize processors, switch fabric and framework processors.

SHARED BUFFER SIZE

Helix Switch

The Helix switch utilizes a self-routing shift enroll ring intended to exchange cells between the impetration and yield ports and uses an effective shared buffer plan at the yield. The switch is composed utilizing dynamic locks and in this way it requires a little zone. Since the move enroll serializes the conveyance of cells to the goal the simultaneous cells headed for a similar yield touch base in an interleaved design. Along these lines, the helix switch settles yield conflict. It is proposed in that the Helix switch architecture is appropriate for VLSI execution since it utilizes short interconnections, low fan out for the entryways and not very many rationale levels hence diminishing the deferral and territory.

In the Helix switch it is accepted that the line interface module (LIM) at the input connection of the ATM hub gets a serial piece stream from the connection and proselytes it into a parallel arrangement of bytes or words. Moreover, the cell mark is prepared in the LIM to distinguish the yield port onto which the cell must be transmitted. The yield port address is pre-pended onto the ATM cell and is then sent to the Helix switch. The Helix switch then courses the cell to the fitting yield port as showed by the pre-pended yield port address. The ATM cell is then changed over into a bit stream and transmitted onto the yield interface. Figure 1.3 demonstrates the piece schematic of an ATM hub.

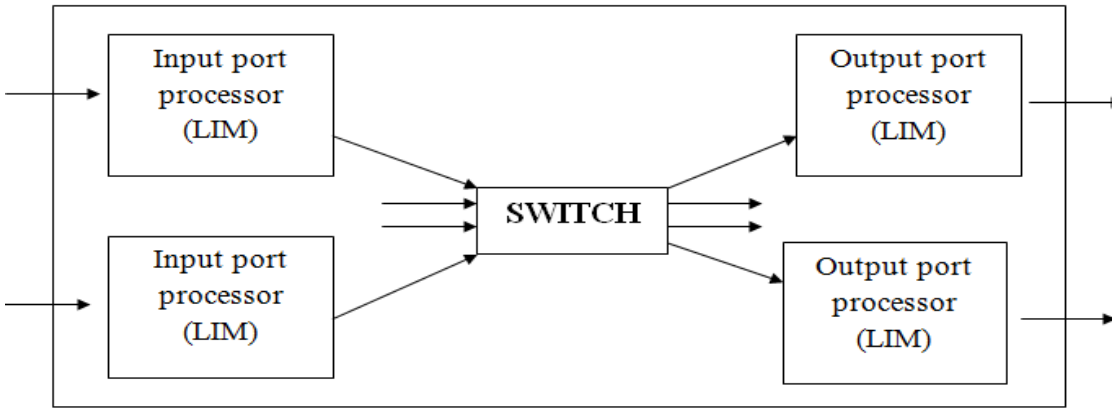

Figure 1: An ATM node

Figures 2 and 3 demonstrate the variety in the cell misfortune execution when the quantity of buffers/port is differed and the measure of load on the switch is changed individually. The chart appeared in figure 2, exhibits the relationship between buffer size and the cell misfortune proportion at 90% load. The idea of shared buffer banks is additionally appeared in the chart. The sharing diminishes the aggregate number of buffers required to accomplish a wanted cell misfortune proportion.

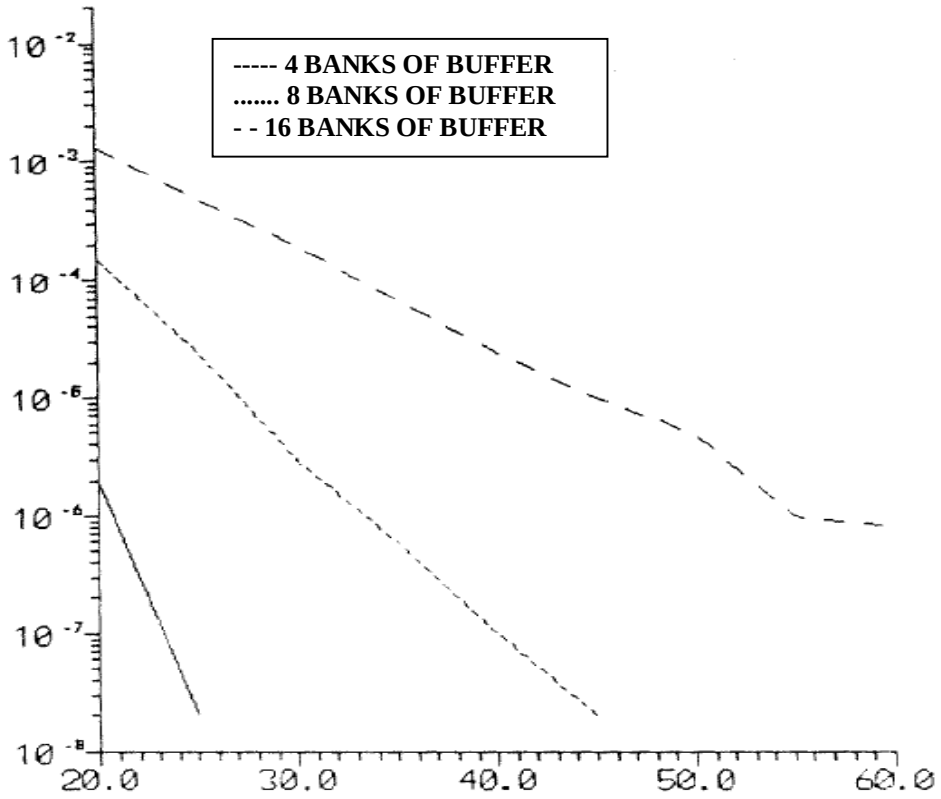

Figure 2: Cell loss ratio at 90% load utilizing Shared yield buffers

M- NUMBER OF BUFFERS PER PORT

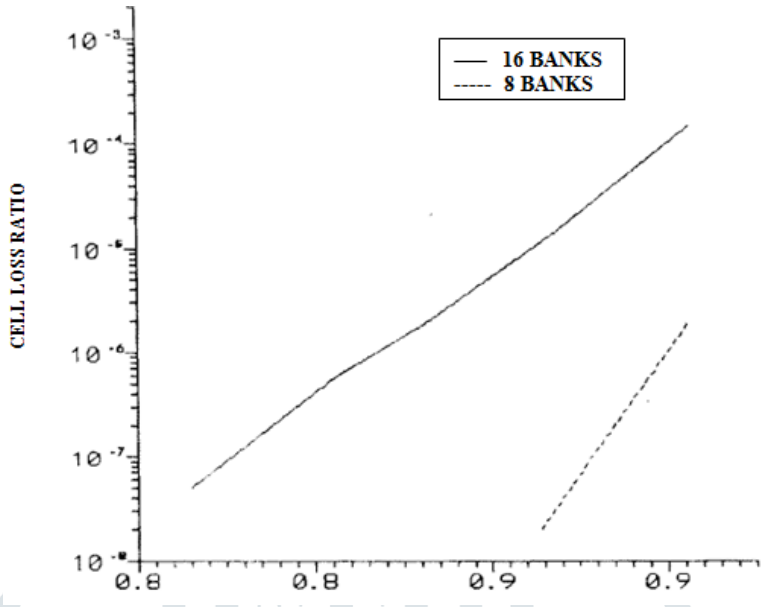

Figure 3: Cell loss execution of Helix under Shared buffer plan of size 16 X 16

Simulation and Verification

In the wake of having portrayed the functions of the considerable number of modules, the following stage in Very Large Scale Integration (VLSI) design execution is to check the functions of the design. Utilitarian verification gives the planning diagram for the design. The planning diagram for every one of the signals in the design is checked by the functions of the design. The software tool utilized for this planning verification is Modelsim (Simulation Tool of Model Technology, Registered Trademark of Mentor Graphics Company).

Keeping in mind the end goal to test the design utilizing this tool, test seats are composed for every one of the modules. The test seat incorporates the example inputs given to the module and the functions of the module. After accumulating the test seat utilizing the software tool, and recreating, the planning diagrams are created which demonstrates every one of the waveforms relating to every one of the input and output signals in the module. Both useful planning and basic planning investigation are done. This strategy is taken after for all the fifteen modules in the design. Every one of the modules is independently mimicked and timing diagrams are created and checked. It was discovered that the functions of the design modules are figured it out. The accompanying segment depicts the functions of the design modules identifying with the waveforms.

Segmentation Module Simulation

a. Packet composes operation in Segmentation Module: The simulation demonstrates the compose operation in this module. In the event that PKT START is 1 then the input information originating from PORT_CELL32JN is composed in the memory gave SEGRDENIN is 0.

b. Segmentation Read Operation: The waveform demonstrates the read operation from Segmentation Module. Stream of incoming information is divided into 48 bytes each and moved through PORT_CELL32_OUT as far as 32 bits for every clock cycle. The reading happens just when SEG_RD_EN_IN is 1, which is set by ATM host interface Module showing that the following 48 bytes can be exchanged. The information that is built into the memory of Segmentation Module amid the SEG WRITE operation is then exchanged to the ATM host interface module. The waveforms demonstrate the output of PORT_CELL32_OUT.

c. Flag set operation after segmentation is finished: The simulation demonstrates that the CELL_RDY_OUT is influenced 1 when 12 to isolate the compose pointer and if the remainder is one. The flag SEG_READ_PACKET_OVER_OUT is set to 1 demonstrating that the segmentation operation is finished.

ATM Host Interface Module Simulation

a. Port 0 to Port 2 VPI connection: In sw_PORT 0_cELL32 0UT amid the first clock pulse 01400000 (HEX) is appended, and amid the second clock pulse 00000000 (HEX) is sent and amid the third to fourteenth clock pulse SEG_CELL32_IN (Payload) is sent. Amid this time SW_PORT 0_CELL32_OUT is made 1.

b. Port 0 to Port 3 VPI connection: In SW_PORT 0_CELL32_OUT amid the first clock pulse 01900000 (HEX) is sent, and amid the second clock pulse 00000000 (HEX) is joined and amid the third to fourteenth clock pulse SEG CELL32 IN (Payload) is sent. Amid this time SW PORT 0_CELL32_OUT is made 1.

c. Port 1 to Port 2 VPI connection: In SW_PORT l_cELL32 0UT amid the first clock pulse 02800000 (HEX) is sent, and amid the second clock pulse 00000000 (HEX) is sent and amid the third to fourteenth clock pulse SEG_CELL32_in (Payload) is sent. Amid this time SW_PORT l_CELL32_OUT is made 1.

d. Port 1 to Port 3 VPI connection: In SW PORT l_CELL32_OUT amid the first clock pulse 05000000 (HEX) is joined, and amid the second clock pulse 00000000 (HEX) is sent and amid the third to fourteenth clock pulse SEGCELL32IN (Payload) is sent. Amid this time SW_PORT l_CELL32_OUT is made 1.

Switch Incoming Interface (SII) Simulation

a. Writing the ATM Cell: In this waveform, it can be seen that when INC_WR_EN_IN is 1 then the ATM cell from ATM Host Interface Module is composed in the memory.

b. Reading the ATM Cell: In this waveform, it can be seen that when INC_RD_EN is l then the information, which was composed in the memory, is read through PORT_CELL32_OUT.

c. Header Slicing: In the waveform, it can be seen that the header is cut and it is conveyed to HVF. Amid the primary clock pulse, first set of header, which originates from PORT CELL32 IN, is put away in the LSB of brief enlist named CELL_HDR_OUT TEMP. Amid the second clock pulse the header is moved from LSB of CELLHDROUTTEMP to MSB of CELLHDROUTTEMP. At the same time second set of header, which originates from PORT_CELL32_IN, is put away in the MSB of transitory enlist named CELL_HDR_OUT_TEMP. At that point 40 bits of header is cut from impermanent enlist and it is conveyed through INC CELL HDR OUT.

Main Memory FSM (MMF) Simulation

Flag set operation for SII and MMC: If the MEM_CURR_STATE moves toward becoming 10 then INC_RD_EN_OUT and MEM_WR_EN_OUT are made 1 showing the SII to exchange the following ATM cell. The second flag MEM_WR_EN_ouT is set to Main Memory Control showing that the ATM cell can be built into the MMC. The VALID_HDR_FLAG_IN flag is additionally set in this case.

Main Memory Control (MMC) Simulation

a. Writing the ATM Cell: In this module if MEM_WR_EN_IN, which originates from MMF, is 1 then the ATM cell is composed in the memory.

b. Reading the ATM Cell from MMC: In this module if mem_rd_en_jn, which is set by MMF, is 1 then the information, which was composed in the memory, turns out through MEM_DATA_OUT.

RESULT AND DISCUSSION

The whole design is recreated and preview perspective of the fundamental signals is appeared in Figure 4. The figure demonstrates the simulation for 144 bytes of input to the ATM switch. The design depends on the determination that it takes 12 clock cycles for payload and 2 clock cycles for the header to be composed or read from a module having memory. As indicated by the design determinations, a sum of 14 clock cycles are required for writing an ATM cell in any memory of the ATM switch. One clock cycle is taken as 1 nanosecond. Henceforth, it takes 14 nanoseconds for any module having memory to process an ATM cell.

Speed Calculations

- It takes 14 clock cycles to compose an ATM cell into Switch Incoming Interface.
- It takes 14 clock cycles to compose an ATM cell into Main Memory Control.
- It takes 14 clock cycles to read an ATM cell from Main Switch FSM.
- Simulation speed = 100 Pico seconds
- 1 clock = 1 nanosecond

Switch Latency

- It is the time slipped by between cell entering the switch and cell leaving the switch.
- Switch dormancy =14 +14 = 42 clocks.
- The switch needs 42 nanoseconds for switching process. The Tables 6.1 and 6.2 give the speed computations for the single chip switch

Table 1 Speed calculations

Time	Bytes
42ns	48 bytes
1s	1.142 * 109

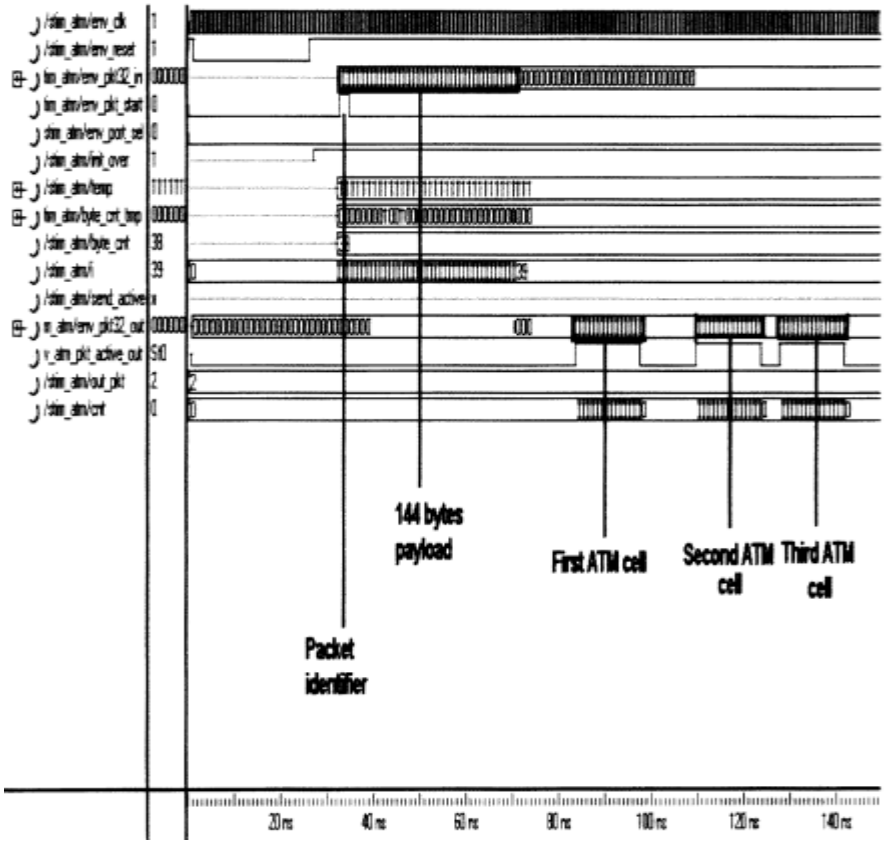

Figure 4 ATM Switching Waveforms

Conclusion

In the light of above study and observation on the topic of "VLSI IMPLEMENTATION OF SWITCH FABRIC ARCHITECTURE IN ATM NETWORKS", I hereby summarize the following conclusions.

Applications and communication network capacity are actually changing at an enormous price for the past 2 years. Besides extremely high speed, lots of real time applications, like videoconferencing, music on demand, and video on demand need communications being delivered to much more than a single location. As an outcome, supporting multicast has turned into an essential requirement for just about any switch created for future broadband communication networks. ATM-like fixed sized packet switching attracts much interest due to the program of its in advanced Internet routers and also switches. A variable sized incoming IP package is internally segmented into fixed size ATM like cells that are changed on the output ports, wherever they're reassembled to the IP datagram. Borrowing from ATM terminology, we utilize the phrase cell to determine the fixed sized packet utilized in the switch, that could be ATM cells, and some other convenient data format [two]. Multistage interconnection network (MIN) design is now an appealing alternative for high speed broadband switch architecture as a result of many attractive attributes like self routing, modularity, distributed control, consistent delay for those input output suitability and pairs for VLSI implementation. A multicast switch fabric with the implicit cell replication is chosen since it includes the routing and replication capabilities into one unified system. This particular design type is going to inherit a lot of the appealing options that come with the MIN design.

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