A Review on Techniques for Power Management in Embedded Systems

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Abstract- *At present all the electronic devices are built by Embedded processors. However, the power management is one of the most critical design issue in these Electronic devices. The basic idea behind any power management method is to maximize the system performance within the given power budget. Today because of many high-end embedded processors development, the number of just mobile devices reaching almost equal to the population of the earth. However, these developments, have also made the task of managing the power consumption in these devices extremely challenging option. In this context the Embedded system designers worked towards development of many power management techniques for Embedded systems. This review paper, highlights the need of power management in Embedded systems and reviews several research works towards development of power management techniques for Embedded systems. To a certain extent, the intention of this paper is to help the researchers and Embedded system developers in gaining insights into the working of power management techniques and designing even more power aware design methodologies for tomorrow's Embedded systems.*

Keywords*: Embedded systems, Classification, review, survey, Power management techniques.*

I. INTRODUCTION

Embedded System is defined as a computational system with software embedded into the hardware to perform the predefined or specified task. Moreover a typical Embedded system can be viewed as a base hardware platform, which executes application software and many peripheral devices connected to different ports. The hardware platform consists of the processing units like CPU, communication channels and the memory elements. Operating system, application level code belongs to software implementation. Power efficiency can be obtained by managing power dissipation in all the parts of the overall system.

In recent years the Embedded systems are growing in phenomenal way in terms of new features and applications. Mobile Embedded devices now offering integration of multimedia applications, wireless data feature, internet browsing and phone. In addition, these new trends also urging for managing power consumption. Further, it's known that, the use of mobile devices has now reached almost equal to the population of the world [1]. In this context, designing an Embedded system with high performance and low power consumption is a major challenge for Embedded system designers.

In this paper, we mainly discuss the necessity of power management in Embedded devices and tried to review some of the research works which are intended at improving energy efficiency of Embedded systems. It's believed that this review may help the researchers and designers in understanding the need of power management in Embedded systems and also motivates them to think for further enhancement.

This paper is planned as follows. Section II presents a background and also the necessity of power management in Embedded systems. Section III explains the power management issues, the designer has to focus in designing power optimized Embedded systems. Section IV addresses classification and discussion on some of the power management techniques developed for Embedded devices. Finally, Section V provides conclusions and also the future challenges.

II. BACKGROUND

In the future, many Embedded devices are expected to become mobile convergence devices. To support multiple features, a mobile convergence device is required to have a lot of processing power. However, many of the Embedded mobile devices are operated with batteries, with limited energy capacity. So, managing power consumption while reaching the throughput requirement of all the functions has been regarded as one of the most crucial issue in designing Embedded mobile devices.

The Embedded systems can be classified based on the power, as portable Embedded Systems and non-portable Embedded Systems. Designing portable Embedded Systems with limited power consumption and high performance is a major challenge. Some of the notable examples of Embedded Systems include DVD players, Digital cameras and mobile phones etc.

For the following reasons but not limited, managing the power in Embedded systems is important [31].

- *Small Size and Battery Life*

For battery functioned mobile Embedded devices, power supply is a crucial aspect. More power consumption from the device leads to heating, which is undesirable in many Embedded Systems. Further, the size of the systems also restrict the amount of heat dissipation that can be managed.

- *Reaching Performance Requirements*

In the ongoing scenario, Embedded processors are used to execute resource concentrated applications like multimedia processing etc. To reach these performance demands, recent Embedded processors are built with complex structures such as multi-cores, multi-level caches etc. Most notably multicore structures are deployed in many Embedded system areas. Certainly these developments have made the

design of Embedded Systems to be optimized for power consumption.

- *Ensuring Longevity*

In [2] described, certain degree of temperature rise leads to the device failure rates by up to a factor of two. This shows power dissipation has effect on reliability of Embedded devices and this factor may be crucial for certain class of Embedded devices like medical Embedded devices and mission critical Embedded devices.

III. OVERVIEW

In designing power optimized Embedded Systems the designer has to focus on the three main power issues [4].

- Power Measurement
- Power Analysis
- Power Management

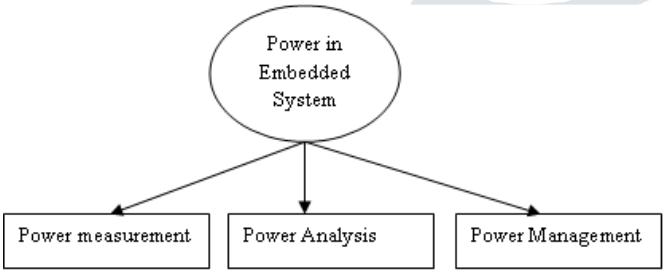

Figure 1: Power Concern in Embedded System

1. *Power measurement*

In a typical Embedded system the power measurement is possible either at hardware level or software level. The hardware level refers to the measuring of CPU, communication channels, the memory units and peripheral devices power and in the software level measuring power is based on the simulation models rather than a hardware measurement. Simulation based approaches are widely preferred over hardware to achieve the objective as simulations can be executed at different levels.
Liang-Bi Chen *et al.* [3] proposed measurement of the real hardware power on ARM based SOC development board and presented a power analysis platform to aid the designer to measure, analyze and control the behavior of complex Embedded applications in real-time. Successfully demonstrated the usefulness of this platform with a case study by first characterizing the power usage of a Digital Still Camera (DSC) and then improving its power efficiency through dynamically taking quality and energy into consideration.

2. *Power analysis*

Analysis of power includes various measurement, experimentation, estimation and techniques to evaluate power and validate the power consumption in a system. Power analysis is used to model the power consumption of the various components including the CPU, memory units and peripherals. Analysis of power consumption has been a hot research topic for many years. For any power saving mechanism, it is necessary to monitor the power used by the system to guide its decision. Study undergone on this issues are explained in [5-7] as examples. Jason Flinn *et al.* [8] developed a tool called *PowerScope* to profile the energy used by mobile application. The PowerScope can analyze the energy consumption based on the power used by various segments of a program structure. Tested the effectiveness of the tool on an adaptive video-payer to reduce the energy consumption.

3. *Power Management*

Power management is, any electronic device feature that allows users to manage the quantity of power consumed by an underlying device, with minimal impact on performance. Power management allows the switching of devices in various power modes, each with different power usage characteristics related to device performance.
Power management has become a major issue in the design of Embedded systems. There are many adverse effects like unstable thermal properties of the die, effect the system performance and also result in increasing power consumption. This makes power consumption issue sometimes more important than speed of the system. The power management in Embedded systems design can be achieved at different levels like, at chip level, architectural level, application level and system level. Among all these, system-level power management techniques have importance, because, to reduce the power consumption, it's to better to follow an intelligent power-aware technique than low-power design[9].

IV. POWER MANAGEMENT TECHNIQUES

Based on their main power saving approach, power management techniques can be classified as follows.

a) DVFS (Dynamic voltage and frequency scaling)

b) Dynamic Power Management (DPM)

c) Architecture level power management

d) Application level power management

Further in this section, some of the power management techniques related to the above classification is discussed.

a) Dynamic Voltage & Frequency Scaling:

DVFS is a method of changing the voltage and frequency of an electronic system based on performance and power requirements. This method basically refers to the change in voltage levels supplied to various system components during runtime so as to reduce the overall system power consumption while maintaining the throughput requirement. In a system primarily the power consumption is monitored by the following equation:

$$P=CV^2f \quad (1)$$

where P is the power consumed, C is the switching capacitance, V is the supply voltage and f is the frequency of operation. It is possible to control the amount of consumed power by simply adjusting voltage-frequency pairs. Several commercial Embedded processors support DVFS technology

for saving the power. The basic idea is to tune voltage and frequency pairs within a predefined levels, to reach the required power and performance level. As an example, DVFS method for a dual-core processor can be viewed as shown in figure 2.

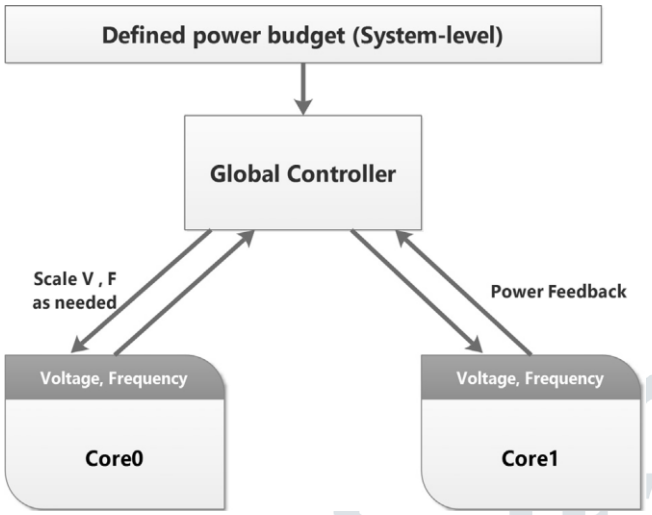

Figure 2: DVFS applied to a Dual-core processor

The system level controller guides the global on-chip controller with the suitable power budget. The global controller checks for voltage, frequency and power usage of each core. Based on these parameters, the global controller actuates voltage and/or frequency as and when required. DVFS methodology is widely applied to almost all modern processors in Embedded Systems, rather than only in general purpose applications [10]. Hua et al. [11] discussed the importance of DVFS in saving the power in Embedded computing systems using DVFS and addressed DVFS can also be used in real-time applications. In [12] discussed the energy minimization factor when running real-time applications that have strict reliability and deadline necessities. Checkpointing, Dynamic Voltage Frequency Scaling (DVFS) and backward fault recovery techniques are used to confirm the satisfaction of the running application's reliability and deadline necessities.

Quan et al. [13] proposed DVFS based methods for optimizing energy in real-time Embedded systems. Studied the problem of determining the optimal voltage schedule, for a real-time system with fixed-priority jobs, running on a variable voltage processor. Also shown that in designing many real-time Embedded systems, proper usage of variable voltage processors can dramatically reduce system energy consumption.

Edward khan et al. [14] presented an investigative algorithm, based on mathematical optimization techniques to identify energy-aware processor frequencies for soft real-time Embedded systems. Using the mathematical models it was possible to identify the desired frequency for a task assuming availability of constant range of frequencies. The proper selection was based on choosing, the closest frequencies which are lesser and bigger than the desired frequency and some of the time each of them should be used to reach the deadline from real-time tasks. This approach provided performance improvements for the issue of multiple target deadlines for each task.

Wonyoung Kim et al. [15] discussed DVFS methods for each core, in chip-multiprocessors (CMP) systems for optimizing energy. They experimented the DVFS methods by considering practical overheads, voltage transition time and advantages, by using on-chip voltage regulators in a 4-core multiprocessor.

b) *Dynamic Power Management:*

Dynamic power management mainly deals with development of policies. These policies analyse run time behavior of the system to optimize the overall power consumption of the system, when the application is running, by selective shut-down of the system components which are idle. In Embedded systems, normally all the system components work in different operating modes, using these operating modes, it is possible to save the overall system power consumption, since different modes may consume different quantity of energy and take different time to return back to their usual mode. By judiciously utilizing these modes in the context of performance loss bounds, like a low-power mode can be used when the system is idle, shutting down the resources during their periods of inactivity etc, it is possible to optimize the overall system energy consumption. In general the rules to determine operating modes of the system components are called as policies. The objective of any power management policy is to optimize the power consumption of any electronic system by pushing system components into different operating modes, and always each mode is signified by certain performance and power consumption level. The defined policies identify the operating modes of system components based on the system history, workload, and performance constraints. Till today many research works are carried-out to develop many Dynamic power management policies.

Huaxiang Lu et al. [16] proposed two dynamic power management policies of type Back propagation and Radial Basis Function based on Artificial Neural Networks (ANN). Experimented these two policies on an IBM mobile disk system to lower the power consumption in system-level greatly.

Wai-Kong Lee et al. [17] proposed effective hybrid model Dynamic Power Management to predict the idle period in portable Embedded systems. The proposed model combines Moving Average (MA), Time Delay Neural Network (TDNN) and random walk model to perform idle period prediction. Experimented these algorithms on portable Embedded devices by assuming the device workload characteristics are always varying according to the user usage pattern.

Rong Ye et al. [18] presented learning algorithm based DPM framework for multi-core processors platform. Included task allocation into learning based, to manipulate idle periods of each processor core. Experimented proposed DPM on synthetic workloads of multi-core processor (4-core, 8-core) Embedded systems to verify the effectiveness in terms of power consumption as well as system performance. Experimental results shown that, the include of learning algorithms in DPM policies significantly performs well.

Young-Si Hwang et al. [19] proposed a predictive power management scheme based on collecting and analyzing information on the status of I/O devices access patterns while the system is running the applications. Proposed scheme distinctive feature is the capability of predicting upcoming I/O

accesses by comparing the previously stored access pattern and the currently occurring execution patterns. Verified the proposed approach by running a set of applications and performance comparison has done.

Ki-Seok Chung et al. [20] proposed a dynamic power management technique for multi-core Embedded processors based on a well-known parallel programming paradigm OpenMP, by utilizing its parallelized property. The proposed technique identifies how many cores are required for certain running application (Number of necessary cores for a given task during run-time). By turning off unnecessary cores, power consumption can be reduced. verified the effectiveness of the technique on Intel Quad Core processor platform and ARM-11 MPCore platform.

W. Lloyd Bircher et al. [21] presented, optimized hardware and operating system configurations to reduce average active power in a multi-core processor such as AMD Quad-Core Opteron. They unveiled that the performance loss and power consumption can be minimized through careful selection of hardware adaptation and operating system control parameters in the case of multi-core Embedded processors. Also discussed the fact, designers can save power while maintaining performance by balancing active to idle transitions in the system properly.

c) Architecture level power management:

Several researchers have proposed architectural level power management techniques for optimizing energy in Embedded systems. Architectural level techniques for power savings include components (CPU core, Device drivers, Memory, registers and bus protocols) dynamic reconfiguration, and generic techniques like clock gating, on-line profiling based monitoring and control etc.

Manjusha M. Kinage et al. [22] designed a soft core processor with dual core by using various Commercial-Off-The-Shelf (COTS) devices. Analysed the power consumption of each cores using XPA (Xilinx Power Analyzer), based on the analysis, they tried to optimize the design towards the lower power consumption.

Lei Yang et al. [23] presented an effective online software-based RAM compression technique for battery-powered, disk-less Embedded systems. Though maintaining high performance and low energy consumption, adjusting the effective RAM capacity dramatically without hardware design changes was their goal. To achieve this, taken advantage of an operating system's (Linux kernel module) virtual memory infrastructure, through keeping swapped-out pages in compressed format.

Emil Talpes et al. [24] proposed a power efficient processor Micro-architecture, based on instruction re-execution. Their goal is to re-execute the instructions as much as possible from the computations performed during previous implementations. Saved the overall power consumption by re-executing the instructions that are already fetched, decoded, executed, and have their registers already retitled, by turning off, front end of the pipeline architecture for large period of time. Experimental results have shown the improvement and the percentage of power reduction is dependent on size of execution cache (EC).

Yi-Ying Tsai et al. [25] proposed an instruction cache memory structure called Trace Reuse (TR) Cache to save processor power towards instruction accesses. Their idea is to improve the performance and power efficiency of a Embedded processor, from reusage of the retired instructions available in the pipeline back-end of the processor. The proposed TR cache acts as an additional instruction delivery mechanism and achieves higher instruction rate.

Samira Ataei et al. [26] proposed power efficient transistors based SRAM memory architecture, suitable for different Embedded multimedia applications. Proposed architecture improves the static noise margin during read and write cycles, so that reduces leakage current in retention mode. Voltage scaling option is also used to reduce the power consumption in many multimedia applications like image and video by properly managing pixel data.

Massoud Pedram [32] discussed the issue that Energy-efficient design requires reducing power dissipation in all parts of the system. Further in the study it's suggested that, also low bus encoding techniques play a major role in the architectural level power optimization of Embedded systems. Performance and power dissipation even restricted by the communication channels, dedicated for data transfer between the processor and memory units.

d) Application level power management:

Application level techniques for power savings include implementation of power aware algorithms, targeting applications such as multimedia etc. The best algorithms for deciding when to off or wake up a specific part of the system is normally decided by the application. This is because running applications will be having knowledge on the usage and activity patterns of various resources of the system. Always in a power managed system, applications only decide the best user's experience quality. In Embedded systems, these application level techniques tries to provide power optimization in such a way, that is transparent to the applications and users. This is because the applications are user-centric and will be having direct knowledge on how the user is utilizing the system to perform the desired.

Youngho Ahn et al. [27] proposed application specific power management method based on processor bandwidth control. Proposed governor is modifications in the DVFS, where CPU usage is customized by controlling the processor bandwidth. Experimental results on multimedia applications have shown that processor bandwidth control method could be very effective to optimize the power in Embedded systems while maintaining the quality of user experience.

Daniel Llamocca et al. [28] implemented 2D FIR (Finite Impulse Response) filter for image and video processing application on Graphic Processing Units (GPUs) and FPGA platforms. Compared energy performance and accuracy on both the platforms. They have observed that, based on energy consumption, FPGAs outperforms, GPUs for the chosen application even though FPGA is lower in performance wise compared to GPUs.

Yi-Chu Wang et al. [29] demonstrated the concept of mapping and optimizing applications to targeted platforms like SOCs for energy minimization and performance optimization. Presented the concept, with high accuracy face recognition application mapping to a smartphone platform. They explored the idea that by tuning the application algorithmic parameters and better utilization of available computational resources like

mobile CPU, GPU, improves both system performance and energy efficiency.

Lei Yang, Robert et al. [30] proposed an adaptive user-application aware, learning based, power reduction method for the Embedded CPU's. Observed that for many processor intensive multimedia applications, performance is extremely dependent upon the specific user and application, and not with CPU utilization. This observation provides a chance for reducing power consumption of processor's. The proposed method makes the processor to adopt continuously in voltage and frequency as per the user's performance requirements, this saves the power. Implemented proposed method on Linux platform and performance comparison has done with Linux default ondemand governor.

V. CONCLUSION

This paper focus on the Power management issue in Embedded systems. Discussed the need of power management in Embedded systems and reviewed some of the power management techniques which comes under, DVFS, Dynamic Power Management, architecture level, and application level. The future Embedded computing systems would be expecting with capabilities for high-speed audio, video processing and communication, which indeed require power efficiency. This certainly requires, the evaluation and necessity of Power management in Embedded systems in all the levels.

It is hoped that the discussion made in this paper might help the researchers in addressing the challenges of power management in designing Embedded systems, and suggested that, the combination of some techniques such as hybrid techniques or improvements to the existing, may improve the results further in terms of both performance and power optimization, even developing energy aware scheduling algorithms for the modern multi-core Embedded processors could also be a better option for the researchers.

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