PERFORMANCE ANALYSIS AND SIMULATION OF DIGITAL MODEMS

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Abstract : Digital modems like M-PSK (M-array phase shift keying)designs are used as a piece of some quick applications like satellite correspondence, as they are power efficient and have more information exchange limit contrast with the other schemes. This examination exhibits extensive scale composed circuit proposals for modulators and demodulators of QPSK (Quadrature phase shift keying), 8PSK and 16PSK structures. The propound modulators make an endeavor not to make use of any multiplier unlike ones in consistent modulators and designed based on the DDS (Direct Digital Synthesis) principle. In light of astute acknowledgment method, this examination put forward new demodulation computations for 8PSK and 16PSK structures. This study moreover demonstrates VLSI (Very Large Scale Integration) models for each of the stated algorithms. The designs are effectively developed at system level and lastly, the models are depicted in Verilog and examined on Xilinx platform.

IndexTerms **– QPSK, DDS, modulation, demodulation.**

I. INTRODUCTION

In recent times, the digital modulation schemes have gained a greater importance than the analogue ones due to many advantages like easier implementation, higher security and they provide better noise performance. Satellite communication system requires modulation techniques, which are power efficient, bandwidth efficient and have a sensible demodulator intricacy. Hence M-PSK modulation schemes are best suited since they satisfy all above criteria. In the literature, the QPSK architectures consists of multipliers which requires large area and it reduces the operation speed. The proposed modulators novelty is that instead of multipliers they are realized using concept of DDS. The proposed QPSK modulator and demodulator forms the elementary component in the architecture designs of 8PSK and 16PSK systems. In reference [1], the multiplier less architecture of QPSK modulator is designed using CORDIC module and shown that the modulators derived from CORDIC offers more hardware complexity but provides better phase resolution compared to modulators designed using look up table (LUT) approach. Hence to decrease the hardware complexity, this study presents all architectures form on LUT approach which be in need of lesser hardware and provides greater speed of operation. This paper also provides new demodulation algorithms found on [2] for 32-APSK system.

1.1 DDS Principle

DDS is having main advantage that, its output frequency, amplitude and phase can be expeditiously manipulated beneath the digital processor control. DDS applications are limited to the base station modulators because of high power consumption. In ref[3], the author discussed two approach for carrier generation using DDS. In first technique, the 256*8 ROM contains 256 amplitude sample values of sine wave carrier which are rounded off to a proximate decimal values in 2π rad. Fig 1 shows the generation of the carrier using 8-bit counter, ROM and digital to analog converter (DAC)[4]. The number of pretended components at the output of DAC is determined by the desire width and depth of ROM. In second technique of generating carrier, only π/2 rad of the carrier is stored in ROM (64*8). In this project, the MPSK modulators are fitted for both method of carrier generation.

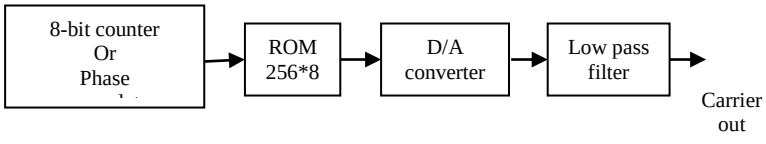

Fig 1.First technique of carrier generation using 2π rad of carrier in ROM

1.2 M-ary PSK modulation

The information to be transmitted in MPSK modulation is conveyed by one of the M-phase shifted versions of the carrier all having same frequency and amplitude. MPSK waveform can be represented in general form as follows

$$V_i(t)= A \cos(2\pi fct+\Phi_i) \quad \text{where } i=0,1,2\ldots\ldots..M-1. \qquad (1)$$

In common, 2^n=M symbol[1] where n is integer = 1,2,3….

In QPSK modulation, n value is 2, hence M=4 i.e., it encode two bits per symbol and there exists four symbols which have phase difference of 90°. In 8-PSK modulation, n=3 so M=8 i.e., 8 symbols exists, which have a phase difference of 45°. In 16-PSK modulation, n=4 so M=16 i.e., 16 symbols exists with phase difference of 22.5°. Hence bandwidth efficiency of 8PSK and16PSK are greater compared to QPSK.

II. DESIGN OF M-PSK MODEMS

2.1 QPSK modulator and demodulator

2.1.1 Modulator

The flow chart, fig.2 gives the QPSK modulator. Input to the modulator is serial bits. These bits are converted into symbols B[1:0] using S2P converter. A combinatory constellation mapper is used to map the input symbol to the needed constellation. The output of constellation mapper is used to generate the address input to the ROM. As the carrier phase of 360° represents the 256 samples, ROM address position d=32 gives us locality of carrier phase of 45°,correspondingly the address locations 96 to135°,160 to 225°and 224 indicates 315° carrier phase.

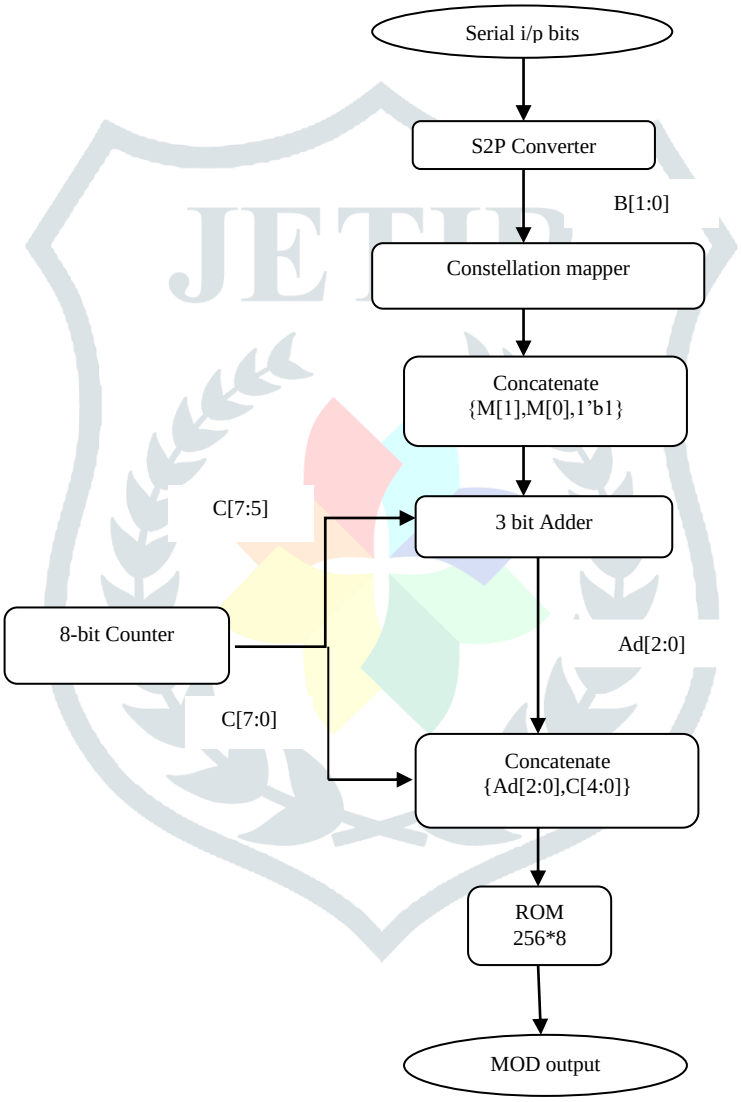

Fig 2.Flow chart for QPSK modulator

2.1.2 Demodulator

The flow chart for QPSK demodulator is shown in fig 3. The input to demodulator is the modulated output. 8-bit counter is used to access COS ROM and SIN ROM. These values are multiplied sample by sample with the input separately and the multiplied result is given to the adder whose another operand is the previous accumulated value which is represented as I_C and Q_C respectively. Looking at the MSB of I_C and Q_C decision is made whether the output bit is 0 or 1. The recuperated symbols are passed across P2S converter to redeem the original input bits.

$$B[1]=0 \text{ if } (I_c>0);\ 1 \text{ if } (I_c \leq 0). \quad (2)$$

$$B[0]=0 \text{ if } (Q_c>0);\ 1 \text{ if } (Q_c \leq 0). \quad (3)$$

2.2 Design of 8PSK modulator and demodulator

2.2.1 Modulator

The 8PSK modulator architecture is shown in fig.4. The incoming input bits are permuted into symbols B[2:0] using S2P converter. It is passed across constellation mapper, which maps the input symbols to chosen constellation diagram. The input address to the ROM is precipitated using 8-bit counter, two, 3 bit input adders and a multiplexer as shown in fig.4. Based on the address generated the modulated output is produced.

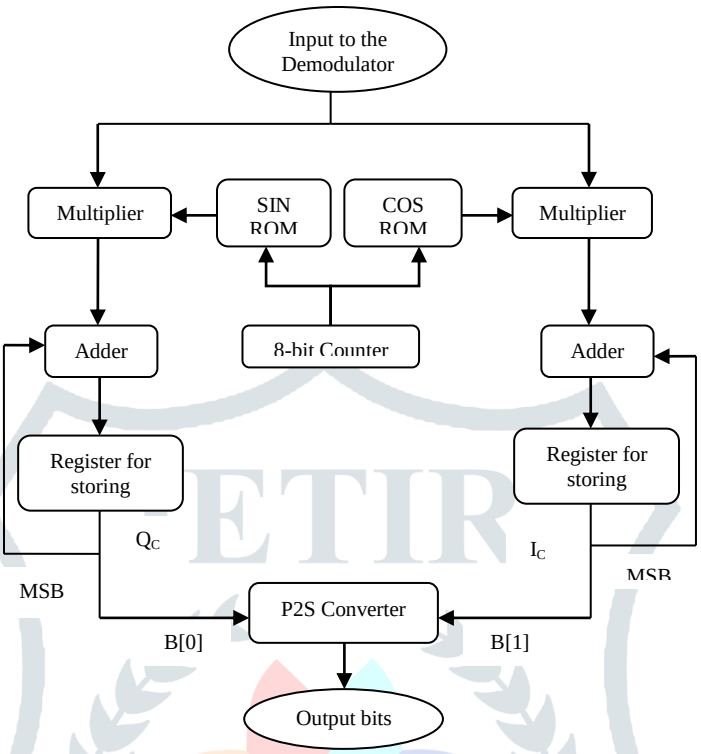

Fig 3.Flow chart for QPSK demodulator

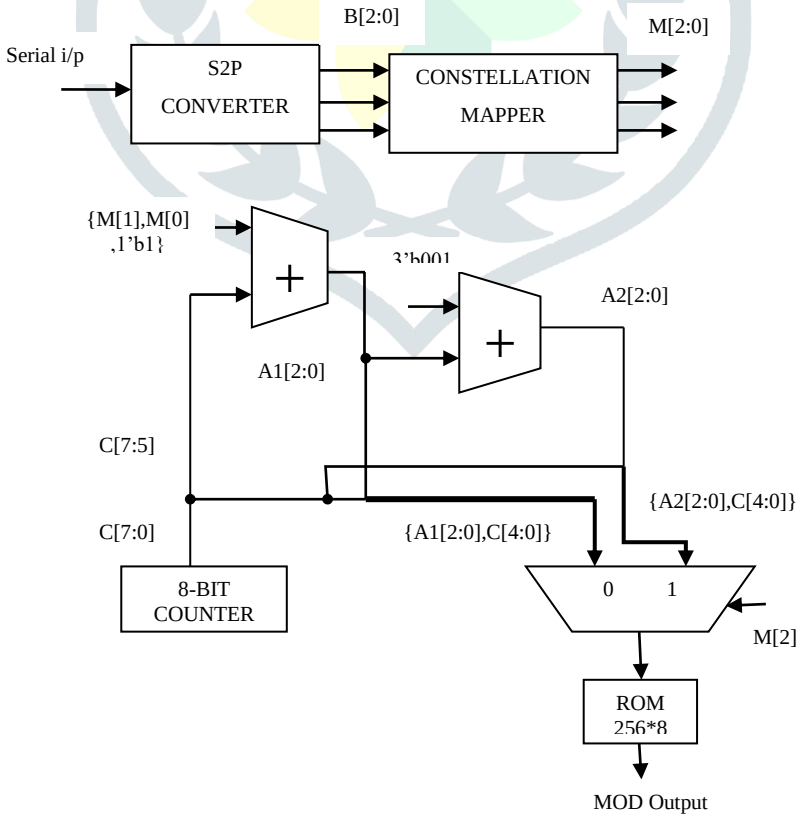

Fig 4.The 8-PSK modulator

2.2.2 Demodulator

The demodulator VLSI architecture for 8PSK is shown in fig.5. At the demodulator the received modulated signal is multiplied by COS ROM and SIN ROM separately and repercussion is accumulated using accumulator. Shifting, adding, subtraction and some logic operations are performed to reclaim the input bits.

The intermediate values can be found as:

$$K1=(2Ic)-Qc \quad (4)$$

$$K2=Ic+(2Qc) \quad (5)$$

$$K3=Ic-(2Qc) \quad (6)$$

$$K4=(2Ic)+Qc \quad (7)$$

To extract the input symbols:

$$B[2]=1 \text{ if} \begin{cases} K3 \leq 0 \text{ and } K4 > 0 \\ K3 > 0 \text{ and } K4 \leq 0 \end{cases} ; \text{ else } 0.$$

$$B[1]=1 \text{ if } (K1 \leq 0) ; \quad \text{else } 0.$$

$$B[0]=1 \text{ if } (K2 > 0) ; \quad \text{else } 0.$$

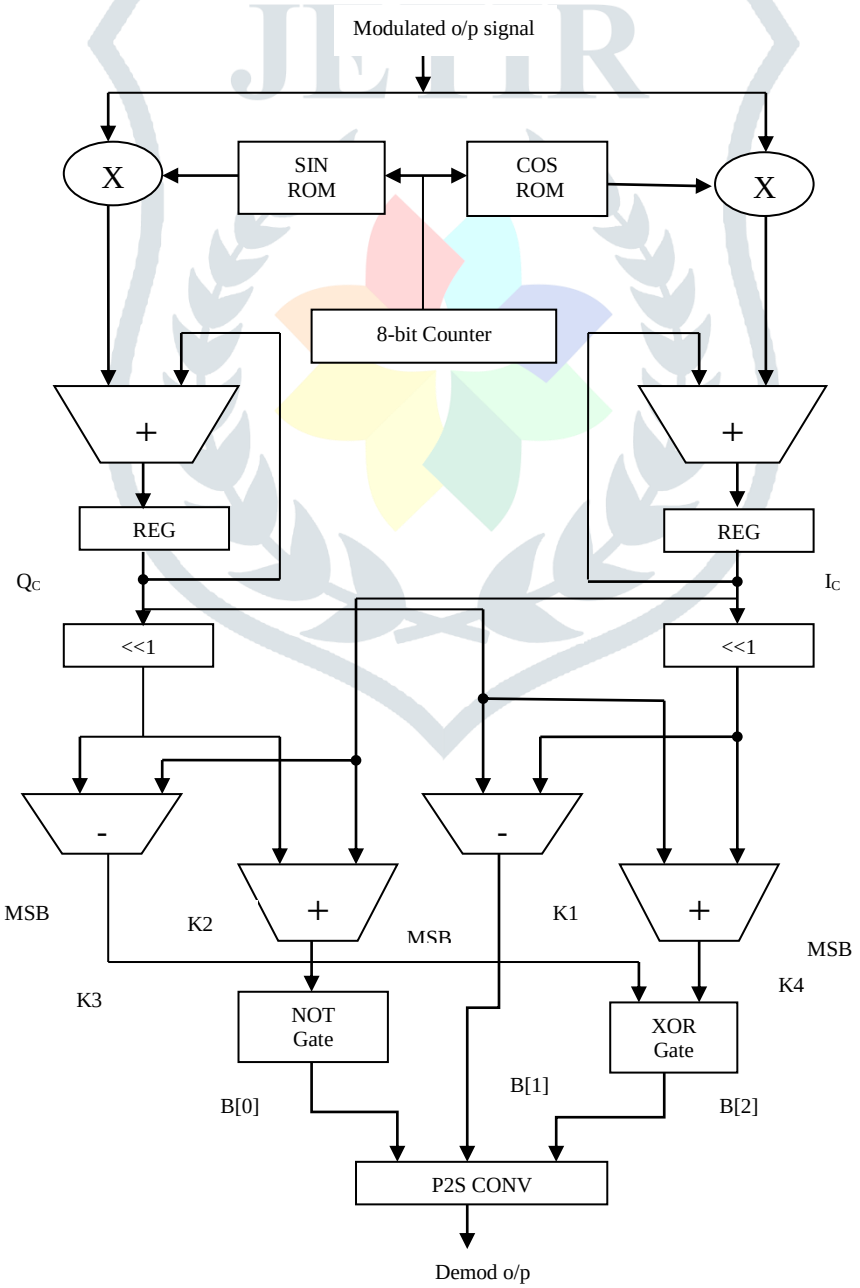

Fig 5.The 8-PSK demodulator

2.3 Design of 16PSK modulator and demodulator

2.3.1 Modulator

The flowchart fig.6 proffers the 16PSK modulator. The serial input bits are transmuted into symbols B[3:0] using S2P converter and move through constellation mapper to get M[3:0] for entailed constellation. The mapper output is passed through phase shift selection block to get logic for phase shifts of +/- 22.5° or 45° producing P[1:3]. This output is used as selection lines for multiplexers and bring out modulation output as shown in fig.6.

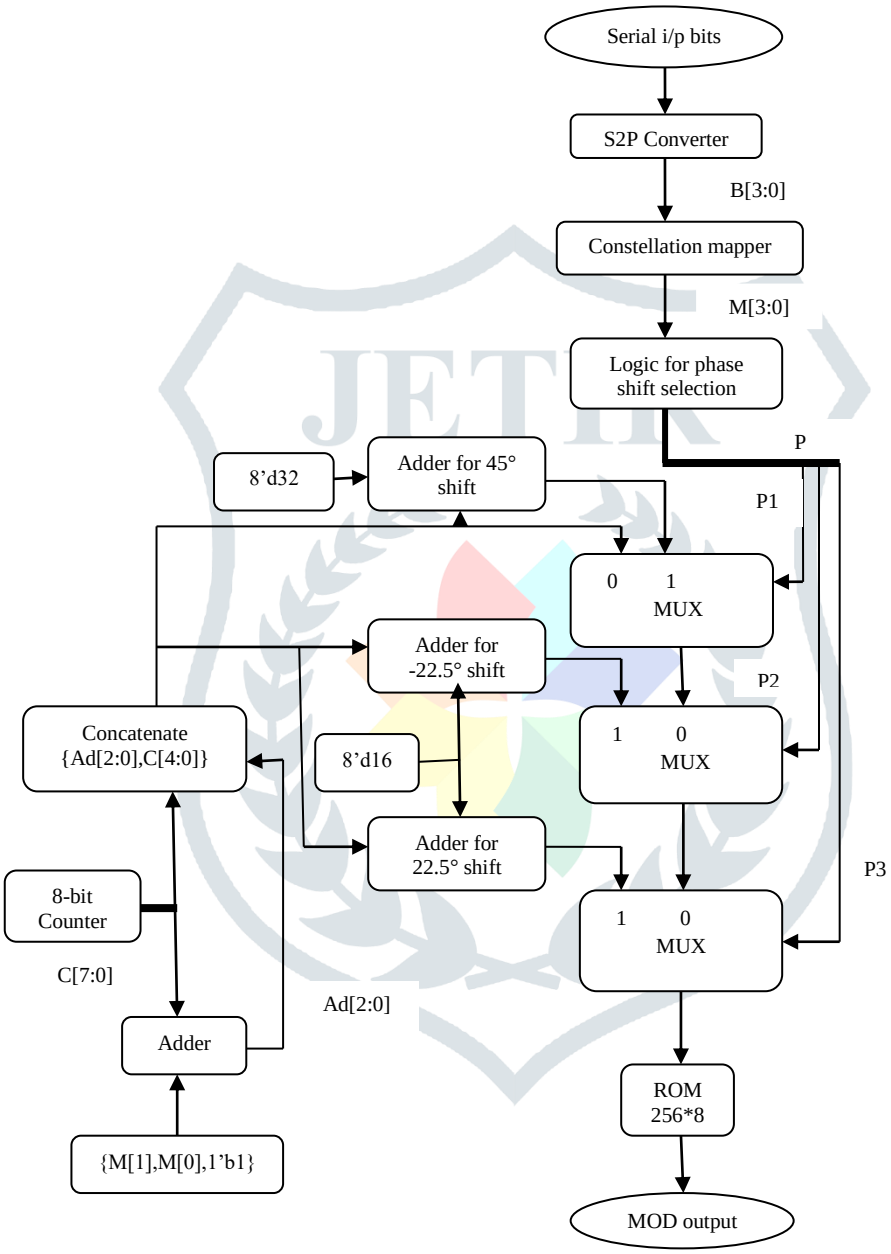

Fig 6.Flow chart for 16-PSK modulator

2.3.2 Demodulator

At the demodulator the received modulated output signal is multiplied by SIN ROM and COS ROM separately and cumulated in the respective registers. It is represented as Q_C and I_C respectively. Later I_C is passed over multiplication by tangent values block which is amendable to pipelining to get K[0:3](Eq.4 to Eq.7) output values. Then some operations are performed to reclaim the symbols B[0:3] and finally the symbols are pass across P2S converter to recuperate input bits as shown in fig 7.

Tangent values can be obtained as follows:

$$K0 = \tan(3\pi/16) * IC \qquad (4)$$

$$K1 = \tan(5\pi/16) * IC \quad (5)$$

$$K2 = \tan(\pi/16) * IC \quad (6)$$

$$K3 = \tan(7\pi/16) * IC \quad (7)$$

Multiplication of tangent values by I_C is accomplished by a sequence of left-right shift operations accompanied by addition/subtraction. Example, $\tan(2\pi/12) * I_C = I_C\ 0.5773$, can be estimated to $I_C\ 0.57714$ and it is obtained as $(I_C>>1)+ (I_C>>4)+ (I_C>>6)- (I_C>>10)$.

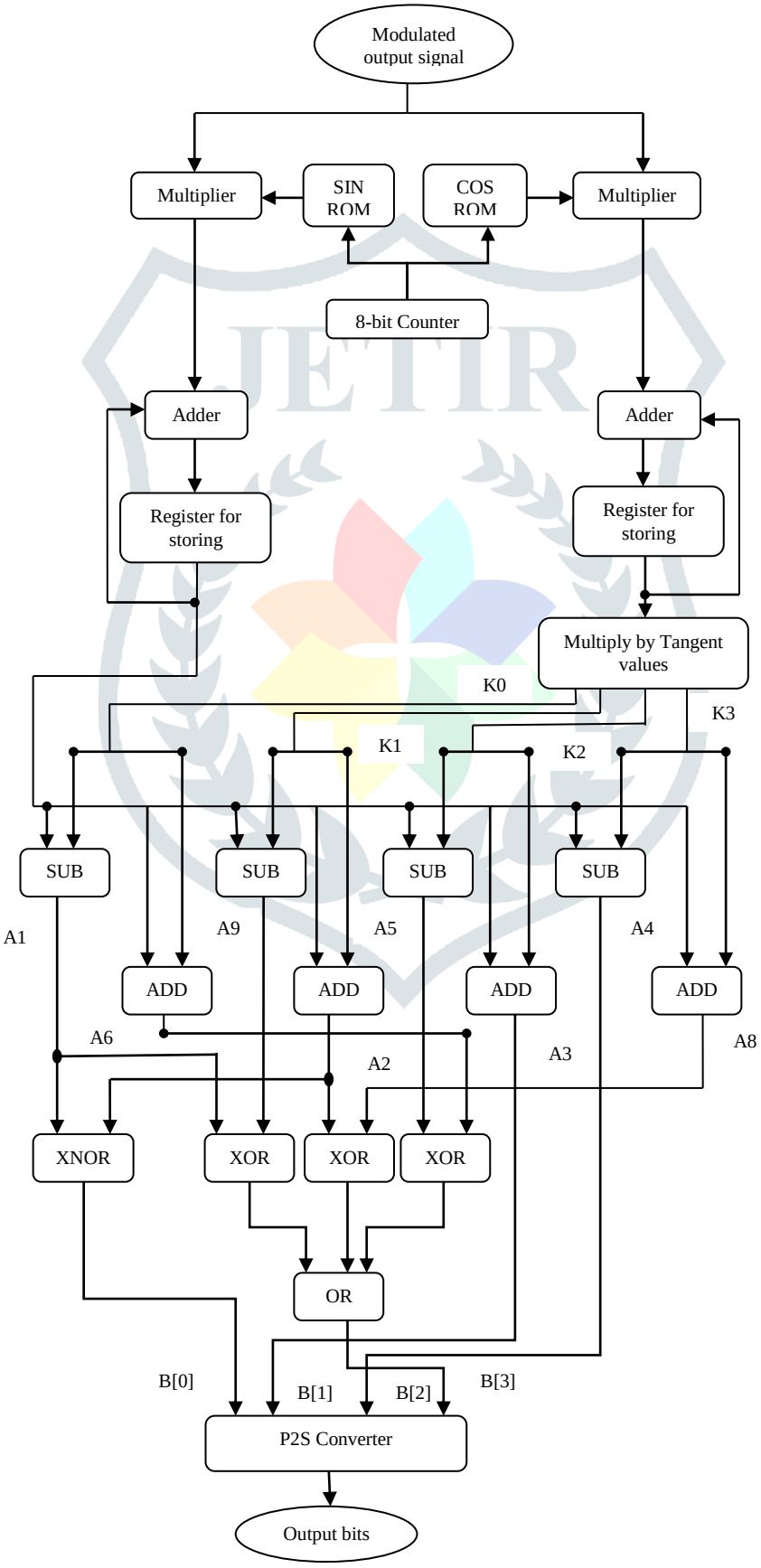

Fig 7.Flow chart for 16-PSK demodulator

III. SIMULATION RESULTS AND DISCUSSION

Xilinx ISE simulator and ModelSim software's are used to develop the M-PSK modulators and demodulators and results are as shown.

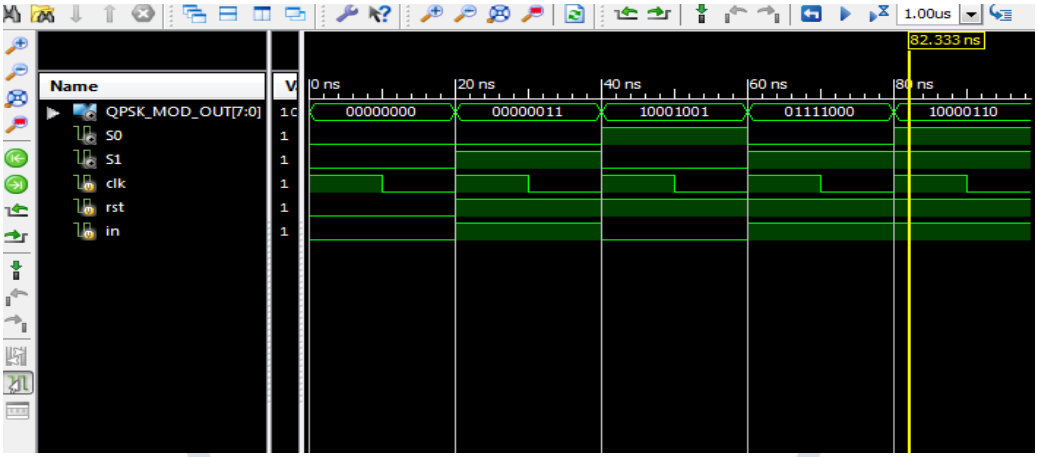

Fig 8.Simulation output waveform of QPSK modulator

The output waveform for QPSK modulator consists of din, clk, rst as input and PSK_16_MOD as output signal. When rst signal is low then whatever may be clk and input din, the output will be zero. When rst and clk signal is high then the input is modulated to produce modulation output as shown in fig.8.

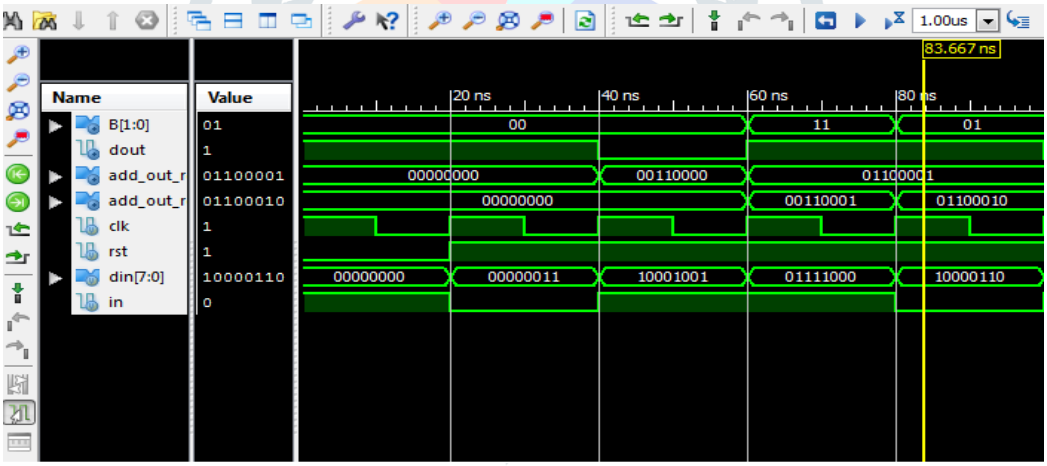

Fig 9.Simulation output waveform of QPSK demodulator

The output waveform for QPSK demodulator consists of din[7:0], clk, rst and dout signals. When rst signal is low then whatever may be clk and input din[7:0], the output will be zero. When rst and clk signal is high then the input symbol is demodulated to retrieve actual data bits as shown in fig.9.

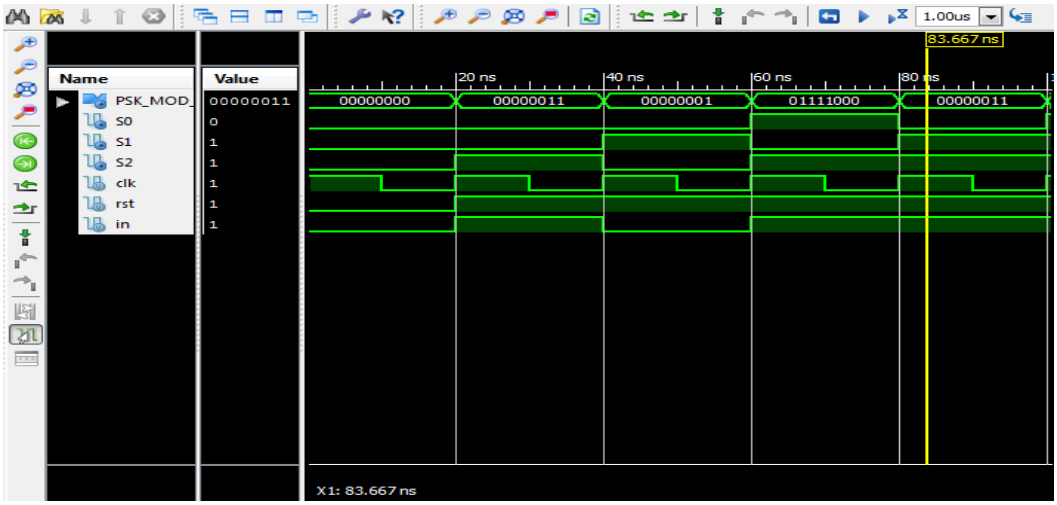

Fig 10.Simulation output of 8-PSK modulator

Similarly output waveforms of modulation and demodulation for 8PSK are shown in fig 10 and 11, for 16PSK in fig 12 and 13 respectively.

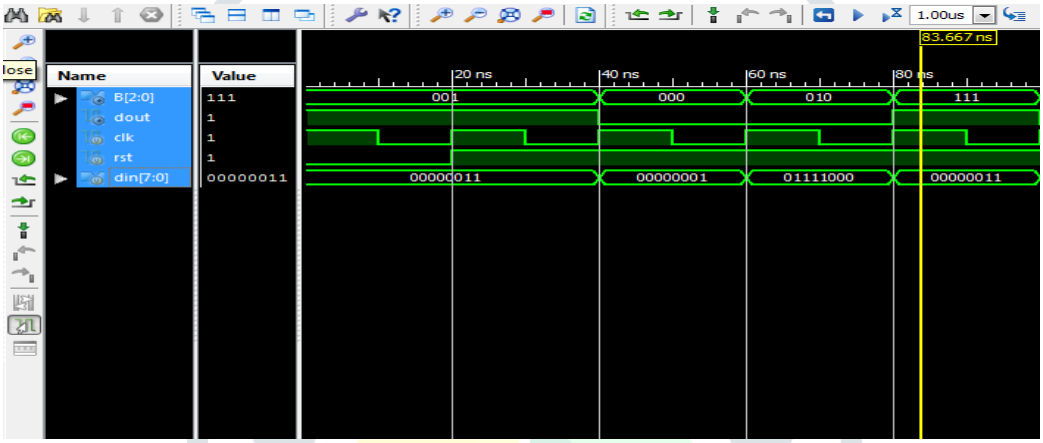

Fig 11.Simulation output of 8-PSK demodulator

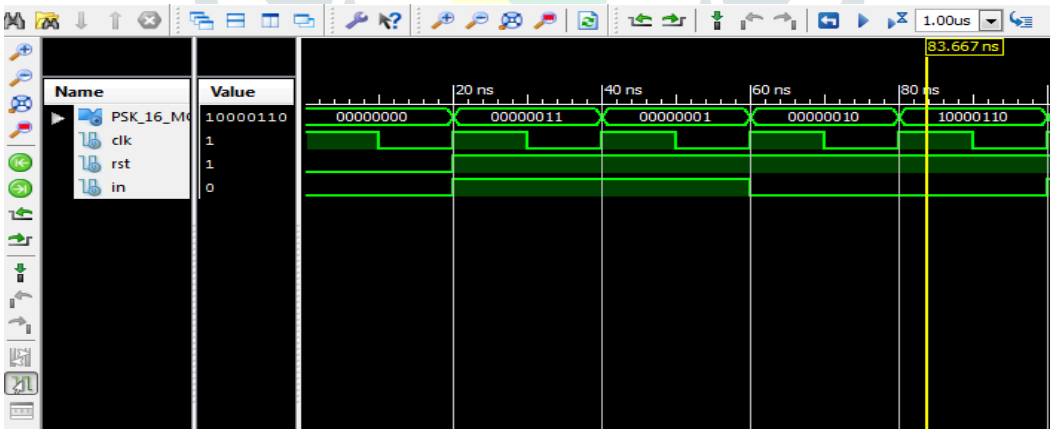

Fig 12.Simulation output waveform of 16-PSK modulator

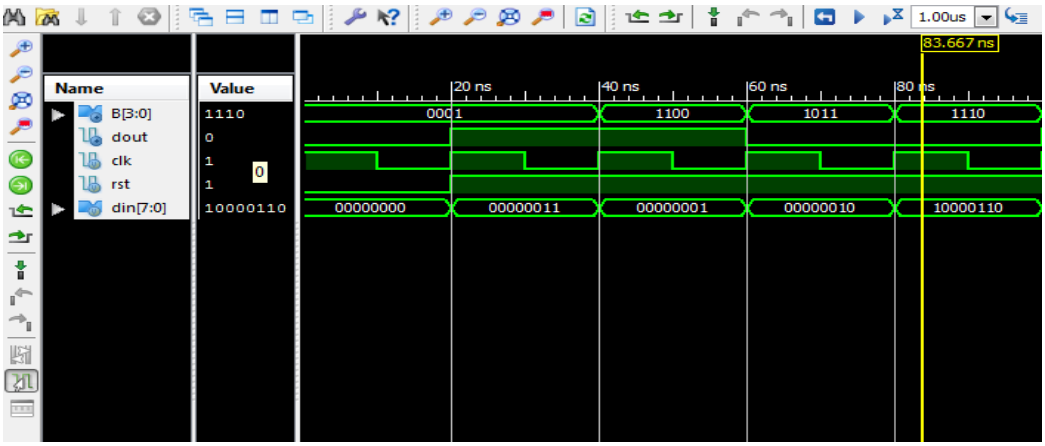

Fig 13.Simulation output waveform of 16-PSK demodulator

Comparison of proposed and conventional QPSK modem is given in table 1.

Table 1.Design summary comparison of conventional and proposed QPSK modem.

Logic Utilization	Prop QPSK mod	Conv QPSK mod	Prop QPSK demod	Conv QPSK demod
Number of Slice Registers used	10	95	26	233
Number of Slice LUTs used	13	157	26	277
Number of used LUT-FF pairs	10	164	24	304
Number of bonded IOBs used	11	14	23	15
Number of BUFG used	1	2	1	3

Table 2.Delay and Frequency of MPSK module

Parameters	MPSK module		
	QPSK demod	8-PSK demod	16-PSK demod
Delay(ns)	0.761	0.943	1.106
Frequency (MHz)	321.82	205.58	178.69

IV. CONCLUSION

The principle of DDS is used to design the VLSI architectures for QPSK, 8-PSK and 16-PSK modulators, which don't use any multipliers as the ones in the literature. Thus, the proposed modulators do not occupy large area and thus they provide high performance. The proposed MPSK demodulators are digitally implemented and are corrigible to pipelining. QPSK modulator with multiplier consumes 164 total number of LUT's and 95 slice registers, where as proposed QPSK modulator utilize only 10 number of LUT's and 10 slice registers as given in table 1, thereby reducing area and consumes less power and increase performance. All MPSK modems are coded in verilog. The modules have been synthesized and output waveforms are obtained using Xilinx ISE Simulator 14.6 and ModelSim10.4b. Further, these MPSK modems can be implemented on FPGA to get accurate synthesis results, which are suitable for satellite communication.

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