Design and Analysis of Low Power 10T SRAM Cell in 45nm CMOS Technology

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Abstract : **Memory components have an important role in the modern electronics industry. The performance of modern electronic devices somewhat depends on the efficiency of the memory cells used in it. Most of the research and development teams looking on to the SRAM memory cell due to its unique capability to retain the data. The entrenchment of VLSI technology gives a new face to the electronics industry. By the uses of VLSI technology the size of the electronic devices are reduced thereby, the area consumption reduces and increases the density. While going for the smaller technology sizes power consumption is an important factor for today's technology. The technology size reduction leads to leakage power, it is becoming an important contributing factor in total power dissipation of the circuit. In order to understand the power dissipation issues in the CMOS technology, briefly gone through the main power dissipation factors. In order to overcome the power dissipation and the delay, a new 10T static random access memory cell with NMOS sleep transistor and transmission gate in 45nm technology is proposed using cadence® virtuoso® EDA tool. The performance of the memory cell is evaluated by considering its data stability and power consumption and also the delay of the cell during read, write and hold modes of operation. In order to compare the performance of the system, some conventional SRAM cells are needed. So implemented the conventional 6T, 7T, 8T and 9T SRAM cells in 45nm technology and also implemented the conventional 10T SRAM cell in 65nm technology and calculated the read, write and hold stability. Also calculated the power consumption of each of these cells during the write, read and hold operations. While comparing the proposed 10T SRAM cell(45nm) with the conventional 10T SRAM cell (65nm), the proposed design has 61.92% reduction in write power and 72.53% reduction in read power and also 66.17% reduction in hold power and also the proposed design has 33.51% reduction in write delay and 38.82% reduction in read delay.**

Index Terms **- NMOS sleep transistor, Pass-transistor, SRAM, Transmission Gates (TG), DRC (Design Rule Check), LVS (layout versus Schematic), cadence.**

I. INTRODUCTION

The modern world mainly focused on portable electronic devices such as mobile phones, iPods, tablets, etc. These devices strictly depend on the battery because the demand for battery operated applications is increasing these days. For the daily long time usages, these devices should be designed to have battery backup. In order to increase the battery life of devices, we should concentrate on the delay and the power dissipation of the device. A major part of the battery is drained by the display and other peripheral components such as speakers. Memory components add up the power consumption of the devices. The memory present in the device carries a major part of the power consumption or dissipation in the system, mainly SRAM (Static random access memory) is ahead of this. In electronic devices, the SRAM plays an important role, because it is used as cache memory because a random-access device allows stored data to be accessed directly in any random order. Because of design limitations other data storage media such as hard disks, CDs, DVDs write and read data only in a predetermined order. Therefore, access time to data varies significantly depending on its physical location leads to increased delay and by increasing the access time the power consumption also increases.

The entrenchment of VLSI technology gives a new face to the modern electronics industry, which leads to the development of nanoscale devices. This technology helps to reduce the size of consumer electronic devices such as mobile phones, iPods, etc. So the demand for portable devices increases. In modern VLSI systems, the memory structures become an indivisible part. Semiconductor memory is presently not only just stand-alone memory chip but also an integral part of complex VLSI systems. The predominant criterion for optimization is often to squeeze in as much as memory as possible in the given area. This nanoscale trend led to portable computing has made power issues in memory.

Static Random-Access Memory (SRAM) is a semiconductor memory that uses cross-coupled inverter circuitry to store each bit. A typical SRAM cell uses two PMOS and two NMOS transistors forming a latch and two access transistors. Access transistors enable access to the cell during reading and write operations and provide cell isolation. During the un-accessed state, an SRAM cell is designed to provide nondestructive read access, write capability and data storage (or data retention) for as long as a cell is powered. In general, the cell design must be dependent on cell area, robustness, speed, leakage, and yield.

II. LITERATURE REVIEW

This chapter provides a condensed summary of the literature survey on key topics related to SRAM cell design. In conventional 6T SRAM [1] cell as shown in figure 1, there are two NMOS transistors N1 and N2 which acts as driver transistors and two PMOS transistors which act as load transistors. These four transistors combine and form cross-coupled inverters to store and force values continuously to each other.N3 and N4 act as pass transistors and called an access transistor which helps to write data from bit lines to node Q and QB. To write the data into the cell first enable write line (WL). Then for writing '1' pass '1' to the bit line (BL) and '0' to bit line bar (BLB). As WL enabled N3 and N4 are ON and pass data through them. This data is stored at node Q and QB as '1' and '0' respectively. After writing the data WL line is disabled. To write '0' we pass '0' to the bit line (BL) and '1' to bit line bar

(BLB).In hold mode, WL remains disabled and disconnects the cell from bit lines. To read the stored data from the cell, first pre-charge both the bit lines to '1' and then enable WL. If stored data is '1' then N1 is OFF and N2 is ON. Pre-charged BL line has no path to ground, so it remains as '1' at node Q and pre-charged BLB is discharged through N4 and N2 to ground, so it reads '0'from node QB. If stored data is '0' then N1 is ON and N2 is OFF. BL discharged through N3 and N1 to ground, so it. Reads '0' from node Q

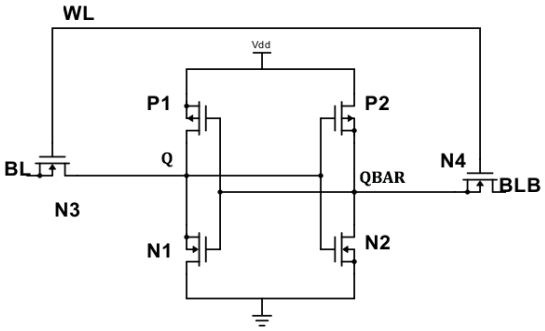

Fig. 1. Conventional 6T SRAM cell

CMOS technology provides better performance than MOS. While going to smaller technology sizes the power dissipation of the CMOS system increases. This power consumption reduces the battery backup of portable electronic devices. [2]Three equations provide a model of the power-performance trade-offs for complementary metal-oxide semiconductor logic circuits. These three equations are mainly used for the analysis of low power CMOS technology. These equations are very much helpful for logic designers, architects, and systems builders. In CMOS technology the power dissipation is an important factor. In CMOS designs the power dissipation is mainly due to the static and dynamic power leakages [3]. Static power implies the off-state leakage, current that leaks through transistors even when they are turned off. It is one of two principal sources of power dissipation in today's CMOS technologies. The other is dynamic power, which arises from the repeated switching of the hundreds of millions of gates in today's chips.

The power leakage and switching speed, these parameters of the transistors can be varied by adjusting the W/L ratios of the transistors [4]. CMOS technology uses both PMOS and NMOS transistors. Normally the size of the PMOS transistors is made 3 times than that of the NMOS transistors. Because in NMOS transistor the charge carriers are electrons and in PMOS transistor the charge carriers are holes. The mobility of the electron is 2.7 times more than the mobility of holes, so in order to balance the speed increases the size of the PMOS transistor. The performance of the cell also depends on the stability of the read, write and hold operations. So the study of failure occurs in the stability of these operations [5] are important. Before going to the conventional 10T SRAM cell [1], need to learn the design and three modes of operation of 6T SRAM cell [1], 7T SRAM cell [8], 8T SRAM cell [6] and 9T SRAM cell [7]. Then only got the reasons for power consumption and delay of the system. To make a new 10T SRAM cell with better performance parameters, it is important to know the sub-micron design issues [9]. For reducing the power dissipation of the system there are different types of low power design techniques are available. Stacking, sleep transistor approaches [10] are one among them. The sleep transistor approach is much better than the stacking technique.

III. CONVENTIONAL 10T SRAM CELL

The conventional 10T SRAM cell consists of 10 transistors. Where 6 transistors constitute a normal 6T SRAM cell, and 4 additional transistors are added to it for getting reliable performance. The normal 6T SRAM cell has two outputs, one of them is a complementary output QBAR. This QBAR is given to the gates of the inverter and the output of the inverter is given to TG (Transmission Gate). The existing 10T SRAM cell is implemented in 65nm technology. The conventional 10T SRAM in 65nm technology is shown in figure 2.

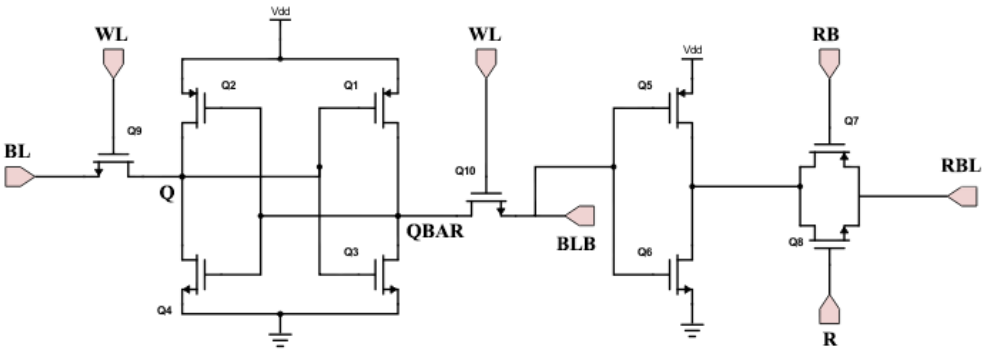

Fig. 2. Conventional 10T SRAM cell

Normally an SRAM cell has three modes of operation i.e., write, read and hold operations. In the write mode, the word line (WL) is set as high in the conventional 10T SRAM cell. By this the access transistors, Q9 and Q10 are turns on. Now the data is given to the BL and BLB input ports. The given data is available at Q and QBAR nodes.

The read operation of the conventional 10T SRAM cell is achieved by making the WL as '1', which turns on the pass transistors Q9 and Q10. Then the data at node Q and QBAR get at the output ports BL and BLB. Here in order to increase the stability of the output, the QBAR output is given as input to the inverter and the inverter output is given to a transmission gate to achieve maximum

voltage swing at the output. So the stable output is got at the read bit line port (RBL). But in hold operation, the word line is kept at logic '1' for a small period of time, in that time the data given through the BL and BLB ports. After given the data the WL is set as '0', it turns off the transistors Q9 and Q10. So the data is held in the cross-coupled inverter. The total power of the read, write and hold operation of the conventional 10T SRAM cell is given in the Table 1. From the table, it is understood that the read operation has higher power consumption than the other three modes of operations.

Table. 1. Total power of conventional 10T SRAM in read, write and hold operations

Technology size	Total write power	Total read power	Total hold power
65 nm	7.38 pW	10.23 pW	10.14 pW

The performance of the SRAM cell is evaluated not only by the total power but also the delay is an important parameter. So the delay of each operation is calculated from the transient response of the read, write and hold operations. The delay of hold operation is mostly the same as the write operation, so here consider only the delays to write and hold operations of the SRAM cell. The delay of conventional 10T SRAM in read and write operations are given in Table 2.

Table 2. Total delay of conventional 10T SRAM in read and write operations

Technology size	Total write delay	Total read delay
65 nm	57.40 pS	41.03 pS

IV. PROPOSED 10T SRAM CELL

Memory is said to be efficient, when it consumes less power and take a lesser delay for the read, write and hold operations. In order to reduce the power and delay of the conventional SRAM cell, here proposes a 10T SRAM cell with sleep transistors and transmission gates. The circuit implementation is shown in figure 3.

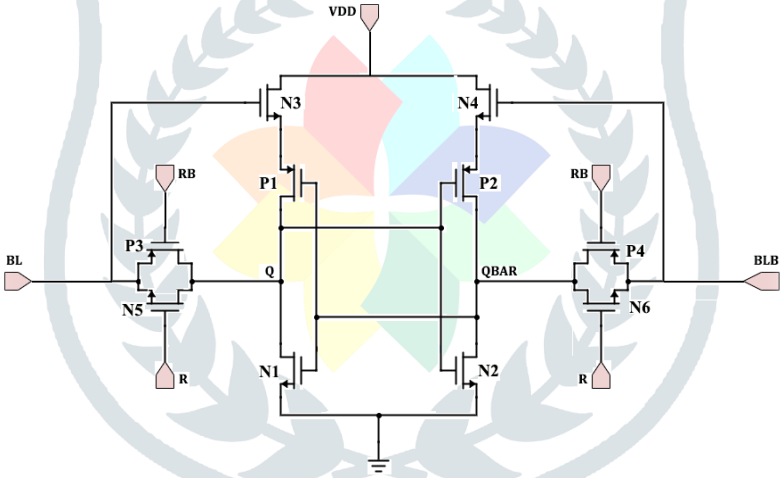

Fig. 3. 10T SRAM with transmission gates and NMOS sleep transistors

In figure.3, the P1, P2, N1 and N2 makes the cross-coupled inverter structure. Where the P3, N5 and P4, N6 makes two transmission gates. The input signals are given to these transmission gates. The N3, N4 is the high threshold sleep transistors attached to the pull-up network.

A. Write operation

The write operation of the proposed 10T SRAM is performed by setting the signals R='1' and RB='0'. This setup turns on the transistors P3, N5, P4 and N6. So the transmission gates are turned on and now the input bits are given to the BL and BLB ports. Assume if BL='1' and BLB='0', then the sleep transistor N3 turns on and the sleep transistor N4 turns off. By the activation of transmission gates, the values at BL and BLB ports are directly available at node Q and QBAR. So the logic '1' value at node Q, turns on the transistor N2 and turns off the transistor P2. Also, the logic '0' at node QBAR turns on the transistor P1 and turns off the transistor N1. So that the node Q is charged to Vdd, so node Q remains in logic '1' state and the QBAR node make a potential between the ground and remains in logic '0'. The circuit setup of the read operation of the proposed 10T SRAM cell is shown in figure 4.

B. Read Operation

For checking the read operation assume Q and QBAR as the inputs and BL and BLB are the output ports. For reading the data the signals SEL1, SEL2 are always in synchronizing with the input signals Q and QBAR and also made R='1' and RB='0'. Thereby the transmission gates are turned on and the value at node Q and QBAR are available at output ports BL and BLB.

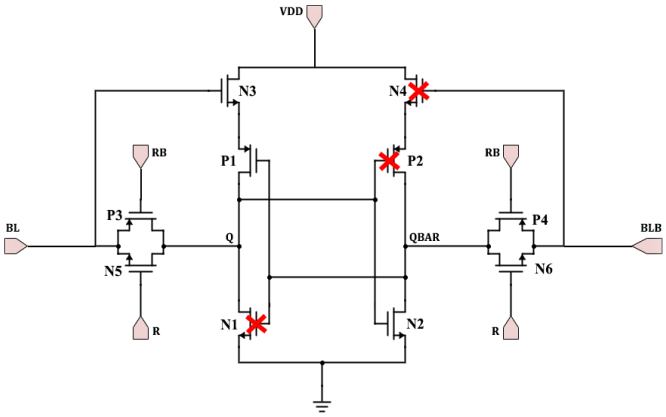

Fig. 4. 10T SRAM cell during write operation

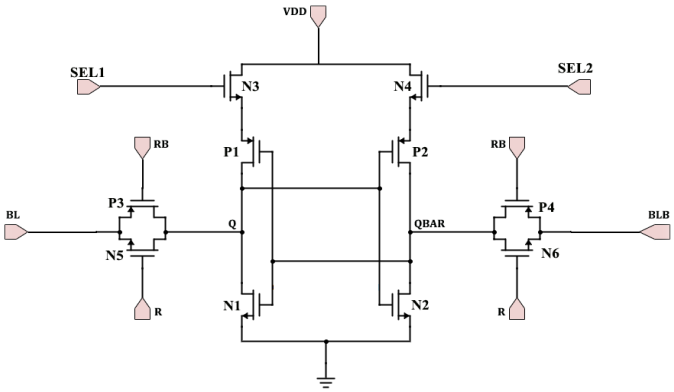

Fig. 5. 10T SRAM cell during read operation

C. Hold Operation

The circuit setup of hold operation is similar to the write operation. For performing the hold operation make a small change in the WL signal. For holding a data firstly write data into the cell. So WL is kept as logic '1' for a small period of time, after writing the data the WL is kept as logic '0'. Then the cross-coupled inverter is isolated from the inputs, so the data is held in the cell.

V. SIMULATION RESULTS

A. Write Operation

The schematic of the write circuitry of the proposed 10T SRAM cell is drawn in cadence virtuoso tool, it is shown in figure 6. Where the input port BL is given by Vpulse signal with period 10ns and its complementary input is given to BLB with the same period. 1V DC is given as Vdd. For the write operation, the R always needs to be in logic '1' and RB always needs to be in logic '0', so a 1v dc is given as R and 0v is given to RB.

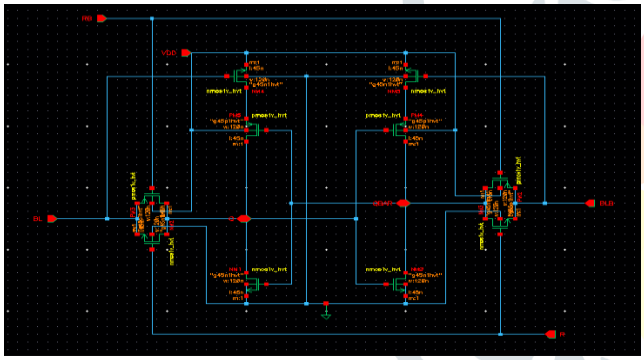

Fig.6. Schematic of write operation of proposed 10T SRAM

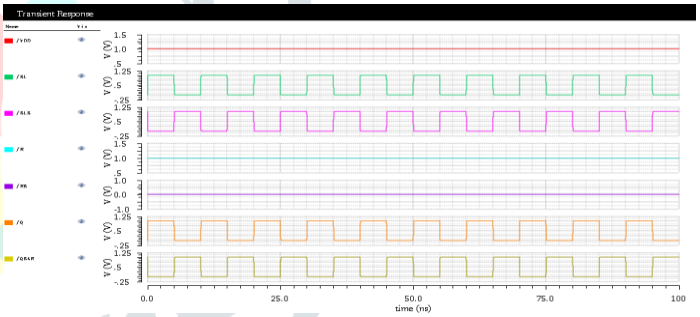

Fig.7. Transient response of the write operation of proposed 10T SRAM

The transient response of the write operation of proposed 10T SRAM cell in 45nm technology is given in figure 7. The delay of the write operation is getting from the transient response of the system shown in figure 7. The delay of proposed 10T SRAM cell is 38.16 pS and the total power consumption is 2.81 pW.

B. Read Operation

The schematic of the read circuitry of the proposed 10T SRAM cell is drawn in cadence virtuoso tool, it is shown in figure 8. The signal from BL, BLB to gates of the sleep transistors are replaced by two separate signals SEL1 and SEL2. The Q and QBAR nodes act as the inputs, so the input Vpulse with a period of 10ns and its complementary signal is given to these nodes respectively. A 1v dc is given as Vdd and R. RB is given with a 0v. The transient response of the read operation of the proposed 10T SRAM cell is shown in figure 9.

The delay of the proposed 10T SRAM cell read operation is given from the transient response as 25.10 pS and the total power consumption is 2.82 pW.

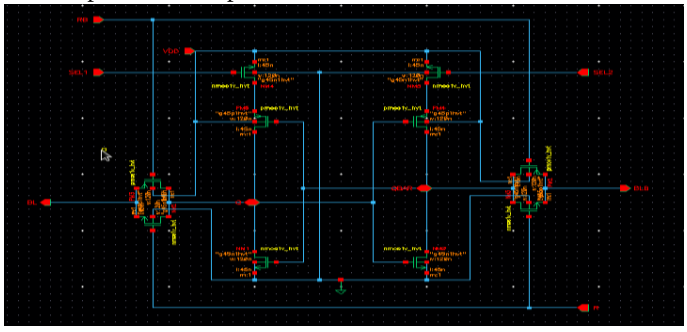

Fig.8. Schematic of read operation of proposed 10T SRAM

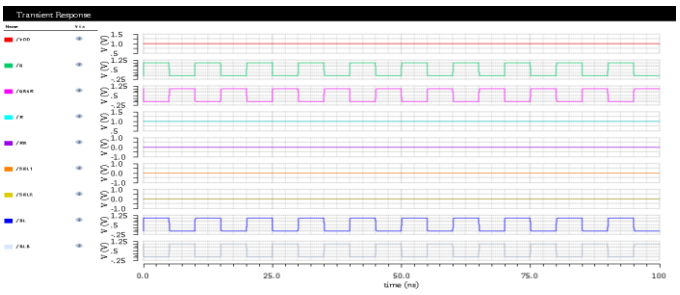

Fig.9. Transient response of the read operation of proposed 10T SRAM

C. Hold Operation

The schematic of the hold operation is same as that of the write operation, the only difference is that the R and RB signals are set as a logic '1' and logic '0' respectively for a small period of time. After writing the data these signals are reversed so the transmission gates are turned off, so the written data's are held in the memory cell. Vpulse signal with period 100ns and pulse width of 8ns is given as R and the RB has Vpulse signal with complementary values of R with the same period and pulse width. The transient response of the hold operation is shown in figure 10.

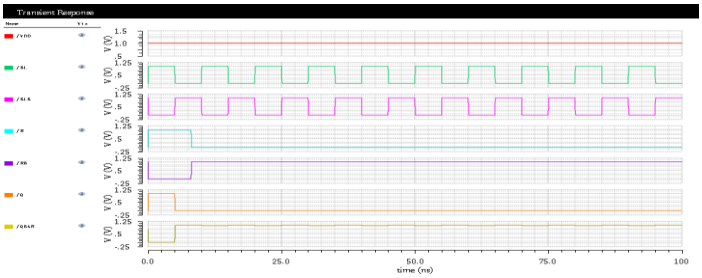

Fig.10. Transient response of the hold operation of proposed 10T SRAM

From figure 10 it is clear that after a small period of time the R and RB signals are made as low and high respectively. So that the transmission gates are turned off and the cross-coupled inverter circuit is completely isolated from the input. So the already written data are held in the memory cell. The total power consumption of the hold operation is 3.43 pW. The hold operation is the same as that of the write operation. So the delay of the hold operation is not considered for the performance evaluation of the SRAM cell.

D. Layout of the proposed 10T SRAM cell

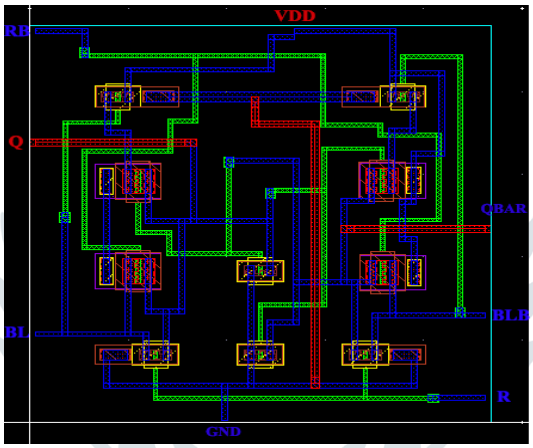

Fig. 11. Layout of the proposed 10T SRAM cell

The pre-layout simulations are completed and go for the post-layout simulation. The post layout simulation contains DRC (Design Rule Check) and LVS (Layout versus Schematic) check. These two checks are completed successfully without errors. The proposed layout consumes an area of 22.51µm^2.

VI. RESULT ANALYSIS

This section compares the power consumption and delay of conventional 6T, 7T, 8T, 9T, 10T and the proposed 10T SRAM cell.

A. Power Consumption

The power consumption of conventional 6T, 7T, 8T, 9T, 10T SRAM (65nm), 10T SRAM (45nm) and proposed 10T SRAM is tabulated in Table 3.

Table 3.comparison of total power of the modified 10T SRAM cell with the conventional basic SRAM cells

Design	Write power	Read power	Hold power
6T SRAM	8.09 pW	8.18 pW	8.09 pW
7T SRAM	7.94 pW	8.18 pW	8.00 pW
8T SRAM	26.38 µW	26.38µW	26.38µW
9T SRAM	15.51 pW	12.24pW	15.51pW
10T SRAM (65nm)	7.38 pW	10.23pW	10.14pW
10T SRAM (45nm)	12.04pW	12.12pW	12.04pW
Proposed 10T SRAM	**2.81 pW**	**2.82 pW**	**3.43 pW**

While comparing the proposed 10T SRAM cell with the conventional 10T SRAM cell (65nm), the proposed design has 61.92% reduction in write power and 72.53% reduction in read power and also 66.17% reduction in hold power.

B. Delay

The power consumption of conventional 6T, 7T, 8T, 9T, 10T SRAM (65nm), 10T SRAM (45nm) and proposed 10T SRAM is tabulated in Table 4.

Table 4. Comparison of delay of the modified 10T SRAM cell with the conventional basic SRAM cells

Design	Write delay	Read delay
6T SRAM	50.76 pS	25.72 pS
7T SRAM	4.95 nS	5.01 nS
8T SRAM	31.13 pS	15.55 pS
9T SRAM	5.00 nS	50 pS
10T SRAM (65nm)	57.4 pS	41.03 pS
10T SRAM (45nm)	53.76 pS	37.93 pS
Proposed 10T SRAM	**38.16 pS**	**25.10 pS**

While comparing the proposed 10T SRAM cell with the conventional 10T SRAM cell (65nm), the proposed design has 33.51% reduction in write delay and 38.82% reduction in read delay.

VII. CONCLUSION

This project proposes a new 10T SRAM cell using transmission gates and NMOS sleep transistors in 45nm CMOS technology. This proposed system achieves much lesser power dissipation and delay than the conventional 10T SRAM cell. The transmission gates used in the read, write ports of the proposed 10T SRAM cell give much more stability and voltage swing at the outputs. The NMOS sleep transistors connected to the pull-up network helps to reduce the power consumption and also the delay of the read, write and hold operations. While comparing the proposed 10T SRAM cell with the conventional 10T SRAM cell (65nm), the proposed design has 61.92% reduction in write power and 72.53% reduction in reading power and also 66.17% reduction in hold power. While comparing the proposed 10T SRAM cell with the conventional 10T SRAM cell (65nm), the proposed design has 33.51% reduction in write delay and 38.82% reduction in reading delay. The conventional 10T SRAM cell is implemented in 65nm technology, so in order to optimize the area, this proposed system is implemented in 45nm technology. The layout of the proposed system is drawn and successfully completed the DRC and LVS checks without errors and the proposed system use an area of 22.51µm2.

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