A Review on Various Low Power and High Performance Comparators

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Abstract As we know that using of electronics devices as well as communication devices is increasing as time is increasing in our daily life. The main reason behind the increasing of demand of electronics devices is that these devices are portable in nature. Everyone buy a electronic gadget by thinking of one factor in the mind which is mainly power consumption of the electronic devices. There is also need or requirement of every person to scale down the power consumption of different devices present in electronics and communication engineering, along with power generation is also a big task. The device which is mainly used to reduce the power consumption of various devices is through the presence of comparator. As we know in present time every analog device is converted into digital device. So we can do this with the help of comparator. So comparator is a device which convert analog signal into digital signal. In my paper, I present a review on the various low power and high performance comparator as well as power dissipation of the different comparator under different temperature on 90nm, 180nm and 250 nm CMOS technology. The main parameter which we considered in the paper are power dissipation of different types of comparator such as conventional single tail comparator, Double tail comparator, modified double tail comparator and comparator with cross couple inverter.

Introduction In order to provide the introduction of the comparator, we can say that there is requirement of such kind of high speed devices which operates faster. For this purpose, there is requirement in order to convert the analog signal to digital signal which can speed up the working of the device as well as increases the accuracy of the device. For achieve the purpose, we required the comparator which convert the analog signal to digital signal. That's why operational amplifier is mostly used in almost all the electronics circuit. Comparator is also known as operational amplifier.[1]Thus open loop configuration of the operational amplifier is known as comparator. Comparator as the name implies compares the two signals which apply at the input terminal .The same input signal is then converted into digital signal. The digital signal is a transform signal of the analog signal. The input signal which we apply at the input terminal of the comparator is mainly two current or voltage correspondence output signal is produced. Sometimes the comparator is also called or known as 1-bit analog to digital convertor. For the design of analog to digital convertor which is of high speed can be achieved with the help of dynamic comparator .There are various advantages of the analog to digital convertor such as high speed, least power requirement and requirement of smaller chip area. In order to reduce the power dissipation we basically used the dynamic latch comparator. If the comparator does not have any feedback, then it is called operational amplifier

Comparator: It is a device which works by comparing two signals i.e. two voltages or two current signals. It provides the output by indication which signal is larger. The input signal of the comparator which is voltage or current signal and in output we get digital signal. Comparator takes two analog input terminals as shown in figure

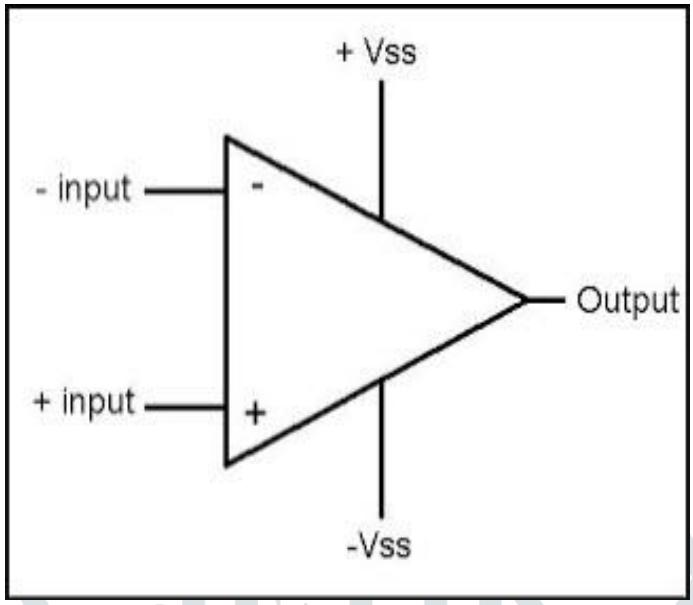

Figure: Schematic of Comparator

In the above figure, it is shown that, it has two analog input terminals i.e. V^+ and V^- along with one output binary digital signal i.e. V_O

If $V^+ > V^-$ then $V_{OUT} = V_S+$

If $V^- > V^+$ then $V_{OUT} = V_S-$

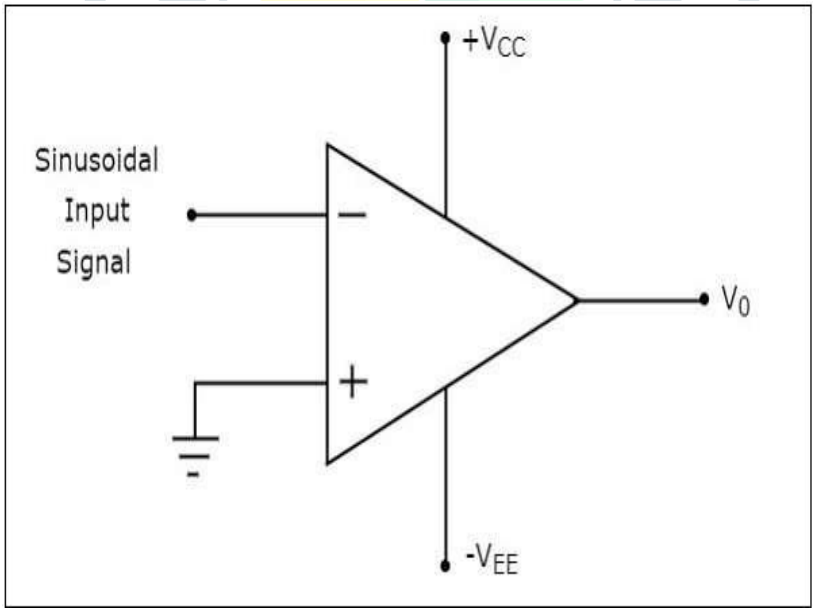

Figure: operational amplified based inverting comparator

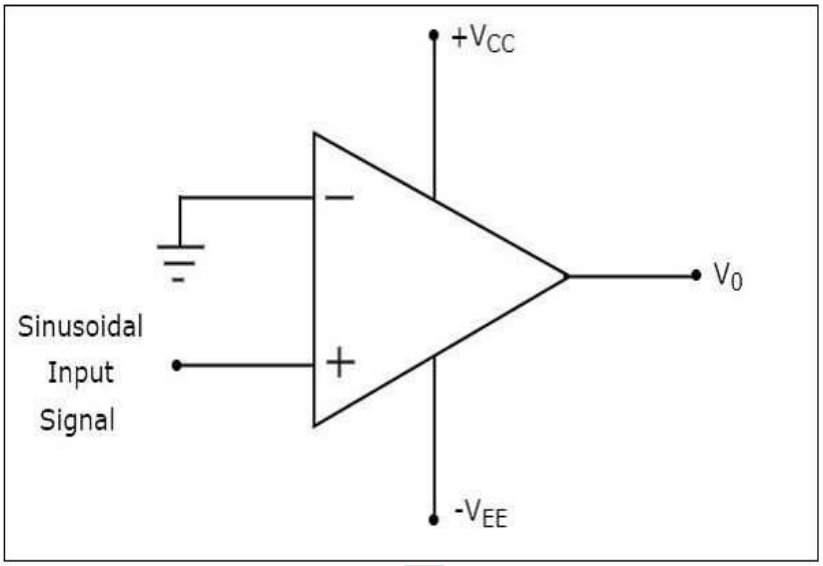

Figure: operational amplifier based non inverting comparator

LITERATURE SURVEY

1 Deepak Parashar et.al [2] In his paper presents the schematic diagram of the complementary metal oxide semiconductor comparator. He also uses the CMOS comparator with very high speed also with low power dissipation. After the analysis DEEPAK PARASHAR gives the design of the CMOS comparator under 180 nm TSMC technologies. He stimulated the design diagram in the cadence environment. In the conclusion he concluded that the circuit diagram work with very high clock frequency i.e.is 100MHZ.he also conclude the following result in his paper as following

A) Low offset voltage=280.7mw
B) Low power dissipation = 0.37mw
C) Noise=6.21 (in micro volt)

2 Pardeep Sharma and Rajesh Mehra et.al [3] provide the design and analysis the properties of 1-Bit comparator. Both of them used XNOR gate and AND gate in order to implement the design of the comparator. They used XNOR gate for the purpose of static energy recovery. As we know that comparator comprises of PMOS and NMOS transistor, So they used 3 PMOS and 7 NMOS transistor. The designing of the comparator took place in logic – editor and the same design is simulated under 45 nm technology. They basically used two designed technique in their paper which are fully automatic layout and semi custom layout

3 Mr.Abhishek Rai et.al [4] made the design of the comparator with the help of 180 nm CMOS technology. He used bias voltage of value 1.8 V and bias current 1 to 2 micro ampere. He designed and stimulated the comparator with the help of Tanner EDA tool. He also compared the difference between proposed comparator with existing double tail comparator. He also compared and concluded the performance of the comparator as following:

a) Average power consumption: 4.591 micro watts of CMOS comparator, without hysteresis.
b) Average power consumption: 6.46 micro watts with hysteresis.

All these values is for the double tail comparator. He also calculated the propagation delay which can be written as $T_{DD,}$ in his paper as 141 nano second,190 nano second respectively. In the last he concludes that

comparator with hysteresis takes almost 1/3 of the total power takes by the double tail comparator. He also said that double tail comparator perform and works faster as compared to the comparator with hysteresis.

4 Gopal Raut et.al [5] presents the designing of the flash ADC which is of 4 bit, with the help of the encode named as 'Transmission Gate based Encoder'. He completed the design of encoder in two stages. This encoder translates thermometer code into intermediate grey code. He further converts the grey code to binary code in order to reduce the effect bubble error. He designed the encoder under 180 nm CMOS technology and stimulation is completed under SPICE. He also said that that comparator worked in three phase as following:

a) Pre amplifier stage
b) Dynamic latch
c) Buffer stage

5 Aduti Kar et.al [6] designed 43 microwatt flash ADC along with TMCC and bit referenced encoder. He stimulated his design under 180 nm CMOS technology. By the modification of the conventional comparator and introduced the TMCC concept i.e. Threshold Modified Comparator Circuit. He completed his simulation under 180 nm technologies with the help of CADANCE software.

6 A.Nadhani et.al [7] presented the performance of the flash ADC with the help of designing of different comparator under 180 nm technologies. He designed the architectures of different comparator. He designed the different circuit diagram of comparator by using GPDK 180 nm technology under CADANCE Virtuoso tool and his simulation is completed with the help of SPECTRE simulator. He used three different comparators in flash ADC as following:

a) Open Loop Comparator

b) Latched Comparator

c) Differential Comparator

In the last he also gave the comparison in various parameters such as conversion time (in nano second),ENOB, SNR(in db),SFDR(in db)

7 Anjult.et.al [8] gives the idea with two bit magnitude comparator under different logic. He completed his stimulation under 90 nm technologies under Tanner EDA tool. He used different styles of logics i.e. CMOS logic style, transmission gate logic style; PTL (Pass Transistor Logic).He obtained the final result in terms of power consumption etc. In last he concluded that NMOS logic provides less delay when compared with different logic styles.

8 Miss Jasbir Kaur et.al [9] designed and presented the area efficient four bit flash ADC with the help of using multiplexer. She designed ADC under GPDK 180 nm technology. In order to make proposed flash ADC, she told, it used less comparator when compared with the making of conventional flash ADC. She stimulated her design with the help of CADANCE analog tool. At last she concluded the result of proposed ADC with the conventional flash ADC and said that power as well as area which is in mainly terms of using transistor to make are reduced. She concluded that the flash ADC with multiplexer takes 6.40 micro watts. On the other hand conventional flash ADC takes 11.23 micro watts. She also said in last that flash ADC with multiplexer used 122 transistors, on the other hand Conventional ADC took 304 number of transistor.

9 S.S Khot et.al [10] also implemented and design 6 bit flash ADC under 250 nm CMOS technology with the help of TIQ comparator. He also did the comparison of 6 bit flash ADC along with TIQ comparator with two different voltages i.e. 2.5 V and 3.3 V. The design of ADC is carried out by flat tree encoder with TIQ comparator. The stimulation is completed ob Tanner EDA Tool with the help of using 250 nm CMOS technology. In the making of his design ,the total number of transistor counted are 1928 in number with maximum speed is 500 on 2.5 volt and speed(MSPS) is 565 on 3.3 V

10 S.Guha et.al [11] made his designed in his paper as a SOC based 8 bit flash ADC under CMOS technology of 45 nm. He designed ADC made by using 255 comparators along with one thermometer to Binary Encoder. Implementation of ADC is completed by using Tanner-Spice(S Edit) and layout is completed in Tanner Spice (L Edit).His result shows that peak power of flash ADC is 41.78 micro watts and average consumed power is 6.45 micro watts. His implemented design also works for low voltage i.e. $0.6BV_{DD}$.

11 Ujjayani Debunath, Shobha Sharma, Amrita Dev and Preeti Singh et.al all of them studied the different types of the comparators. These different comparators are then simulated with the help of different techniques as well as technologies. They discussed different comparators such as comparators which are based on pre amplifier based stage and comparators based on latch circuit design. Their main objective for studied different comparators is to get analysis on the power consumption which is considered as important parameter of the comparator. They studied double stage comparator in two different stages such as pre amplifier stage as well as latching stage. They studied double trail comparator which is made up of two type of PMOS and NMOS transistor. After studying the behavior of the comparators, they simulated their design under 90nm, 180nm, and 130nm and 250nm CMOS technology.

12 Dharmendra B.Mavani et.al [12] gives the introduction of the comparator which used in flash A to D convertor. He presented mainly two comparators in his paper as following:

a) TIQ comparator i.e. Threshold Inverter Quantization Comparator.
b) Two stage open loop comparator

He stimulates both the above mentioned comparator circuit under 50 nm CMOS technology. He completed his stimulation in two phases as pre and post simulation. He completed pre stimulation with the help of L-T spice and post stimulation is completed with the help of Micro wind 3.1.For the purpose of simplicity of designing of circuit diagram, he extended the architecture of the two mentioned comparator from medium to high resolution applications.

Research Methodology

In our research methodology, as we know that we use Tanner EDA tool for the study on power dissipation of different types of comparators along with their various temperature ranges in 90nm,180nm and 250nm CMOS technology. Therefore we design various comparators such as conventional single tail comparator, double tail comparator, modified double tail comparator and comparator with cross couple inverter. All the four above mentioned comparators are designed in different 90nm, 180nm and 250 nm in complementary metal oxide semiconductor technology in order to study their power dissipation along with different temperature ranges. For this purpose we use 3 different Tanner tools such as following:

1 **S-EDIT:** It is basically a schematic tool.

2 **T-SPICE:** This tool is mainly used for the simulation of the design.

3 **L-EDIT:** This tool provide the physical layout of the proposed design.

In order to compare the power dissipation of such different comparators. Firstly we draw the schematic diagram of such comparators by using PMOS and NMOS. After we run these schematic layouts by browsing their respective models and library files and note down their power dissipation of comparators and compare them with different temperature ranges.

CONCLUSION

After surveying of various literature review of different comparators we conclude in the last that power dissipation of different types of comparators such as conventional single tail comparator, double tail comparator, modified double tail comparator and comparators with cross couple inverter will be studied on different types of complementary metal oxide semiconductor technology such as 90nm, 180nm and 250nm and compare them in terms of power dissipation in different temperature ranges.

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