21 LEVEL STAIRCASE SINE WAVE INVERTER WITH REDUCED SWITCHES AND THD

[1] A. Annai Theresa, [2] Sinu Cleetus, [3] A. Abinesh, [4] C.Thamizharasan, [5] S. Shanmuganatham.

[1] Assistant Professor, [2,3,4,5] UG Students
[1] Department of Electrical and Electronics Engineering,
[1] St. Anne's College of Engineering and Technology, Cuddalore, India.

Abstract: Several industrial applications require high power inverter with sinusoidal waveforms with minimum distortion. For medium and high power applications, it is difficult to attain depending on a single switch. Therefore, the concept of multilevel inverters where introduced in 1974. At present situation multilevel inverter is becoming more popular due to its staircase output whose characteristics is closer to the characteristics of sinusoidal waveform. But generally it has some disadvantages like, requirement of increased number of switches and complex pulse width modulation methods to reduce harmonics. The cascaded H-bridge multilevel inverter requires least number of components to achieve various voltage level by which the quality output is obtained. However as the number of voltage levels m grows, the number of active switches increases according to 2× (m-1) for the cascaded H Bridge. Here, the novel multilevel inverter topology with reduced number of power switches is proposed and the switching frequency is getting reduced. The power quality of the proposed system is improved by using selective harmonic elimination (SHE) method. The whole system is numerically reformed developing MATLAB/SIMULINK and the simulation results are presented.

Index Terms **- Multilevel inverter (MLIs), PWM techniques and Total Harmonic Distortion (THD), Cascaded H-bridge, SHE.**

I. INTRODUCTION

Generally, the voltage source inverters generate an output voltage with a two level, so they are also called the two-level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require a high switching frequency along with various PWM techniques. For the high power and medium power applications, these two-level inverters have some disadvantages. The two level inverter is operating at high frequency therefore this causes the switching losses, distorted output voltage and current and very large Total harmonic distortion of the output voltage and current [1]. Hence multi-level inverters are used to mitigate the overall THD. In the multilevel inverter increasing the number of voltage levels without requiring higher ratings on individual devices can increase the power rating. And if the number of voltage level increases, the harmonic content of the output voltage decreases. The multilevel inverter can be classified as flying capacitor, Cascaded H-Bridge and diode clamped multilevel inverters. Out of these technologies Cascaded H-Bridge multilevel inverter is one of the well-known, most advantageous, much simpler and basic method of multilevel inverter.

The multilevel inverter can be classified as flying capacitor, Cascaded H-Bridge and diode clamped multilevel inverters. Out of these technologies Cascaded H-Bridge multilevel inverter is one of the well-known, most advantageous, much simpler and basic method of multilevel inverter [2].

Multilevel inverter provides a suitable solution for medium and high power systems to synthesize an output voltage which allows a reduction of harmonic content in voltage and current waveforms.

In the cascaded multilevel inverter, H-bridge inverter is used. Number of H bridges are connected in series, each H-bridge having a separate DC source. The capacitor or diode is not required for clamping purpose. So these are the advantages of cascade multilevel inverter over diode clamped and flying capacitor multilevel inverter. And also the output waveform will be sinusoidal in nature if number of level is increased and even we don't filter it [3].

In this paper, Selective Harmonic Elimination (SHE) control strategy is used, and the 21- level cascaded multilevel inverter simulation has been done in MATLAB software.

II. MULTILEVEL INVERTER

The multilevel inverter is a type of inverter circuit which is used to increase the efficiency of the inverter operation and reduce the THD level in the operation of inverter in order to reduce the losses. Various pulse width modulation techniques are used to get the desired output.

2.1 Cascaded H-bridge topology

The term H Bridge is derived from the typical graphical representation of a circuit. An H bridge is built with four switches (solid-state or mechanical). One of the basic and well known topologies among all multilevel inverter is cascaded H-bridge multilevel inverter. It can be used for both single and three phase conversion. In Cascaded H-Bridge multilevel inverter, Number of H-Bridges are connected in series. Each H-Bridge has separate DC source which is to be obtained from any natural sources, ultra-capacitors, fuel cells or batteries to produce inverted ac output [4].

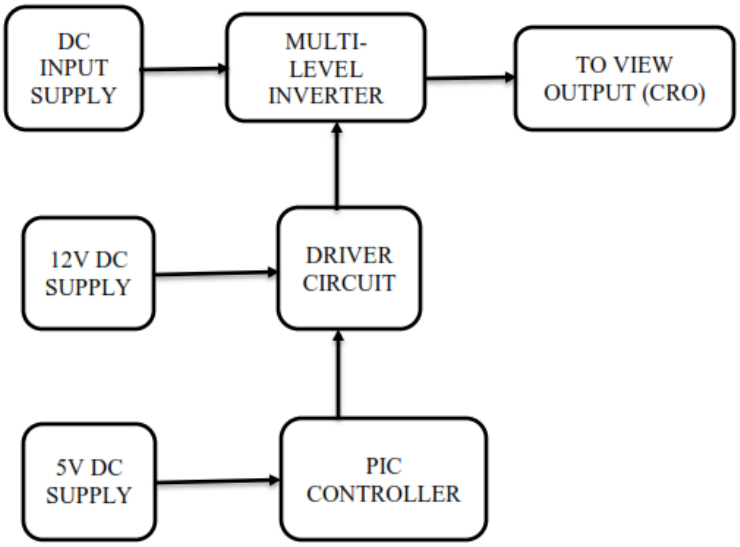

Fig.1 Block diagram of multilevel inverter

III. PROPOSED SYSTEM

A new multilevel inverter with reduced number of switches are proposed and the switching losses also get reduced and level is increased up to 21 level with reduced THD. In conventional approach, PWM techniques are used by comparing reference and carrier signals to provide the required gating signals for the inverter switches. The number of switches required to achieve m levels is given in the following equation: $Ns = 2(m - 1)$ for the implementation of 21-level CMLI, the number of switches required is 40.
The proposed ACMLI topology for 21-level inverter requires, only twelve semiconductor switches and four isolated dc sources which separate output voltage in two parts. One part is called level generation part (left side) and is responsible for level generating in positive polarity and negative polarity. The other part is called polarity generation part (right side) and is responsible for generating the polarity of the output voltage. This topology combines the two parts (left part and right part) to generate the multi-level output voltage waveform. The main purpose of this proposed ACMLI topology is to control the EMI, minimize the total harmonic distortion with selective harmonic elimination (SHE) technique and also to minimize power semiconductor switches than conventional multilevel inverter. For a conventional single-phase 21-level inverter, it uses 40 switches, whereas the proposed topology uses only 12 switches with the same principle. PIC microcontroller PIC16F877A is used to generate pulse for Switches.

3.1 Operation of the proposed topology

The proposed single-phase asymmetrical cascade 21-level inverter for line to ground voltages is shown in figure 2. With this inverter, 21 levels (0, ±10V) of output voltage as a staircase waveform is obtained.

The different switching states (i.e) ON, OFF states of different switches for obtaining different voltage levels are given in the table.1 and are explained as follows.

Switches S9, S10, S11 and S12 are used for complementary pair. When S9, S10 are turned ON together, positive half cycle (level: +1, +2, +3, +4…) can be generated and when S11, S12 are turned ON together, negative half cycle (level: -1, -2, -3 and -4…) can be generated across load. When switches S2, S4, S6 and S8 switches are turned ON the output voltage will be “zero” (level 0). When S1, S4, S6 and S8 switches are turned ON the output voltage will be “Vdc” (level +1). The output voltage will be “2 Vdc” (level +2) when switches S2, S3, S6, and S8 are turned ON. When switches S1, S3, S6 and S8 are turned ON, the output voltage will be “3 Vdc” (level +3). When switches S1, S4, S6, S7 are turned ON, the output will be “4Vdc (level +4). When switches S1, S3, S5, S7 are turned ON, the output will be “5Vdc (level +5). When switches S1, S3, S5, S8 are turned ON, the output will be “6Vdc (level +6). When switches S2, S4, S5, S7 are turned ON, the output will be “7Vdc (level +7). When switches S1, S4, S5, S7 are turned ON, the output will be “8Vdc (level +8). When switches S2, S3, S5, S7 are turned ON, the output will be “9Vdc (level +9). When switches S1, S3, S5, S7 are turned ON, the output will be “10Vdc (level +10). So, for all these positive 10 levels complementary pair S9, S10 are in ON condition. The same switches are in ON condition for all the negative 10 levels, but the complementary pair in ON condition is S11, S12.

3.2 Modulation strategies

In this proposed scheme, the selected harmonic elimination technique is used and by which the lower order harmonics are eliminated. The harmonic elimination is performed for several reasons. The first reason is that harmonics are the source of EMI. Without harmonic elimination, designed circuits would need more protection in the form of snubbers or EMI filters [5], as result, designed circuits would cost more. The second reason is that EMI can interface with control signals used to control power electronics devices and radio signals. The third reason is that harmonics can create losses in power equipment. The fourth reason is that harmonics can lower the power factor of a load. Increased harmonic content will decrease the magnitude of the fundamental relative to the magnitude of the entire current, as a result the power factor would decrease. There are four kinds of control methods for multilevel converters. They are the traditional PWM control method, selective harmonic elimination method and space vector control method and space vector PWM control. The traditional PWM, space vector PWM and space vector modulation methods cannot completely eliminate harmonics. Of these four kinds we use here the selective harmonic elimination technique which is very important and efficient method. This technique is widely used in control of the conventional VSIs, in order to improve much more the quality of their output voltages.

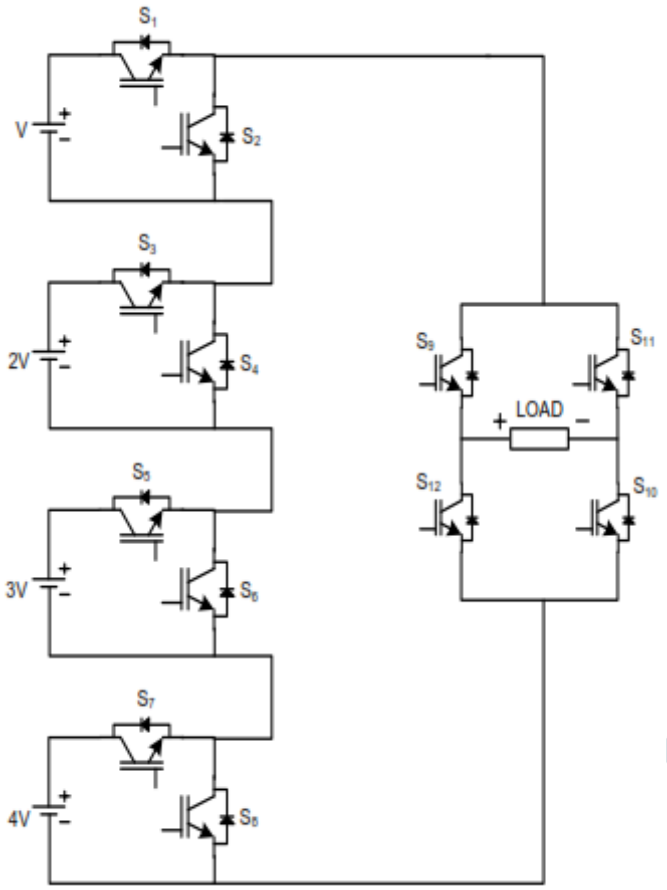

Fig.2 Proposed topology

Table. 1 Switching States of Proposed Scheme

VOLTAGE LEVEL	SWITCHING STATE												OUTPUT VOLTAGE
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	
+10	1	0	1	0	1	0	1	0	1	1	0	0	10V
+9	0	1	1	0	1	0	1	0	1	1	0	0	9V
+8	1	0	0	1	1	0	1	0	1	1	0	0	8V
+7	0	1	0	1	1	0	1	0	1	1	0	0	7V
+6	1	0	1	0	1	0	0	1	1	1	0	0	6V
+5	1	0	0	1	0	1	1	0	1	1	0	0	5V
+4	0	1	0	1	0	1	1	0	1	1	0	0	4V
+3	1	0	1	0	0	1	0	1	1	1	0	0	3V
+2	0	1	1	0	0	1	0	1	1	1	0	0	2V
+1	1	0	0	1	0	1	0	1	1	1	0	0	V
0	0	1	0	1	0	1	0	1	1	1	0	0	0
-1	1	0	0	1	0	1	0	1	0	0	1	1	-V
-2	0	1	1	0	0	1	0	1	0	0	1	1	-2V
-3	1	0	1	0	0	1	0	1	0	0	1	1	-3V
-4	0	1	0	1	0	1	1	0	0	0	1	1	-4V
-5	1	0	0	1	0	1	1	0	0	0	1	1	-5V
-6	1	0	1	0	1	0	0	1	0	0	1	1	-6V
-7	0	1	0	1	1	0	1	0	0	0	1	1	-7V
-8	1	0	0	1	1	0	1	0	0	0	1	1	-8V
-9	0	1	1	0	1	0	1	0	0	0	1	1	-9V
-10	1	0	1	0	1	0	1	0	0	0	1	1	-10V

3.3 Selective harmonic elimination technique

Selective Harmonic Elimination technique SHE is used to increase MLI efficiency by reducing output Total Harmonic Distortion THD associated with MLI switched output [6], [7]. It is rather simple to be applied to proposed topology by selecting suitable switching angles α1, α2, α3, etc….. The Fourier series expansion of the (stepped) output voltage waveform of the proposed topology in twenty one levels configuration is

$$V(\omega t) = \sum_{n=1,3,5}^{\infty} \binom{n4V_{dc}}{n\pi} [cos(n\alpha_1) + cos(n\alpha_2) + cos(n\alpha_3) \ldots\ldots cos(n\alpha_{21})]\sin(n\omega t)$$

This waveform has 10 step angles $\alpha_1\alpha_2\alpha_3 \ldots\ldots \alpha_{10}$, therefore the switching angles are chosen so as not to generate the 3rd, 5th, 7th and 9th order harmonics while achieving the desired fundamental voltage.

The mathematical statements of these conditions are:

$$\frac{4V_{dc}}{\pi[cos(\alpha_1) + cos(\alpha_2) + cos(\alpha_3) + \cdots \ldots cos(\alpha_{10})]} = V_f$$

$$\frac{4V_{dc}}{\pi[cos(3\alpha_1) + cos(3\alpha_2) + cos(3\alpha_3) + \cdots \ldots cos(3\alpha_{10})]} = 0$$

$$\frac{4V_{dc}}{\pi[cos(5\alpha_1) + cos(5\alpha_2) + cos(5\alpha_3) + \cdots \ldots cos(5\alpha_{10})]} = 0$$

$$\frac{4V_{dc}}{\pi[cos(7\alpha_1) + cos(7\alpha_2) + cos(7\alpha_3) + \cdots \ldots cos(7\alpha_{10})]} = 0$$

$$\frac{4V_{dc}}{\pi[cos(9\alpha_1) + cos(9\alpha_2) + cos(9\alpha_3) + \cdots \ldots cos(9\alpha_{10})]} = 0$$

By using these mathematical statements we eliminate the low-order harmonics 3, 5, 7, and 9.

IV. RESULT

The circuit for 21 level inverter is simulated in MATLAB/ SIMULINK and its outputs (i.e) load current and voltage are obtained. The simulation circuit, gate pulses, simulation output (load voltage and current) are given in figures 3, 4, 5, 6, 7.

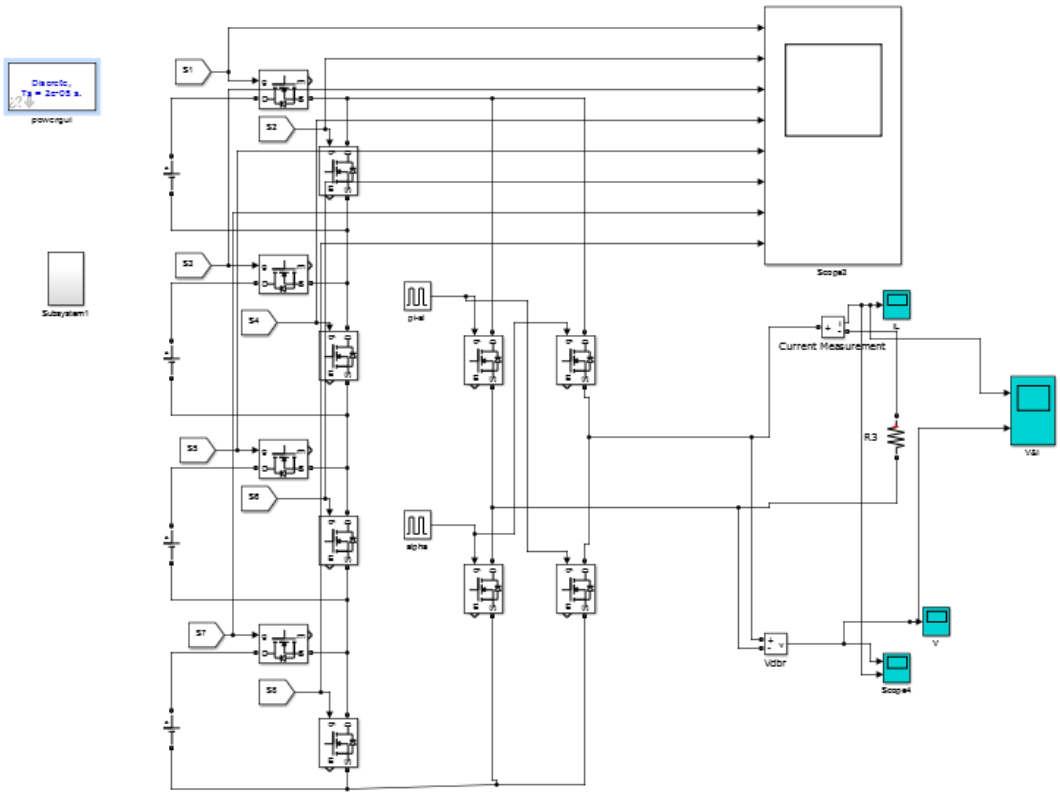

Fig.3 Simulation Circuit diagram

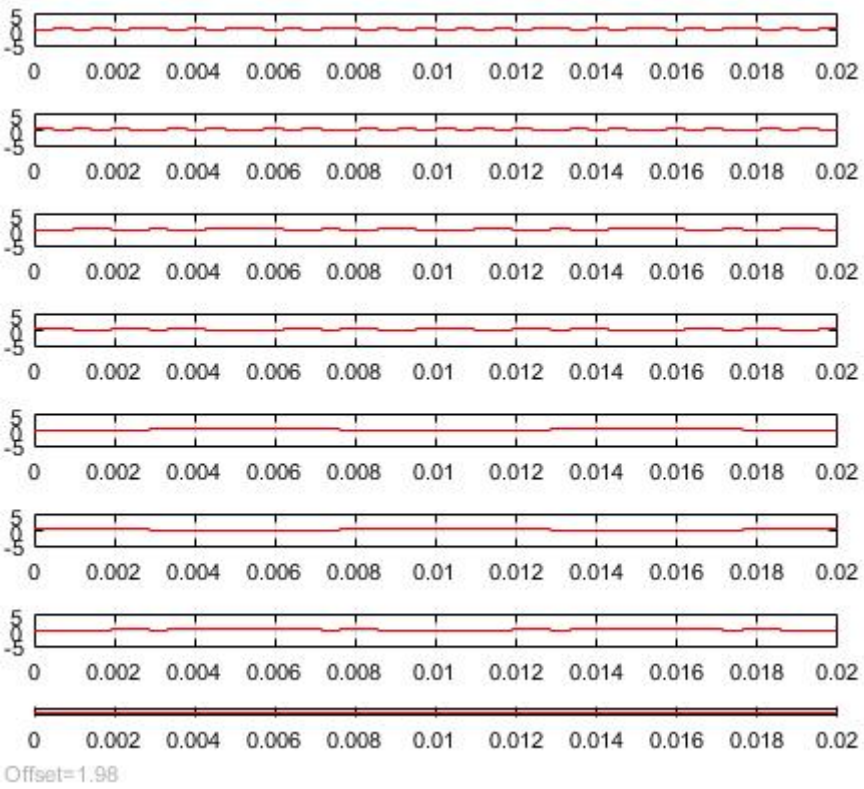

Fig.4 Gate pulses for MOSFET

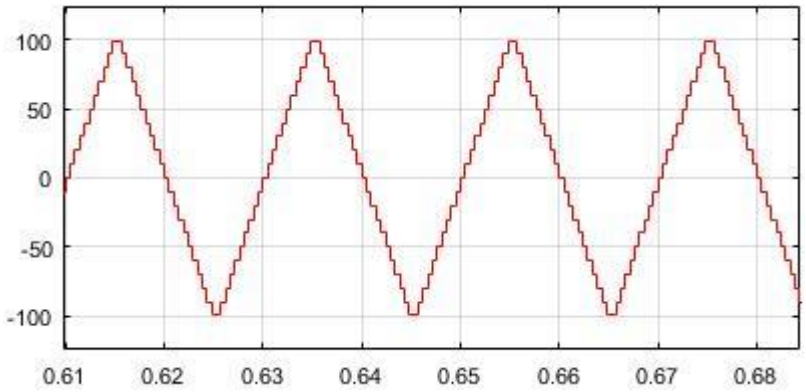

Fig.5 Load voltage

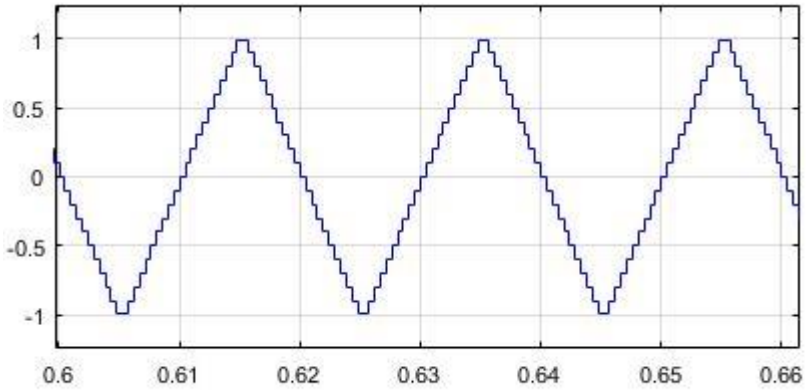

Fig.6 Load Current

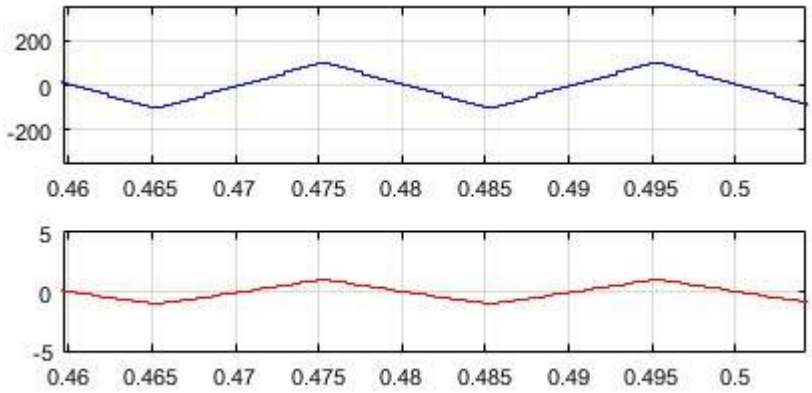

Fig.7 Load voltage and current

V. CONCLUSION

This paper introduces a new MLI topology based on conventional asymmetric cascaded half H-bridge inverter. Asymmetric DC sources configuration is utilized in order to maximize number of output voltage levels. DC sources are sized and interconnected in order to allow the proposed topology to produce both negative and positive half cycles. Thus, it eliminates the need for conventional polarity changer H-bridge. And also, instead of using 40 switches, the number of switches are reduced to 12 so that the switching losses are getting reduced and the cost required for the devices becomes less. In addition to that the THD is reduced to a reasonable value (12.6%) by using selective harmonic elimination (SHE) technique. The scheme has successfully been implemented and tested by using R2012a version of MATLAB/Simulink software.

REFERENCES

[1] Dr.Asha Gaikwad, Pallavi Appaso Arbune (2016). Study of Cascaded H-Bridge Multilevel Inverter. In: International Conference on Automatic Control and Dynamic Optimization Techniques (ICACDOT).

[2] Mohammad Ahmad and B.H. Khan, Senior Member, IEEE (2012). New Approaches for harmonic reduction in solar inverters.

[3] Jigarkumar.V. Patel, N. G. Mishra, wjter 2018, Analysis of Five- Level Cascade Multilevel Inverter Using SPWM Technique.

[4] Pravin T. Jadhav Swapnil Y.Gadgune, and Lohit R. Chaudhary "Implementation of Shunt APF based on Diode Clamped and Cascaded H-Bridge Multilevel Inverter" IEEE 2015.

[5] K.J.Mckenzie, onverter using resultant theory, Symmetric polynomials, and Power Sums ", Master thesis,2004.

[6] Kamaldeep, J. Kumar, Performance analysis of H-Bridge multilevel inverter using Selective Harmonic Elimination and Nearest Level Control technique, in: 2015 International Conference on Electrical, Electronics, Signals, Communication and Optimization (EESCO), 2015, pp. 1–5.

[7] L.M.Tolbert, F.Z. Peng, T.G. Habetler, Multilevel converters for large electric drives, IEEE Trans. Ind. Appl. 35 (1) (1999) 36–44.