DESIGN OF 32 BIT ASYNCHRONOUS RISC-V PROCESSOR USING VERILOG

G.Rajesh Babu, Asst.Proff. ,ECE Department, Usha Rama College Of Engineering and Technology , Telaprolu
M.Bhanu Prakash ,B.Tech, ECE Department, Usha Rama College Of Engineering and Technology , Telaprolu
M.Vijaya Kumari, B.Tech, ECE Department,Usha Rama College Of Engineering and Technology , Telaprolu
Ch.V.D.Ashok Kumar, B.Tech, ECE Department,Usha Rama College Of Engineering and Technology,Telaprolu
G.Sai, B.Tech, ECE Department,Usha Rama College Of Engineering and Technology , Telaprolu

Abstract – The main Aim of the Project is to design of 5 stage pipeline 32 bit asynchronous RISC-V CPU and its implementation. It performs operations,like division, subtraction, and addition. The ST control signal can be used as a centralized generator of activation signals is based on the micropipeline. The asynchronous processors have a number of benefits, mainly in System on chip it reduces the cross talk between the mixed circuits, ease of integrating multi-rate circuits, component reuse and low power consumption. Implementation of such kind of asynchronous RISC-V processor by using Verilog on Xilinx ISE Design Suite tool where it is the potential of handling R Type, I-Type and Jump instructions Along with it uses separate memory for both data and instruction. The performance parameters were obtained through simulation. The estimated power, and delay were low compared to synchronous CPU were observed by the simulation results of the design.

Key Words: RISC-V(Reduced Instruction Set), Harvard Architecture, ALU(Arithmetic and Logical Unit), Verilog, Xilinx, Asynchronous.

1. Introduction:

Most Current design is based upon a Synchronous approach. However, Nowadays there has been growing interest in asynchronous design due to low power consumption and Faster execution. In Asynchronous Design circuits, there is no clock signal and also the circuit state will changes as input changes. Asynchronous circuit has no need to wait for clock to begin its operation, these are faster than the synchronous circuits. Asynchronous circuits typically communicate and synchronizing using handshake signals. The feature of the RISC-V processor is the speed up the execution.

The 32 bit RISC-V processor comprises of load and store architecture. It means having two instructions for accessing memory LOAD instruction is to load the data from the memory and STORE instruction is used to write the data in to the memory and also uses the Hardwired architecture to increase the performance of the processor.

2. Related Work

In RISC, Harvard architecture is used that means it uses separate memory for both data and program. Asynchronous design increases the performance of the processor by reducing the waiting time at clock edges. The Operations are start its operation after immediate completion of previous operation instead of wait for the positive edge of the clock edge this can be achieved by using micropipeline structure. Asynchronous design reduces the power consumption and also reduce the heat dissipation it leads to lengthen the life of the battery. In previous work VHDL language is used to design 32 bit asynchronous RISC processor and in this work Verilog language is used to implement 32 bit Asynchronous processor due to more compatible to hardware modelling and also compact.

3. Architecture of 32 bit RISC-V Processor

3.1. Microprocessor Architecture

The 32 Bit Asynchronous RISC-V processor Comprises of Arithmetic unit(ALU), Booth's Multiplier, Control Unit, Register Bank, Memory and Data path. The Architecture divided into five stages. The pipeline stages are Instruction fetch(IF), Instruction decode(ID), Instruction Execution(IE), Memory Access(MA), Write back(WB).

The Design consists of three types of memories are Data memory, Instruction memory and register memory. In Instruction fetch stage, the 32 bit Instruction is being loaded into Instruction register by using address in the program counter(PC). After the fetch cycle the PC will increment by four addresses because of each register stores only 8 bit as it requires 4 registers to store 32 bit instruction.

In Instruction Decode stage, the 32 bit Instruction is divided. Depends Upon the 6 bit opcode it decodes from instruction. The Opcode is sent to the decoder then appropriate control signals are generated.



Fig1: 32 bit Asynchronous RISC-V processor

In Execution stage, the ALU unit performs the operations as per the decoded information. In Memory access (MA) the load and store instructions access the memory I.e read and write operations on memory

In Write Back stage, the result from ALU/Memory system write back to register file.

| Function | Opcode |
|-------------|--------|
| Addition | 00100 |
| Subtraction | 10100 |
| AND | 11100 |
| XOR | 11101 |
| OR | 11110 |
| NOT | 11111 |
| Division | 01111 |

Swap

01101

Table1:Opcode Functionality

3.2 Instruction format

The Instructions are categorized into 3 types .They are

1.Register (R) Format: The opcode consists of MSB5 bits, the Rs consists of 6 bits, Rt and Rd consists 5 bits each. These Instructions are mostly used for Arithmetic and logical(ALU) operations.

2.Immediate(I) type: The opcode consists of MSB 6 bits ,Rs and Rt having 5 bits each and 16 bit immediate address value. These instructions are for data transfer, immediate and conditional branch instructions.

3.Jump(J) type: The opcode consists of MSB 6 bits and 26 bit word address. These instructions are used for unconditional branch instructions.



4. Comparison between Synchronous and Asynchronous RISC-V Processor

In Asynchronous design the required stages only operate there by power consumption is reduced and the total delay were reduced due to its micropipeline structure. The Total power is estimated by using the X power Analyzer tool.

| S.N | Parameter | synchronous | ASynchronous | | | | |
|-----|-------------------------|-------------|--------------|--|--|--|--|
| 1 | Total Delay | 18.243ns | 12.305ns | | | | |
| 2 | Total Power consumption | 0.829 w | 0.109 w | | | | |

Table2:Comparison between synchronous and asynchronous RISC-V Processor

5. PERFORMANCE ANALYSIS:

5.1 RTL Schematic Output of 32 bit Asynchronous RISC-V processor

| JSE Project Navigator (P.20131013) - E:\Xilinx.ISE.Design.Suite.v14.7\project\RISC32\RISC32.xise - [top (RTL1)] | - | o x | | | | | | | | |
|--|----------------------------|--------------|--|--|--|--|--|--|--|--|
| 🔝 File Edit View Project Source Process Tools Window Layout Help | | _ # × | | | | | | | | |
| | | | | | | | | | | |
| Design ↔ □ 𝔅 X K If Vew: ○ If Implementation ● If K If Behavioral If If Hierarchy If If RISC32 If If Automatic includes If If If If If If If If If If If If If If If If If If If If If If If If If If If If If If If If If If <td< td=""><td></td><td>^</td></td<> | | ^ | | | | | | | | |
| Image: Simulate Behavioral Model | | | | | | | | | | |
| Start 🗠 Design 🚺 Files D Ubraries memory.v X 🚍 rom.v X 🚔 pio.v X 🚔 uart.v X 🚔 sasc_top.v X X Sasc_top.v X X Sasc_top.v | top (F | RTL 1) 🔽 🖣 🕨 | | | | | | | | |
| View by Category | | ⇔⊡₽× | | | | | | | | |
| Usign upgets of top Level block Properties of Instance: top | rioperues of instance: top | | | | | | | | | |
| Instances Pins Signals Name Value Image: Type top://type top://type top://type top://type Image: Print type Print type top://type top://type Image: Print type Print type top://type | | ~ | | | | | | | | |
| Errors A Warnings R Find in Files Results III Wew by Category | | | | | | | | | | |

5.2 Simulation Result

| < | Æ | | | | | | | | 63,603,950.000 ns |
|---------|----------|------------------|-------------|-----------------------|---------------|---|---------------|---------------|-------------------|
| | ۲ | | | | | | | | |
| | | Name | Value | 63,603,925 ns | 63,603,930 ns | 63,603,935 ns | 63,603,940 ns | 63,603,945 ns | 63,603,950 ns |
| 4 | 2 | 🐻 RST_n | 1 | | | | | | |
| | ~ | COUNT[31:0] | 00000000000 | | 000000000 | 0 100 1 10 1 10 100 100 | 001110 | | |
| J. | 6 | INDEX[7:0] | XXXXXXXX | | | XXXXXXXXXXX | | | |
| 1 | 9 | LCDDBI[7:0] | 00000000 | | | 0000000 | | | |
| î, | <u>1</u> | 🐻 RXD | 1 | | | | | | |
| 1111 | - | ዀ стs | 0 | | | | | | |
| 1.1.1 | - | 🕨 📷 KEYXI[4:0] | 1XXXX | | | 1XXXX | | | |
| 1.1 | 1 | 🕨 📷 result[31:0] | 00000000000 | | 000000000 | 000000000000000000000000000000000000000 | 000010 | | |
| 0 | r | 🗓 сік | 1 | | | | | | |
| 1.1.1.1 | 2 | 🗓 RST | 0 | | | | | | |
| 1.1.1.1 | 11231 | 1₽ сүс_о | 1 | | | | | | |
| 1.1.1.1 | 10 | 🖓 STB_O | 1 | | | | | | |
| 1 | ζ]L | 🗓 АСК_І | 1 | | | | | | |
| | 111 | ADR_O[31:0] | 00000000000 | | 000000000 | 000000000000000000000000000000000000000 | 001000 | | |
| | | 🕨 📑 DAT_I[31:0] | 00100001000 | X | 0010000 | 1000000101010111 | 111111011 | | |
| | | DAT_O[31:0] | 00010010001 | | 0001001000 | 1 10 1000 10 10 1 100 1 | 111000 | | |
| | | | | | | | | | |
| | | | | X1: 63,603,950.000 ns | 3 | | | | |
| | | < > | < > | < | | | | | |

Fig4: Simulation Result of a processor

4.3 Power Analysis

| 🜆 Xilinx XPower Analyzer - top.ncd - [Table V | iew] | | | | | | | | | | | | - | o > |
|---|--|--|--|--|--------------------------------|-------------------------------------|-----------------------------------|---|--|--|---|---|---|-----|
| 🏭 File Edit View Tools Help | | | | | | | | | | | | | | _ 2 |
| 🖻 🛃 🖉 🕲 🖹 | | | | | | | | | | | | | | |
| Report Navigator X | A | В | C D | E | F | G I | H | IJ | К | L | М | N | | |
| View | Device Family Part Package Temp Grade Process | Artix 7 xa 7a 100t csg 324 Industrial v Typical v | On-Chip Clocks Logic Signals BRAMs DSPs | Power (W) 0.008 0.001 0.002 0.015 0.000 | Used 1 4186 4976 2 | Available | Utilization (%) 7 1 | Supply Source Vccint Vccaux Vcco18 Vccbram | Voltage 1.000 1.800 1.800 1.800 1.000 | Total Current (A) 0.042 0.013 0.004 0.004 | Dynamic Current (A) 0.020 0.000 0.000 | Quiescent Current (A) 0 0.017 0 0.004 0 0.004 | | |
| Golor Source | Speed Grade Environment Ambient Temp (C) Use custom TJA? Custom TJA (C/W) Airflow (LFM) Heat Sink Custom TSA (C/W) Board Selection | -21 25.0 No NA 250 Wedium Profile NA Medium (10"x10") | IOs Leakage Total Therma | 0.000 0.082 0.109 | Effective TJA (C/W) 4.6 | 210 Max Ambient J (C) 99.5 | 17 unction Temp (C) 25.5 | Vccadc Supply | Power (W) |) 0.020 | 0.000 | 0 0.020 Quiescent 7 0.082 | | |
| Estimated Default Calculated | # of Board Layers Custom TJB (C/W) Board Temperature (0 The Power Analy (*) Place mouse ove | 12 to 15 NA sis is up to date. | tailed BRAM utilit | zation. | | | | | | | | | | |
| Views | Table View | | | | | | | | | | | | | |

Fig5: Power estimation

7. Future Enhancement:

The above design can be further enhanced to 64 bit wide RISC-V processor, optimization of area and also the logic. In future this can be optimized by upcoming techniques.

6. Conclusion:

The design of 5 stage 32 bit Asynchronous RISC-V processor has been achieved using verilog HDL, generate the RTL Schematic and simulated with ISIM. The result of the power estimation in asynchronous CPU design is analyzed by using X Power Analyzer.

REFERENCES:

[1] John Paul Shen and Mikko H. Lipasti, —Modern Processor Design: Fundamentals of Superscalar Processors, McGraw-Hill Higher Education, New York, 2005.

[2] Hwang, K., and Faye, A. —Computer architecture and parallel processing United States: N. p., 1984.

[3] Sunggu Lee. —Design of computers and other complex digital devices, Prentice Hall, Upper Saddle River, New Jersey, 2000.

[4] J. L. Neves and E. G. Friedman, —Minimizing power dissipation in nonzero skew-based clock distribution networks, Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on, Seattle, WA, 1995, pp. 1576-1579 vol.3.

[5] J. P. Fishburn, —Clock skew optimization, in IEEE Transactions on Computers, vol. 39, no. 7, pp. 945-951, Jul 1990.

[6] C. Yeh et al., —Clock distribution architectures: a comparative study, 7th International Symposium on Quality Electronic Design (ISQED'06), San Jose, CA, 2006, pp. 7 pp.-91.

[7] Mohamed Shaker, Magdy Bayoumi, —Novel Clock Gating techniques for lower Flip-flops and its Applications IEEE International Midwest Symposium on Circuits and Systems 2013, pp.420-424.

[8] Q. Wu, M. Pedram and X. Wu, —Clock-gating and its application to low power design of sequential circuits, Proceedings of CICC 97 - Custom Integrated Circuits Conference, Santa Clara, CA, 1997, pp. 479-482.

[9] J. Shinde and S. S. Salankar, —Clock gating — A power optimizing technique for VLSI circuits, 2011 Annual IEEE India Conference, Hyderabad, 2011, pp. 1-4.

[10] Q. Wu, M. Pedram and X. Wu, —Clock-gating and its application to low power design of sequential circuits, Proceedings of CICC 97 - Custom Integrated Circuits Conference, Santa Clara, CA, 1997, pp. 479-482.

[11] M. Singh and S. M. Nowick, —The Design of High-Performance Dynamic Asynchronous Pipelines: High-Capacity Style, in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 15, no. 11, Nov. 2007, pp. 1270-1283.

[12] K. Y. Yun, P. A. Beerel and J. Arceo, —High-performance asynchronous pipeline circuits, Proceedings Second International Symposium on Advanced Research in Asynchronous Circuits and Systems, Fukushima, 1996, pp. 17-28.

[13] I. E. Sutherland, —Micro pipelines, Communication of the ACM, v.32 n.6, p.720-738, June 1989.

[14] S. M. Nowick and M. Singh, —High-Performance Asynchronous Pipelines: An Overview, *I* in IEEE Design & Test of Computers, vol. 28, no. 5, pp. 8-22, Sept.-Oct. 2011.

[15] K. Yi and Y. H. Ding, —32-bit RISC CPU Based on MIPS Instruction Fetch Module Design, International Joint Conference on Artificial Intelligence, Hainan Island, 2009, pp. 754-760.

