ENERGY EFFICIENT DENSITY OPTIMIZED FUSED MAC UNIT USING CLOCK GATING AND MODIFIED SQUARE ROOT CARRY SELECT ADDER

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Abstract:

Clock gating is a well known method to reduce the power in synchronous design. Various arithmetic operations use floating point calculation and can be used for implementation of various computational and logical unit operations. In this proposed work a fused multiply- addition unit is used, which utilizes the common addition block for both addition and multiplication operations. The floating point number is first converted into the IEEE 754 format and then the calculation for both addition and multiplication is performed. The significant is extracted from the number and the calculations are performed on the basis of the exponent difference between the numbers. In the proposed approach a parallel architecture is designed which first extracts the significant and exponent value in the first unit and multiplication-addition operations on the second block. The final output is carried out on the third block where normalization and zero detector operations are performed. In this paper modified square root modified carry select adder is implemented with optimized parameters.

Index Terms: Floating point, clock gating, modified square root carry select adder, zero detector.

I. Introduction

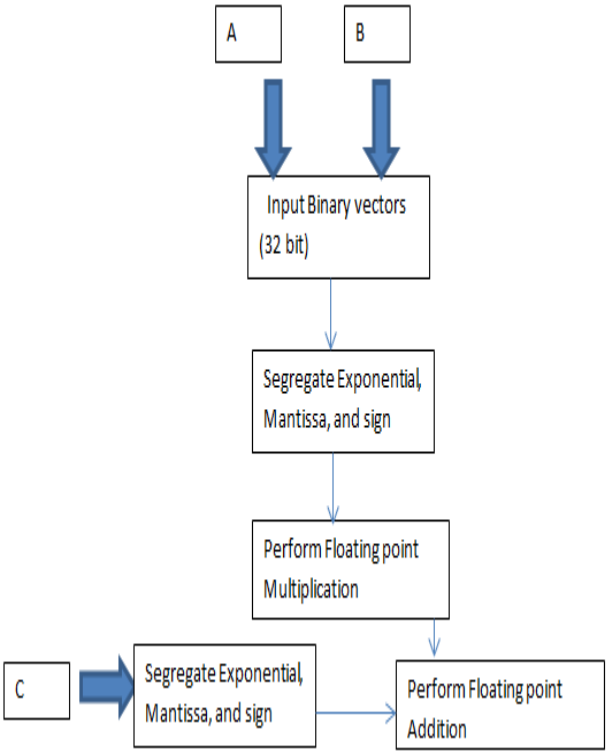
In this proposed system we use two techniques for FMA i.e. clock gating and modified square root carry select adder. By using of this clock gating we can reduce the power consumption and modified square root carry select adder is used to reduce the area and time delay. Whenever we use these techniques along with floating point there is both energy efficiency and density optimization .

II.FLOATING POINT MAC UNIT

In this proposed approach we are required to implement certain techniques for fused multiply – add unit. In our proposed architecture the adder part of addition unit is common for multiplication as well. It's implemented in the architecture in order to reduce the total area and time delay . Initially the input is converted into IEEE – 754 standard format. The resulting operation is called post normalization. This unit is taken as a parallel processing unit. The units proposed in the technique include significant alignment unit where the comparison of exponents and the alignment of significants take place, it's required to extract the exponents, significants and sign bit from the given input operands. Then, the comparison is done between the exponents. The larger exponent is shifted to right in accordance with the difference of two numbers. Thus the exponents are first compared and then on the basis of comparison the greater significant is shifted accordingly. However, if there will be no difference in the exponents then the significant should remain same i.e. there will be no shifting. Let us take 'X' and 'Y' as two input floating point numbers that were initially

converted to IEEE – 754 Standard format. So it's required to extract all parts of floating point numbers and then compare their exponents. Now let us suppose the exponent of input 'Y' is greater than input 'X' then its required to shift the significant of 'X' to +the right by an amount equal to difference of exponent value. Then again the significants of the inputs are translated to IEEE format as shown in the below figure 1.

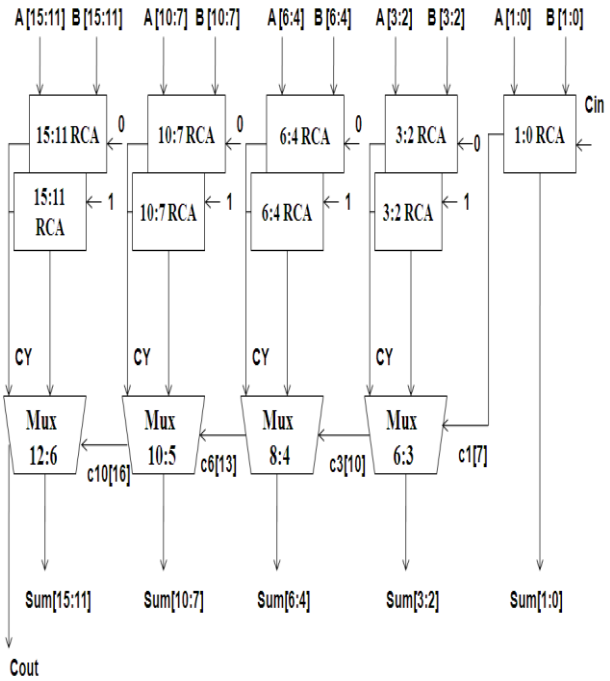
Figure1: Flow chart of floating point.



III.EXISTING METHOD

The Regular Carry Select Adder is represented in fig 2. Basically this project is mainly targeted for data processing processors to perform fast arithmetic functions.

Fig 2: Regular Carry Select Adder



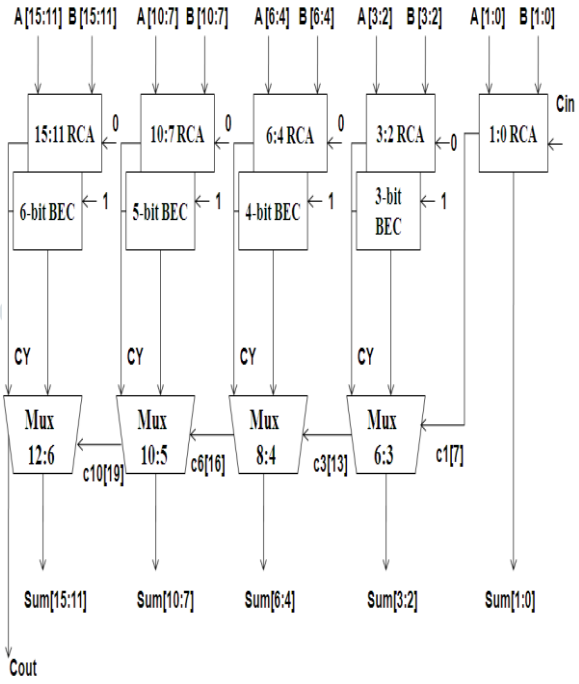
Here in this design, the carry select adder is designed using Ripple carry adders and multiplexers. The design can be viewed as groups where the groups are internally designed using n-bit RCA and multiplexers.

Initially, we add carry 0 as well as carry 1 to the given inputs, then based on the carry which is given to the multiplexer the required output is obtained i.e.; if the carry for the multiplexer is 0 then it take the output from the first block as shown in the fig 2.So,we get the desired output. But, the drawback of this method is, it consumes more area, in order to overcome this drawback we used modified square root carry select adder.

IV. PROPOSED METHOD

Here in this paper we are implementing modified square root carry select adder. By using this adder we reduce the area and time delay.

Fig 3: Modified square root Carry Select Adder



As stated above, the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption.

Finally, the performance of the two designs is evaluated in terms of area, power and time delay.

V.MERITS

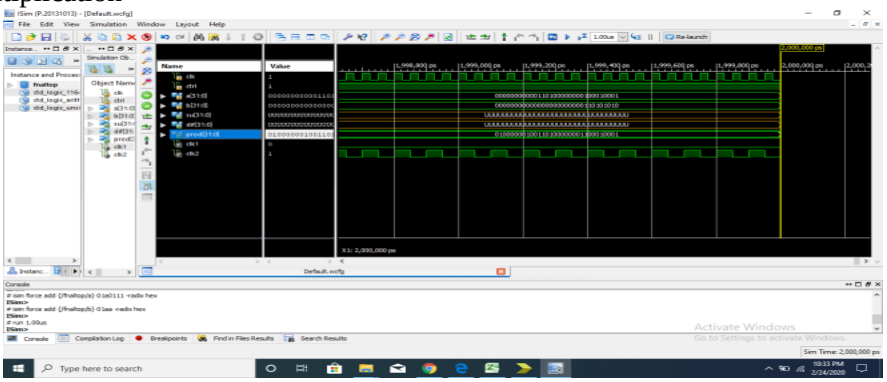
By using this MAC unit using clock gating and modified square root carry select adder the following are the merits;
1)We can reduce the area by using modified square root carry select adder technique so, there is an density optimized.

2)We can reduce power consumption by using clock gating technique.

3)We can get output within less time due to two techniques(clock gating and modified square root carry select adder).so, over all time cdelay is reduced.

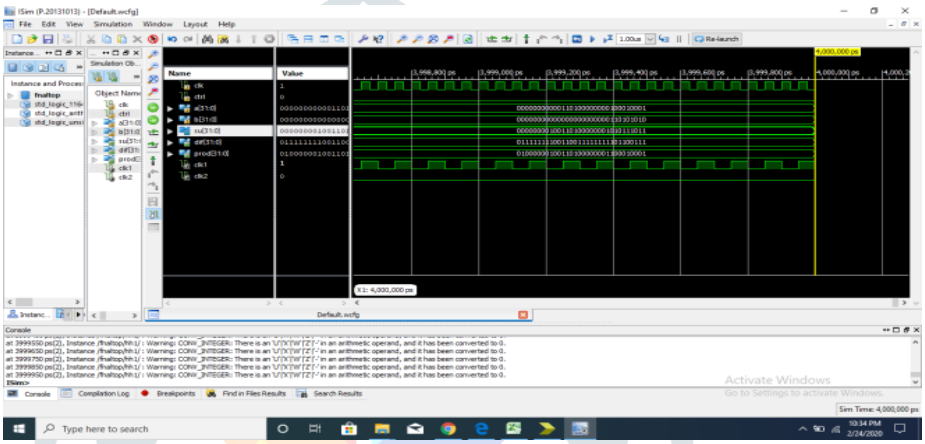
VI.SIMULATION

fig 4: floating point multiplication



when we apply clock gating to the adder circuit then it block the current flow so we will receive only product output.

fig 5: floating point representation of both adder and multiplication output.



When we apply clock gating to the multiplication circuit then block the current flow to multiplier then we will receive both product and adder output.

VII.CONCLUSION

Floating point arithmetic operations form an important part in various digital signal processing applications. Fused operations in floating point unit is an important area of research in recent times and various researchers have proposed architectures to improve the efficiency and the accuracy of the arithmetic operations. In the present work a fused architecture is proposed to improve the timing delay in the design. The techniques clock gating and modified square root carry select adder are used to reduce power consumption and area respectively .

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