The revolutionary change in transistor technology: FinFet

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Abstract: Transistor is an active device of electronics and it is a very big revolutionary research in electronics industry. As time flies away, needs of customers increases in many aspects of area and portability of device. Circuits for Nanoelectronic devices become more complicated and most challenging. The first transistor invented in 1948 in Bell laboratory. Initially Bipolar Junction Transistors able to perform various operation of electronic. But time to time requirements changes and technology changes. After BJT, Field effect transistors (FET) introduced. These were most advanced transistors. These transistors operate by the effect of electric field generated. But in nanoelectronic devices FET transistors cannot perform well. Now days some new transistors are introduced like MESFET, FinFet.

To make more short devices, parameters of transistors have to scale down. But after a certain limit FET behaves enormously. New transistor is come in picture for solution of MOSFET limitation is Multi-gate Field Effect Transistor and FinFet is a type of Multi-gate Field Effect Transistor (MGFET). This paper includes limitations of BJT and FET and advantage and challenges of FinFet.

Keywords: BJT, MOSFET, FinFet, multi gate transistor, short channel effect

I. Introduction

These tiny transistors just play a big part in our electronic gate. A famous scientist Gordon Moore described the evaluation of transistor density in integrated circuits in 1965. He mentioned in his paper that number of transistors per chip would quadruple every three years as mentioned in figure.1 [1, 2].

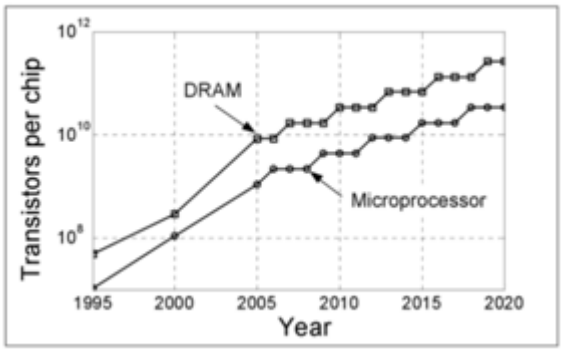

Figure.1: Number of transistors increased per chip over the years [1]

Future nanoelectronic devices face substantial challenges, in particular increased power consumption, saturation of performance, large variability and reliability limitation. In this respect, novel materials and innovative device architectures will be needed for Nanoscale FETs. The Main limitation of FETs is heating of device and the challenges are innovation in technologies, nanoscale material, small devices architecture, very low power and high performance. The main limitation of MOSFET is leakage current increases, due to

scaled down device. Leakage current increases power dissipation increases. Electronic devices have large number of MOSFET devices, so overall power dissipation increases. As chips have millions of such devices, leakage current results in large power dissipation. The reason of higher off current is due to Drain Induced Barrier Lowering (DIBL) effect [3]. To diminish this problem, gate-oxide thickness can be reduced but it leads to increase leakage due to Gate Induced Drain Leakage (GIDL). To minimize GIDL, very high and abrupt drain doping is preferred because it provides lower series resistance as required for high transistor drive current. Multiple gates with fully depleted and partially depleted fabrication techniques are used for overcome short channel effects [4-7].

II. Short channel effects (SCE)

Due to short channel effect parameters affects the overall system performance. All dimensions, parameters affected after the shrinking the device. But most affected dimension is channel length and due to this all worst effects occurs. As research is continuously going on to overcome this short channel effect. A solution is that covers the complete channel with gate control. This can be possible in 3D design of FET using Silicon on Insulator fabrication technique (SOI). In planar design techniques channel controls by gate to source voltage Vgs, but in case of small channel devices electric field dominates the channel. The main parameters are which affects due to short channel length are: Vt, Vgs, Vds, Short channel effects are following:

1. Drain Induced Barrier Lowering (DIBL)
2. Punchthrough
3. Surface scattering
4. Velocity saturation
5. Impact ionization
6. Hot electrons
7. Hot Carrier Injection (HCI)

(a) **DIBL:** In conventional MOSFET operation channel is formed when gate to source voltage Vgs increased beyond threshold voltage. After the channel formation between source to drain, a path will induce for flowing of current. With this path current flow from drain to source by applying drain to source voltage (Vds). The channel inversion occurs when electrons cross depletion layer barrier. For crossing barrier electrons should have sufficient electric field and this electric field provides by gate to source voltage Vgs). From the above discussion it is concluded that current cannot flow without inversion channel and the Vgs is responsible for channel formation. This all apply for long channel devices. But in case of short channel devices source and drain are very close to each other, so sometimes current starts flow from drain to source without applying Vgs. Due to this sub-threshold current flows under condition Vgs<<Vto. This phenomenon is known as Drain Induced Barrier Lowering (DIBL). This is very serious concern during scaling.

(b) Punchthrough

As drain to source voltage (Vds) increases more than depletion region also increases. Due to this carriers flow in the body instead in channel. And current Ioff increased. This phenomenon is known as punchthrough.

(c) Surface scattering

In FET Charge carrier electron flows in conduction channel from source to drain. This channel is formed by gate to source voltage Vgs. As charge carriers have opposite polarity to Vgs, they attracted by it. Electric field is induced while applying Vgs and this electric field attracts the charge carriers. Mobility of charge carrier decreased due to this phenomenon. This phenomenon is known as surface scattering. This phenomenon more affects in short channel devices. Because length of channel is decreased and the lateral electric field component becomes stronger, which is generated by drain to source voltage Vds. This electric field dominates the vertical electric field, which is created by the gate to source voltage. Charge carriers more scattered in case of short channel devices from Si-Sio2 surface.

(d) Velocity Saturation

Velocity of charge carriers depends on mobility and electric field as states in below equation. Electric field is increasing due to short channel, so velocity of charge carries also increased. Electrons can crossed the junction by gaining high velocity.

V=μE

V=velocity of charge carriers

μ=mobility of charge carriers

E=electric field

This equation states that velocity of charge carriers (Holes or electrons) proportional to electric field. In short channel devices electric field is higher and due to this velocity increased rapidly.

$$vd = \frac{\mu E}{1 + {}^{E}/_{Ec}}$$

Ec= critical electric field

(e) Impact ionization

In previous discussion, velocity of charge carriers increased due to high lateral electric field, due to short distance of channel between source and drain. These carriers with high energy are called as "hot carriers". The high energy hot carriers travel through substrate and a possibility of collision with atom. Due to enough energy of charge carriers, this energy passed to the atom upon collision can knock out an electron out of the valence band to the conduction band. The result of this collision an electron-hole pair generates. From this hole is attracted to the substrate while the electron attracted by the drain. This phenomenon is known as impact ionization effect.

(f) Hot electrons

In this situation electron-hole pairs is having very high energy and due to this two adverse effects can happen.

A Bipolar junction transistor (BJT) is formed with source-substrate-bulk. In this source behaves as emitter, substrate behaves as base and drain behaves as collector. Generally, in large channel dvices this transistor is in off condition due to large voltage drop at substrate. But In small channel devices it is in on condition. Due to impact ionization effect holes attracted by the substrate and this is enough to create voltage drop at substrate.

(g) Hot Carrier Injection (HCI)

One more adverse effect due to hot carriers is ageing. Sometimes these high energy electrons move towards oxide surface. Due to this threshold value will change and it will be increased. The transistor behavior abruptly changes. This effect is affecting the memories in terms of interpretation of bits.

III. Multi gate FETs:

To overcome short channel effect 3D Silicon on Insulator (SOI) MOS transistor introduced. There are two types of SOI: partially and fully depleted SOI. From the above discussion of short channel effects, gate electrode is mostly affected by electric applying electric fields from Vgs and Vds [8-10]. Buried oxide is used in these devices to terminate extra electric field. Figure2 shows the basic difference between multiple gate and planar transistor. Following are the types of FET on the basis of number of gates:

Single gate: MOSFET (only one gate electrode)

Double gate: GAA, FinFET, MIGFET

Triple gate: Trigate FET, π-gate FET, Ω-gate FET

Quadruple: Quadruple gate FET, cylindrical FET, Multi bridge FET

Here double gate means single gate electrode present on two different sides. Triple gate means single gate electrode present in three sides. MIGFET is an exception case, in this two gate electrodes are used and these are biased with different potentials as shown in figure.3 [11].

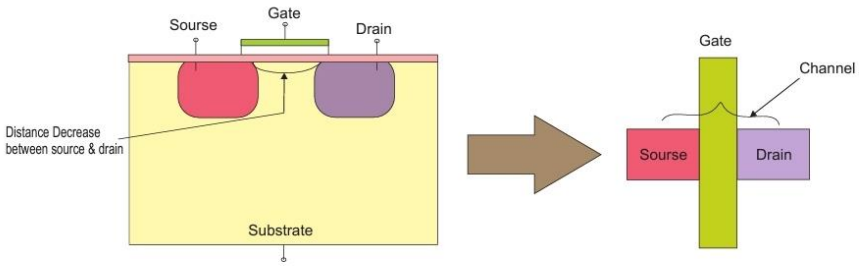

Figure.2: Planar MOSFET Transistor and multi gate transistor with full control of gate

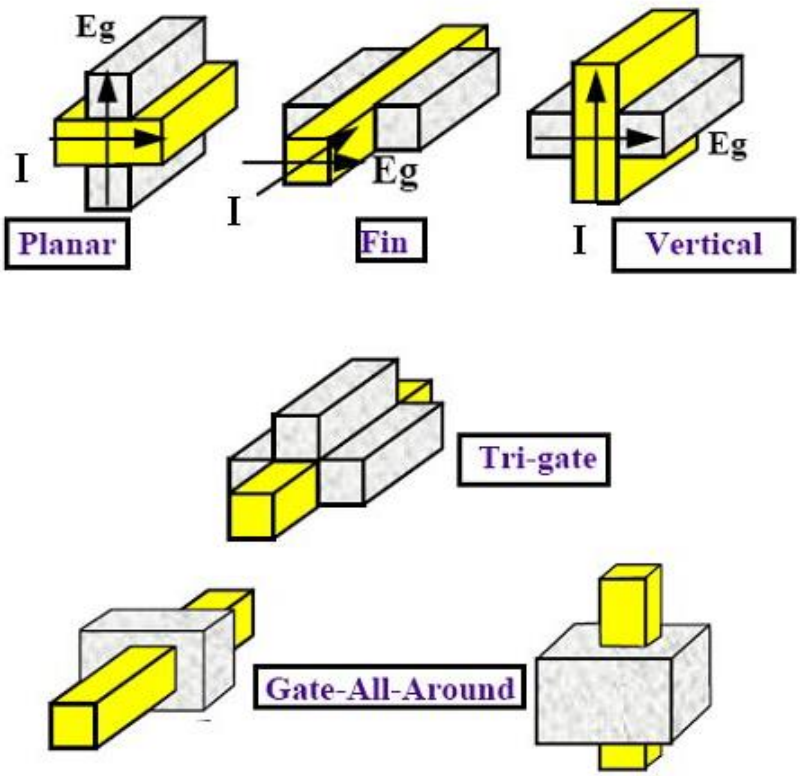

Figure.3 Multiple gate electrode transistors [11]

Table 1 shows the multiple gate transistors, which affects the effective gate length. FinFet and nanowire transistors are able to maintain the desired gate length [12, 13].

Table.1 multiple gate Effects on gate length [12, 13]

S. No.	Transistor	Gate length	Effective gate length
1.	Planar SOI	10nm	2.5nm
2.	Double gate	10nm	5nm
3.	Tri-gate (FinFet)	10nm	10nm
4.	Surrounding gate (nanowire)	10nm	10-20nm

IV. FinFet

In small devices doping concentration increases to overcome short channel effect. DELTA (Depleted Lean-channel Transistor) is a first double gate Silicon-on-insulator FET transistor in 1989. This is type of fully depleted method of fabrication. In these devices thin layer of silicon is used and these are called finger, leg or fin. Fully depleted SOI provides good scalability and efficiency and they required less silicon substrate for building multi gate transistor. The concept of multiple gate FETs comes in picture to control inversion layer completely. Channel of FinFet fully controlled by gate electrode. There are two types of FinFet: double gate and triple gate. Triple gate FinFet is widely used for better performance

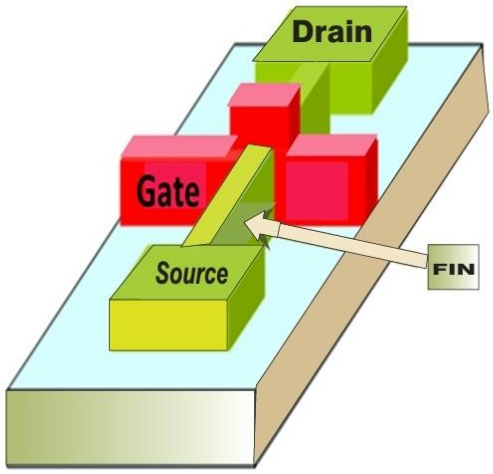

Figure.4 Structure of FinFet

FinFet is a type of double gate MOSFET. In this, Fin means gate electrode covers the channel. Various short channel effects due to lost the command of gate on channel length. This fin gate wrapped on entire channel length to reduce the leakage current as shown in figure.4 . This is the basic difference between FinFet and MOSFET as shown in figure.5. FinFet can flow more current per unit area than planar devices, because gate covers complete effective channel length.

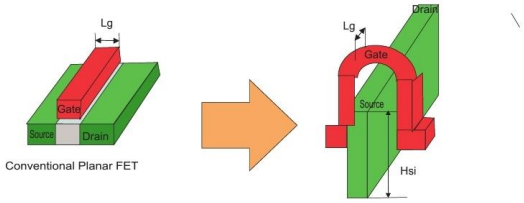

Figure.5 Comparison between Planar FET and multiple gates FET

V. Conclusion and Future work

Finfet transistor overcomes the problem of short channel in planar transistors. This improves short channel controls through its fully depleted operation and requires low

This is very useful in memory designing. Transistor is a basic element of any electronic circuit design like memory designing. SRAM memory cell is able to perform read, write and hold operation by using

MOSFET. But there is main problem is power dissipation, which degrades the overall performance of device. As electronic devices becomes shorter and shorter day by day. For this small scale devices needed and if MOSFETs are used for this all small scale effects encounters. Now a day's FinFets are used as a design element of SRAM. This improves Stability of SRAM and decreased power dissipation. In future electronic chips will replace planar transistors with multi gate 3D transistors.

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