DESIGN OF LOW POWER HIGHPERFORMANCE 2-4 AND 4-16 MIXED LOGIC LINE DECODERS

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ABSTRACT: A mixed-logic design technique for line decoders,combining transmission gate logic, pass transistor dual-value logic and static complementary metal oxide semiconductors by this paper.Two novel topologies provided for the 2-4 decoder: a 14-transistor topology aiming on minimizing transistor depend and energy dissipation and a 15-transistor topology aiming on high power optimization.Both a traditional and an inverting decoder are applied in each case,yielding a total of four new designs.Furthermore,4 new 4-16 decoders are designed,by using mixed-logic 2-4 pre-decoders combined with general CMOS post-decoder.All proposed decoders have complete swinging functionality and reduced transistor rely as compared to their

traditional CMOS counterparts.Finally,quite a few comparative spice simulations on the 32 nm shows that the proposed circuits present a enormous development in power and put off,outperforming CMOS in nearly all cases.

KEYWORDS: Line decoders, Mixed -logic, High strength put-off performance.

I. INTRODUCTION

Address decoder is important elements altogether SRAM memory block which answer very high frequency.Time interval and power consumption of memories is essentially determined by decoder design.Design of a random access memory(RAM) is usually divided in to two parts,the decoder,which is that the circuitry from the address input to the word line,and therefore the sense and column circuits,which incorporates the bit line to the data input/output circuits.Due to large amount of storage cells in memories it are often found various solutions of address decoder designs resulting in power consumption reduction and performance growth.Usually differeing types of pre charging dynamic decoders are used.Design of dynamic decoder is complex and having more probability of wrong sensing.Traditional static decoder gives more accurate result but it's having more number of transistors with large delay.

Decoders play a very significant role in memory applications so we implement high-speed a mixed-logic design method for line- decoders.Static CMOS circuits are used for the sizeable majority of logic gates in incorporated circuits.They include complementary nMos pulldown and pMos pullup networks and present exact performance in addition to resistance to noise and device variation.Therefore,CMOS logic is characterized by means of characteristics towards voltage scaling and transistor sizing and linked to transistor gates only,offering reduced design complexity and facilitation of cell-based logic synthesis and design.

Pass- transistor logic was especially developed in the 1990's,when numerous layout patterns have been introduced aiming to offer

Alternative of CMOS logic is enhance speed,energy and area.Its important layout difference is that the inputs are applied to both the gates and the source/drain diffusion terminals of parallel pairs of nMos and pMos called transmission gates.

Novel design technique based decoder is implemented using 32nm CMOS technology which has better power consumption and

Delay compared with traditional decoder.

The proposed design is utilize mixed logic with the assistance of various techniques are observed from different existed logic.Circuits represented in above.Modified mixed logic decoder analysis increases the performance(delay and power) compared with existed CMOS NAND and NOR based decoder.The paper is partitioned as follows:Section II represents related work and styles.Section III Description of mixed logic design. Section IV represents proposed system.Section V represents results and conclusion.

II. RELATED WORK

i. 2-4 line decoder

A 2-4 line decoder generates the 4 minterms D(0-3) of two input variables A and B.Its logical operation is summarised in table.Depending on the input combination,one among the 4 outputs is choosen and set to 1 while the others are set to 0.An inverting2-4 decoder generates the complementary minterms I(0-3),thus the chosen output is about to 0 and therefore the rest are set to 1,As shown in table 1.

By using 2 inverters and 4 NOR gates,both yielding a complete of 20 transistors of 2-4 Decoder and this will be shown in fig1(a). The truth table of the 2-4 decoder is shown in table 1.

A0	A1	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table I: Truth table of 2-4 decoder

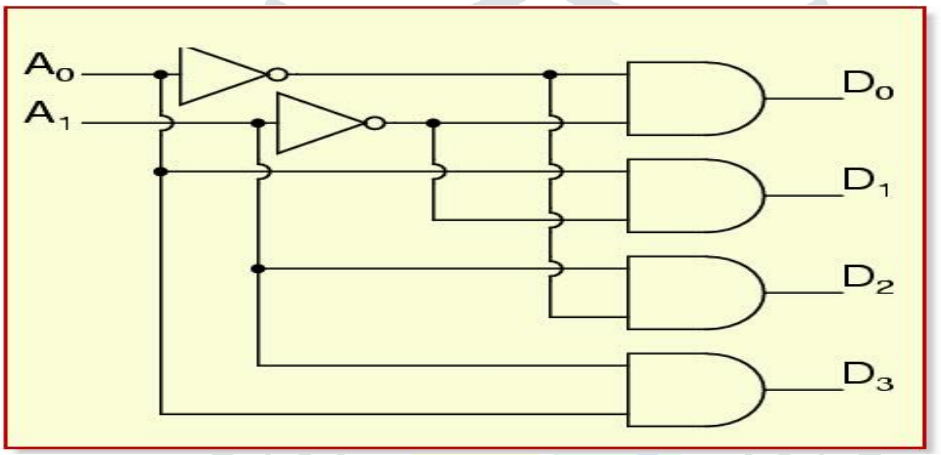


Fig1(a):Non-inverting 2-4 decoder

i. Inverting 2-4 decoder

An inverting 2-4 decoder generates the complementary minterms Q(0-3),thus the chosen output is about to 0 And therefore the rest are set to 1,as shown in table 1. An inverting 2-4 decoder are often designed by using 2 inverters And 4 NOR gates,both yielding a complete of 20 transistors and this will be shown in fig1(b). The truth table of the inverting 2-4 decoder is shownin table 1.

A	B	Q0	Q1	Q2	Q3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Table II:Truth table of inverting 2-4 decoder

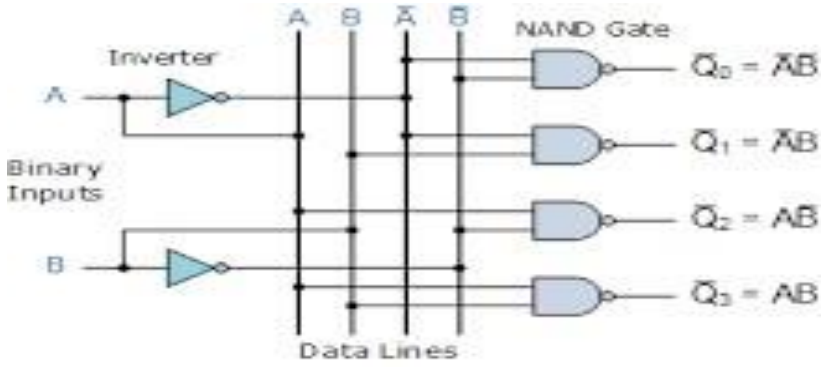


Fig 1(b): Inverting 2-4 Decoder

ii. 4-16 Decoder

A 4-16 line decoder generates the 16 minterms D(0-15) of 4 input variables A,B,C and D and an inverting 4-16 line decoder generates the complementary minterms I(0-15).With this system,a 4-16 decoder are often implemented with two 2-4 Inverting decoders and 16 2-input NOR gates(Fig.2(a)) and an inverting one can be implemented with 2 2-4 decoders and 16 2-input NAND gates(Fig.2(b)).In CMOS logic ,these design require 8 inverters and 24 4- input gates,yielding a complete of 104 transistors each.

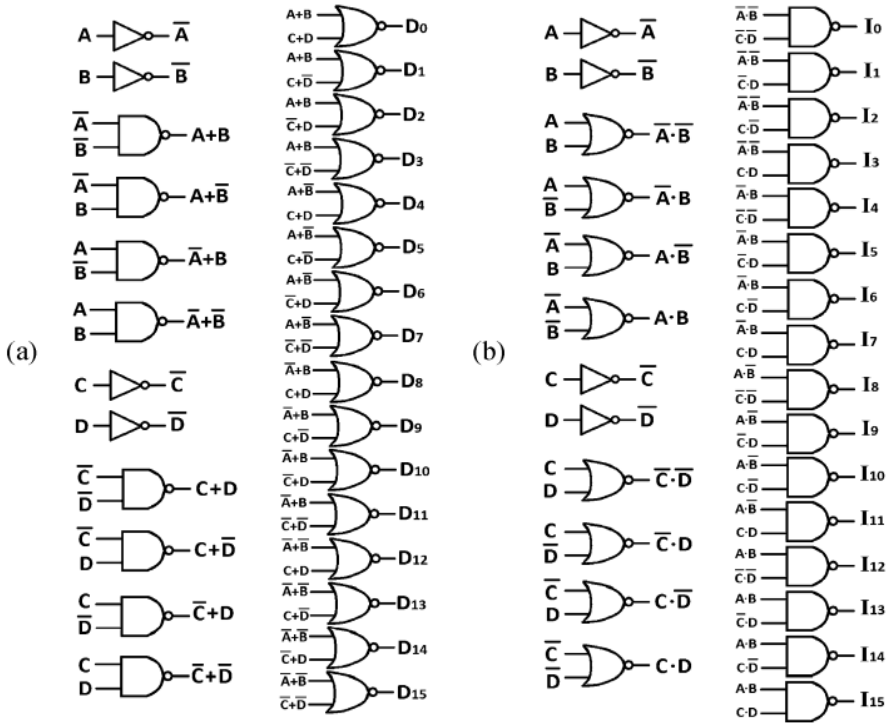


Fig 2(a):Non-Inverting 4-16 Decoder Fig2(b):Inverting 4-16 Decoder

A	B	C	D	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table III:Truth Table of Non-Inverting 4-16 Decoder

A	B	C	D	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Table IV: Truth Table of Inverting 4-16 Decoder

III. DESCRIPTION OF MIXED LOGIC DESIGN

Regarding pass-transistor logic,there are two main circuit styles:those who use nMOS only pass-transistor circuits,like CPL and people that use both nMOS and pMOS pass-transistors,like DPL and DVL.The design we consider during this work is DVL,which offers an improvement on DPL,preserving its full swing operation with reduced transistor count.The 2 input DVL AND/OR gates are shown in respectively.Almost like the TGL gates,they are full-swinging but non-restoring.Assuming that complementary inputs are available ,the TGL/DVL gates require only 3 transistors,as against the 4 required in CMOS NAND/NOR gates.Decoders are high fanout circuits,where few inverters are often employed by multiple gates,thus using

the TGL/DVL gates may result to reduced transistor count.

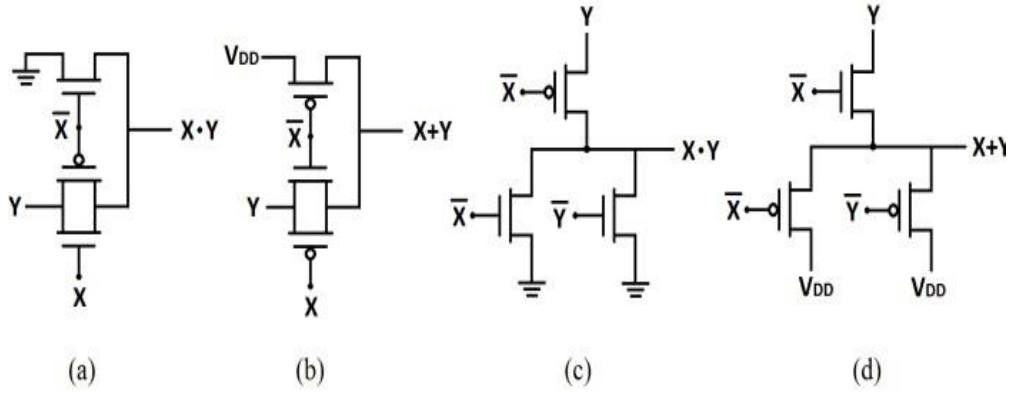


Fig3: TGL AND GATE TGL OR GATE DVL AND GATE DVL OR GATE

IV. PROPOSED SYSTEM

4.1.14-transistor 2-4low power decoder:

Using TGL or DVL gates we were designed a 14-transistor 2-4 low power decoder.It require 5 PMOS and 9 NMOS,whereas14-transistor inverting decoder would require 5NMOS and 9PMOS,yielding a complete of 14 transistors each.The new 14 transistor 2-4 decoders are shown in fig 4.1(a) and fig 4.1(b)

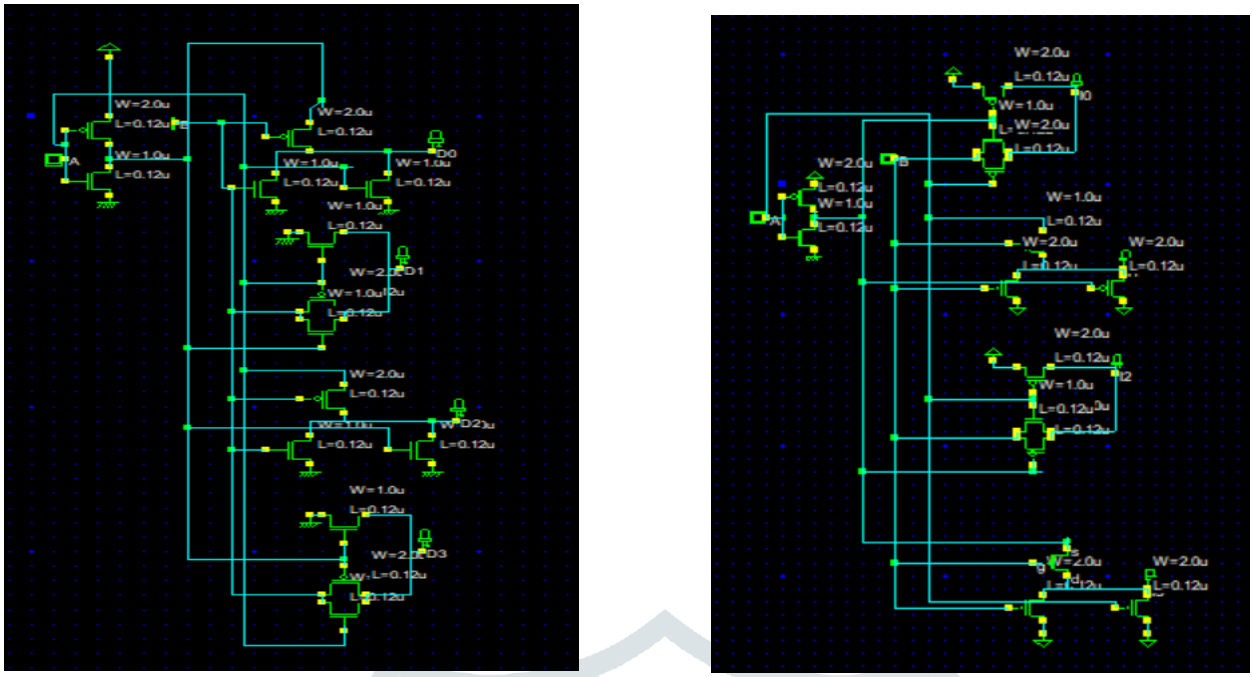


Fig 4.1:New 14 Transistor 2-4 decoder (a)2-4 Low Power (b) 2-4Low Power Inverting

Using DVL gates we were designed D0 and D2 where A is employed as propagating signal and D1 and D3 are often designed with TGL gates ,where B is employed as propagating signal.Whereas in inverting I0 and I2 are often designed with TGL gates whereas B is propagating signal and I1 and I3 are often designed with DVL gates where A is employed as propagating signal.The new two topologies are LP and LPI whereas LP stands as Low power and that I is as inverter.

4.2.15 transistor 2-4 High performance decoder:

We have a drawback in low -power topology with in the case of D0 and I3 regarding worst case delay which comes from the utilization of complementary A is used as propagataing signal.However,D0 can be designed with CMOS NOR gate and I3 with CMOS NAND circuit.The 2-4 HP are often designed by using 9 nMOS and 6 pMOS whereas 2-4 HPI are often designed by using 6 nMOS and 9 pMOS ,yielding a complete of 15 transistors each.The 2-4 HP and 2-4 HPI decoders are shown in fig 4.2(a) and (b) respectively.So,in 15 transistor topology there's a improvement in delay,slightly increase in power dissipation compare than 2-4 low power topology .

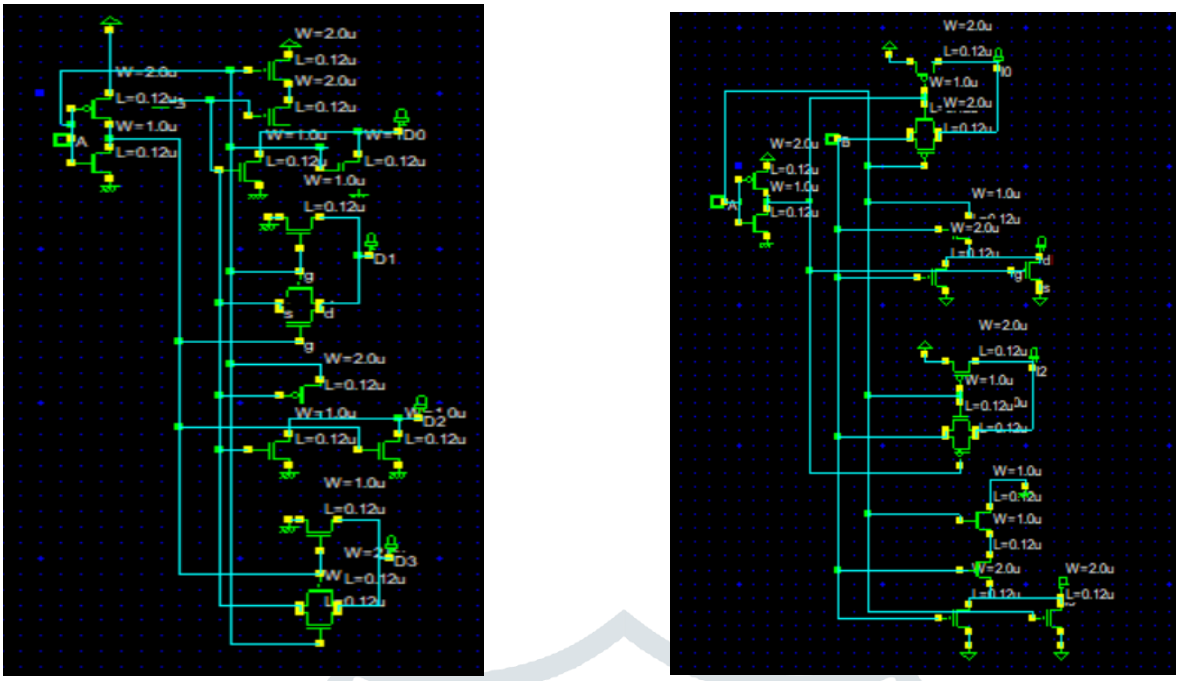
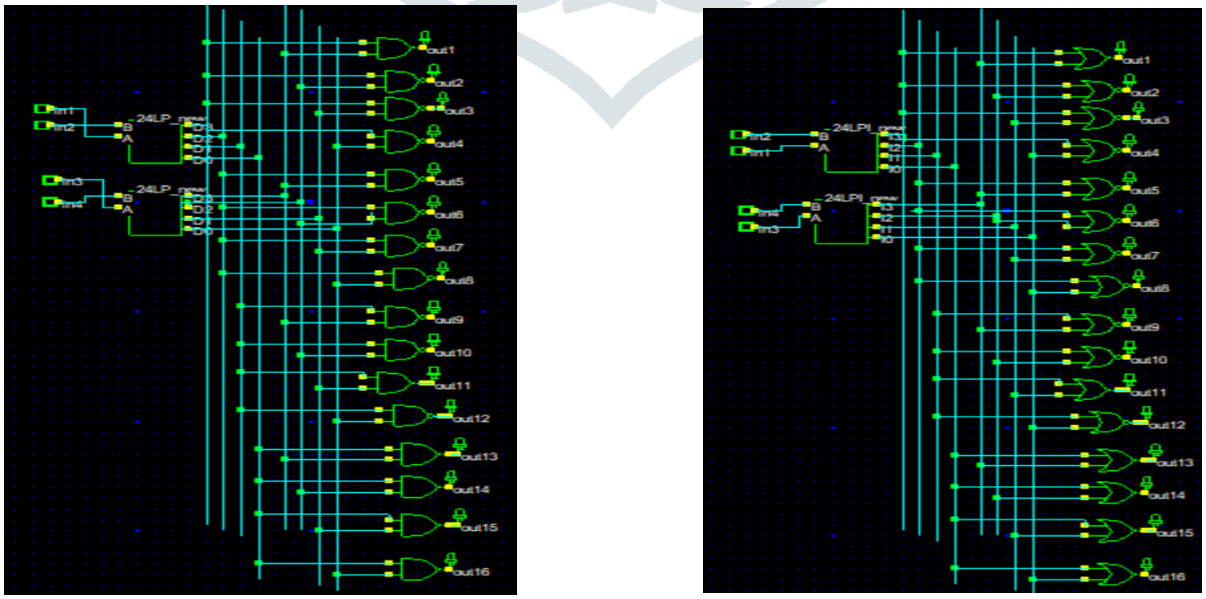


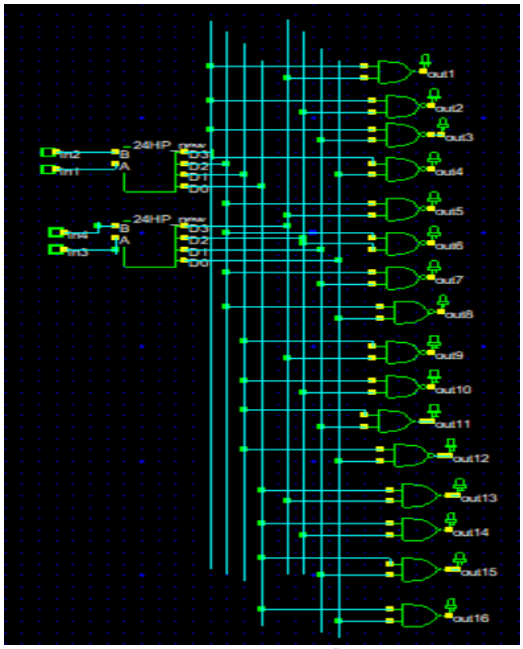
Fig 4.2: New 15 Transistor 2-4 decoder (a)2-4 HP (b)2-4 HPI

4.3.New 4-16 topology:

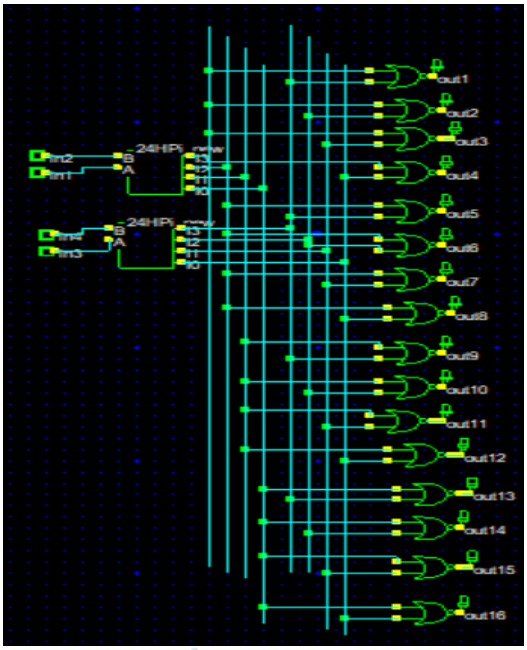
By combining 2 2-4 LPI pre decoders with a NOR based post decoders we are getting a 4-16 LP which is shown in fig4.3(a) whereas 4-16 LPI are often designed by combining 2 2-4 LP pre decoders with a NAND based post decoder shown in fig 4.3(b) yielding a complete of 92 transistors.The 4-16 HP are often designed by combining 2 2-4 HPI pre- decoders with a NOR based post decoder shown in fig4.3(c)whereas 4-16 HPI are often designed by combining 2 2-4 HP pre decoders with a NAND based post decoders shown in fig4.4(d),yielding a complete of 94 transistors.



(a) (b)



(c)



(d)

Fig 4.3: (a) 4-16 LP (b) 4-16 LPI (c)4-16 HP (d)4-16 HPI

V RESULTS AND CONCLUSION

Table III:Power Dissipation Results

2-4 DEC.	500 MHZ			1 GHZ			2 GHZ			4-16 DEC.	500 MHZ			1 GHZ			2 GHZ		
	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V		0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V
CMOS	269	415	622	545	862	1287	1100	1768	2636	CMOS	841	1349	2030	1692	2751	4112	3393	5564	8310
2-4LP	246	386	576	495	790	1173.1	996	1594	2369	4-16LP	785	1258	1878	1577	2546	3816	3160	5140	7662
2-4HP	248	391	583	499	800	1185	1004	1618	2397	4-16HP	791	1270	1905	1588	2572	3847	3182	5198	7749
CMOS INV.	268	421	631	849	867	1290	1095	1767	2622	CMOS INV.	843	1330	2000	1698	2735	4096	3412	5562	8327
2-4LPI	242	381	567	488	778	1155	984	1571	2337	4-16LPI	788	1265	1888	1584	2566	3827	3178	5179	7724
2-4HPI	245	389	578	495	793	1175	998	1604	2377	4-16HPI	793	1271	1894	1592	2580	3841	3194	5209	7758

2-4 DEC.	500 MHZ			1 GHZ			2 GHZ			4-16 DEC.	500 MHZ			1 GHZ			2 GHZ		
	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V		0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V
CMOS	176	127	128	357	264	265	720	541	543	CMOS	1123	817	836	2260	1666	1694	4532	3369	3423
2-4LP	203	149	155	408	306	315	821	617	636	4-16LP	995	730	750	1998	1478	1524	4004	2984	3061
2-4HP	153	115	120	308	235	244	620	475	494	4-16HP	963	698	702	1933	1413	1417	3873	2855	2854
CMOS INV	167	126	134	530	260	274	683	529	556	CMOS INV.	1326	897	886	2671	1844	1815	5367	3749	3690
2-4LPI	134	102	106	271	209	216	547	422	438	4-16LPI	1328	940	931	2669	1906	1887	5356	3846	3809
2-4HPI	133	102	105	269	208	213	542	420	430	4-16HPI	1203	849	839	2415	1723	1702	4844	3479	3438

Table IV:Power Delay Product Results

Table V:Propagation Delay Results

2-4 DEC.	0.8V	1.0V	1.2V	4-16 DEC.	0.8V	1.0V	1.2V
CMOS	105	49	33	**CMOS**	214	97	66
2-4LP	132	62	43	**4-16LP**	203	93	64
2-4HP	99	47	33	**4-16HP**	195	88	59
CMOS INV	100	48	34	**CMOS INV.**	252	108	71
2-4LPI	89	43	30	**4-16LPI**	270	119	79
2-4HPI	87	42	29	**4-16HPI**	243	107	71

Table III tells about the power dissipation of all decoders in which LP represents low power, HP represents high performance,LPI represents low power inverter,HPI represents high performance inverter.Table IV tells about the power Delay product(PDP) of all decoders.Table V tells about the propagation-delay of all decoders,it tells which one is efficient.

VI.CONCLUSION

By compairing the existing system simulation results with proposed system.From results,2-4 LP gives 9.3% less power dissipation,26.7% propagation delay ,15.7% power delay product than CMOS 20T. on the opposite hand, 2-4 HP outperforms CMOS 20T altogether aspects,reducing power ,propagation delay and PDP by 8.2%,4.3% and 15.7% respectively.Both of our inverting designs,2-4 LPI and 2-4 HPI outperform CMOS 20T inv.Altogether aspects ,as well specifically,2-4 LPI reduces power Propagation delay and Power delay product by 13.3%,11% and 25% respectively. While 2-4 HPI gives 11.2%,13.2% and 25.7%. According to 4-16 simulations, the obtained results are similar.The 4-16 LPI decoder, which uses the slower 2-4 LP as predecoder gives 6.4% lower power dissipation with the value of 17.9% propagation delay and 1.9% higher power delay product than CMOS 104T. The remaining decoders, namely 4-16LP,4-16HP and 4-16HPI present better results than corresponding CMOS decoders Altogether cases, which may be summarised as:7.4%,6.5% and 6.0% lower power,4.5%,9.3% and 2.3% lower delay and 11.1%,15.3% and 7.9% lower PDP respectively.

A variety of comparitive spice simulations was performed at the 32 nm, verifying in most cases, a particular advantage in favour of the proposed designs.The 2-4 LP and 4-16 LPI topologies are mostly suitable for applications where area and power minimization of primary concern.The 2-4 LPI,2-4 HP and 2-4 HPI also because the corresponding 4-16 topologies proved to be viable and all -around efficient designs, thus they will effectively be used as building blocks with in the design of larger decoders,multiplexers and other combinational circuits of varying performance requirements.Moreover,the presented reduced Transistor count and low power characteristics can benefit both bulk CMOS and SOI design also.The obtained circuits are to be implemented on layout level, making them suitable for normal cell libraries and RTL design.

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