Based on SK-LC Technique Energy Efficient in SRAM Architecture

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Abstract: **In many VLSI chips, Static Random Access memory (SRAM) has become an important part due to their large storage capacity and small access time. Low power adequate memory design is one of the most challenging issues in SRAM architecture. As the technology node scaling down, leakage power consumption has become a significant problem. There are various power gating schemes available in the literature such as sleep technique, stack technique, sleepy stack technique, sleepy keeper technique, lector technique, foot switch technique and double switch technique for leakage power reduction. In this paper, the design is carried out for an efficient SRAM cell and Sense Amplifier using a novel power gating technique namely sleepy keeper leakage control transistor technique (SK-LCT) which can be used in various application such as PC, Personal Communications, Consumer Electronics and other fields. The proposed SK-LCT technique is applied in both SRAM cell and sense amplifier for a new low power high speed SRAM architecture design. The Simulation is done using MICROWIND tool and the results obtained show a significant improvement in leakage power consumption and speed. Further the Designs are modified by Dual Sleepy Stacked LECTOR SRAM which had shown further enhancement in the results obtained.**

***Index Terms*: Address decoder, Leakage, Sense amplifier, SRAM, Sleepy Keeper transistor**

1. INTRODUCTION

Very Large Scale Integration is the process of integrating a million of transistors within a single chip. Rapid growth in VLSI fabrication process results in the increase of densities of the integrated circuit by scaling down the technology [1]. With the advancement in technology that are happening in the world, the demand for large storage of data is increasing in a way that needs to be faster than the existing technologies [2]. Also, another concern is about large power dissipation especially during accessing a memory in a computing system [3].

Static Random Access Memory (SRAM) is majorly used in hand held devices, System On-Chip (SoC) & high performance VLSI circuits which often consumes a dominant portion of power in each chip. Due to the quadratic relation between power and supply voltage of transistors [4]; the power consumption can be effectively reduced by decreasing the supply voltage. Owing to high bit-line swing requirement, the leakage power consumption of memory circuit during a write operation is high. The techniques like power gating technique, Sleep technique, Stack technique, Sleepy stack technique, Sleepy keeper technique, LECTOR technique, Foot switch technique & Double switch technique are some of the commonly used techniques for leakage power reduction.

K.S.S.K. Rajesh, S. Hari Hara Subramani and V. Elamaran reduced the length of the transistors to overcome the challenge of circuit area and power. Since the battery technology does not grow rapidly, still people are forced to use such a large size batteries in the system to operate as the reduction in size of battery involves risk factors like being highly explosive. Hence the designers have the choice of consuming low power. Complementary Metal Oxide Semiconductor (CMOS) logic styles are much popular for dissipating less energy or low power. They used alternative CMOS logic for 8-bit comparator logic circuits like conventional CMOS, Dynamic CMOS and Domino CMOS. Using single-bit comparator design, the higher order comparator designs are developed for usage in data path module of a processor based systems.

Manjith Ramaswamy adopted a low power adequate memory configuration by using sleepy keeper leakage control transistor technique (SK-LCT) for a handheld gadget applications. The SK-LCT technique is applied in both SRAM cell and sense amplifier for a new low power high speed SRAM architecture design. The outline of SRAM architecture utilizing pass transistor decoder (PT-Decoder) gives better outcomes in term of power. At 100 nm barrier, the CMOS transistor ceases to be a virtually ideal switch consuming power only when changing state. The leakage power is proportional to the total number of transistors on chip as reported in the ITRS Roadmap, transistors devoted to memory structures in a typical microprocessor-based system is about 70% today and it is expected to rise to 80% in the near future [1]. Also the temperature dependence of some sources of leakage power.

This paper is organized as introduction to design of SRAM and its architecture in section I, Existing Design in section II, power gating techniques in section - III and proposed design i.e., SK-LCT Technique in section-IV. The results are discussed in section -V and finally the paper is concluded.

2. EXISTING SYSTEM

The SRAM Architecture consists of SRAM cell, sense amplifier, pre-charge circuit, row/ column decoder and write driver circuit. Fig.1 shows the block diagram of SRAM Architecture, where the decoder (row decoder/ column decoder) translates the binary address into unary address exactly only one word in the array is selected. The memory

location within the memory devices are selected by the address inputs of the decoder. The data I/O connection is the path in which data are entered for storage and extracted for reading. The bit lines (BL & BLB) are read by sense circuitry that sense the value of the bit lines; amplify it to speed it up and restore the signal to the proper voltage levels.

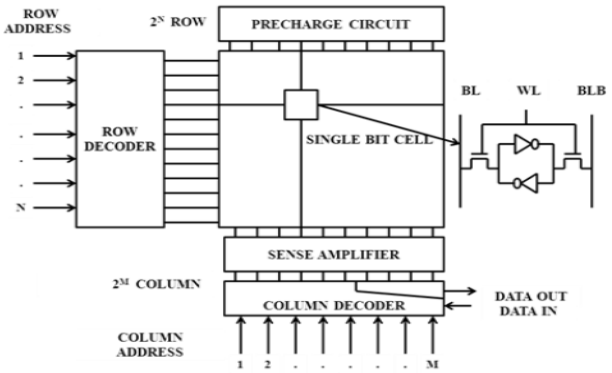


Fig.1: SRAM Architecture

SRAM can be word oriented or bit oriented. In word oriented memory, each address accesses a word of n bits whereas in bit oriented memory, each address accesses a single bit, where SRAM cells are arranged in an array of horizontal row and vertical column. In array architecture, there are 2N rows that are called as word lines and 2M columns that are called as bit lines. So, the total number of memory cells in the array is 2 (N+M). For fast read and write operation separate write driver circuit and sense amplifier dedicated to each column.

The SRAM cell uses a bi-stable latching circuitry to store one bit binary information. The memory cell has two stable states which are denoted as „1" & „0". During read and write operation, two additional NMOS transistors control the access to the storage cell. The conventional SRAM cell uses six MOSFET to store data in memory as shown in Fig.2

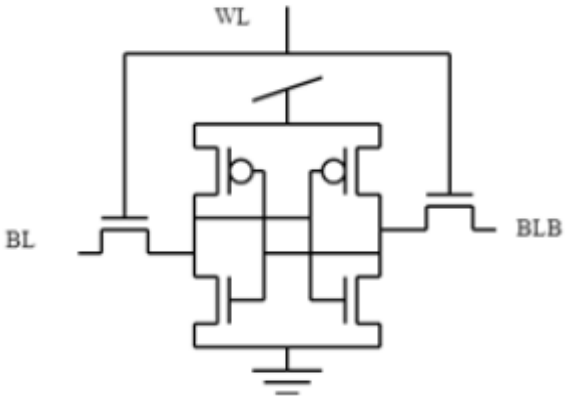


Fig.2: SRAM cell

The Sense amplifier is the part of read circuitry that is used to read the data from the SRAM Architecture; its role is to sense the low power signals from the bit lines (BL&BLB) and amplify the small voltage to decipherable logic levels so that the data obtained can be interpreted properly in SRAM array. Fig.3 shows the Differential sense amplifier.

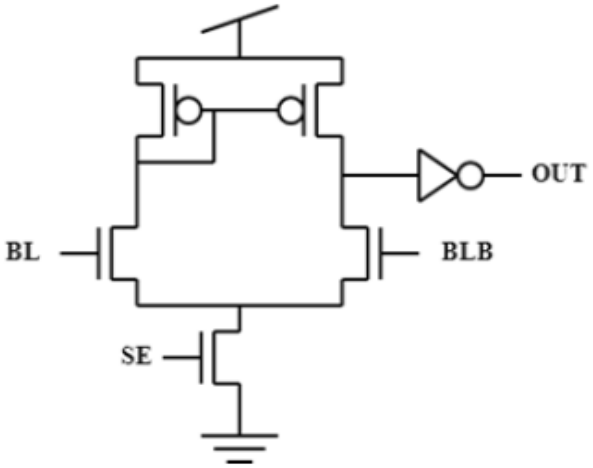


Fig.3: Differential Sense Amplifier

The Pre-charge circuit consists of three PMOS transistors. Two upper transistors are used for pre-charging and the lower one is used for equalization. Before the read and write operation, pre-charge circuit is used to pre-charge both bit lines (BL & BLB) to VDD. Each column has a single pre-charge circuit in the memory array. The Fig.4 shows the Pre-charge circuit.

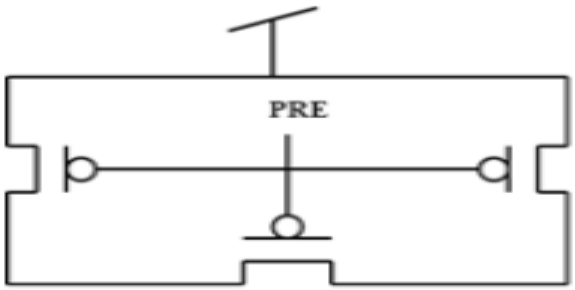


Fig.4: Precharge circuit

The write driver circuit is used to discharge any one of the bit lines (BL & BLB) from precharge level. It is enabled by a write enable (WE) circuitry. In the each column of memory array, only one write driver circuit is required. The WE signal is turned on; when the write operation is intended. Otherwise, the WE signal isolates the bit lines from write drivers.

In memory design, the decoder is used to decode the given address and enable the particular row or column of the memory array. Row and column decoder is used to enable Word Line (WL) and Write Enable (WE) of a SRAM array. Based on the address line, particular memory cell is chosen and the data is read and written in the memory array.

3. POWER GATING TECHNIQUES

Power gating technique is most commonly used integrated circuit design to reduce the leakage power, by shutting off the current to blocks of the circuit that are not in use. An externally switched power supply is used to achieve the static power reduction, which is the basic form of power gating. During standby mode, most of the power is wasted in SRAM cell; because leakage power plays a predominant role in SRAM power consumption. The various power gating techniques are available in literature to shrink the static power of memory cell. In sleep technique, "sleep S" PMOS transistor

is inserted between VDD & pull up network and "sleep S BAR" NMOS transistor is inserted between the pull down network & ground. The wake up time of the sleep technique has a considerable impact on the competence of the circuit [5]. Stack technique is state maintenance technique with the disadvantage of increased delay and area [6]. The divided transistor of sleepy stack technique increases the delay drastically & also limits the convenience of this technique [7]. In Sleepy Keeper Technique parallel connected PMOS and NMOS transistor is placed between pull up network & VDD and pull down network & ground. LECTOR technique has two leakage control transistors (LCT1 &LCT2) which are inserted between the pull up & pull down network. It has a very low leakage power which results in a delay penalty [8]. The data retention problem occurs in the circuit, which can be minimized by placing sleep transistor [9]. There is a need of a new power gating technique to overcome the disadvantages of the above existing techniques. Sense Amplifier is one of the critical parts in the memory. The performance of sense amplifier strongly affects both memory access time and overall memory power dissipation. Improper design of the amplifier circuitry affects the robustness of the memory device. In order to reduce static power & delay of Sense Amplifier; Latch-type Sense Amplifier is designed using Foot switch Technique & Double switch Technique.

The Footer Switch Voltage Latch Sense Amplifier (FS-VLSA) senses the voltage difference (ΔVBL) between bit line voltage (VBL) & bit line bar voltage (VBLB) and amplifies it to rail output voltages. The Footer Switch Current Latch Sense Amplifier (FS-CLSA) senses the current difference produced by ΔVBL and amplifies it. By inserting an additional head switch (i.e. Double Switch PMOS Access & Double Switch NMOS Access) the invalid current paths in FS-VLSA can be removed which introducing a complementary sense enable signal. The sensing dead zone can be completely removed using Double Switch Transmission Access-Voltage Latch Sense Amplifier (DSTA-VLSA) [10].

4. PROPOSED DESIGN

SLEEPY KEEPER LEAKAGE CONTROL TRANSISTOR TECHNIQUE (SK-LCT TECHNIQUE) FOR LOW POWER HIGH SPEED SRAM ARCHITECTURE is used.

The SK-LCT Technique is the combination of both Sleepy Keeper and LECTOR Technique. The delay & power of the SRAM Architecture can be further reduced and the data retention can be maintained using this novel technique.

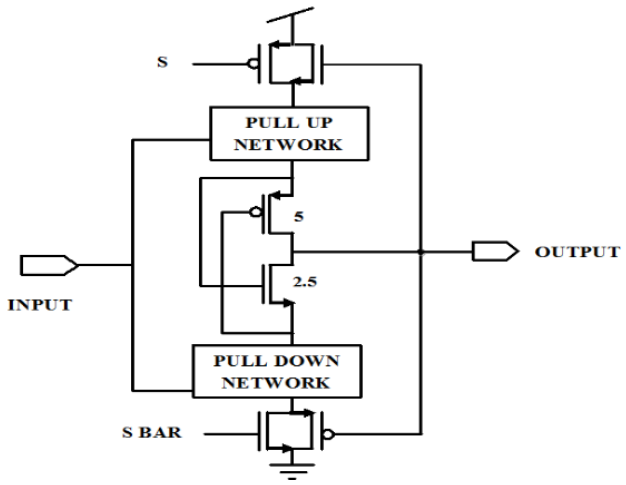


Fig.5: SK-LCT Technique

Fig.5 shows the SK-LCT Technique. Here, leakage control transistor (LCT-PMOS & LCT-NMOS) is placed in between pull up & pull down network. Both PMOS and NMOS are tied up parallel to preserve the stable retention in standby mode. LCT- PMOS gate is connected to the drain of pull down network and LCT-NMOS gate is connected to the drain of pull up network. Here, the sleep PMOS(S) transistor is placed below VDD and sleep NMOS (S BAR) transistor is placed above ground. In sleep mode, parallel connected NMOS is the only terminal between pull up network & VDD and parallel connected PMOS is the only terminal between pull down network & ground. The SRAM cell and Sense Amplifier are the two main peripheral components of SRAM Architecture; by the optimized design of these two components using this SK-LCT technique low power & high speed memory architecture can be obtained.

Fig.6 shows the Block Diagram of SRAM Architecture using SK-LCT Technique. Initially, precharge both the bit lines (BL & BLB) by using Precharge circuit. By enabling the word line (WL) of the SRAM cell, the data either „0" or „1" is stored. If data „1" is written in SRAM cell, BLB automatically discharges to „0" & BL remains high and vice-versa. Sense Amplifier boosts the data in SRAM cell and acts as a read part circuitry. No change in the memory cell takes place during hold operation.

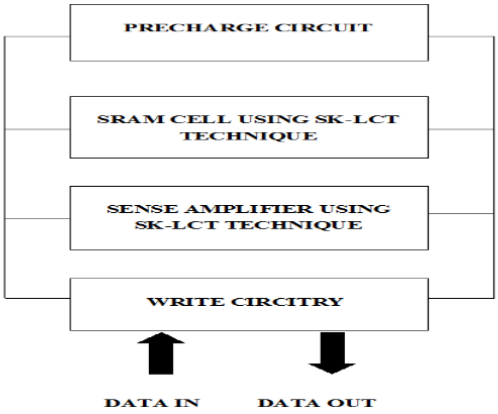


Fig.6: SRAM Architecture using SK-LCT Technique

Table 1: Read and Write Operation of SRAM cell

WRITE OPERATION		READ OPERATION	
WRITE '1'	Q=0, Q-bar=1 Word Line=1 Bit bar=0 Bit =1	READ '1'	Precharge both the Bit lines Word line=1 Bit bar=0(discharges to 0) Bit=1
WRITE '0'	Q=1, Q-bar=0 Word Line=1 Bit bar=1 Bit =0	READ '0'	Precharge both the Bit lines Word line=1 Bit bar=1 Bit =0(discharges to 0)

Table 1 show the read and write operation of SRAM cell. When Word Line (WL) and Write enable circuitry (WE) is enabled, previous data is modified and new data is written in the memory cell. When either Word Line (WL) or Write enable circuitry (WE) is disabled, the previous data is hold in the memory cell. No change in the memory cell takes place during hold operation

The SRAM cell is designed using SK-LCT Technique to reduce the leakage power dissipation of memory. Fig.7 shows SRAM cell using SK-LCT Technique. When word line (WL) is asserted high, access transistors are turned „ON" for write operation. This connects the cell to two complementary bit lines columns (BL &BLB) and the data either „1" or „0" is written in the memory cell. When WL=0, SRAM cell is being inaccessible from both bit lines; keeping it in standby mode. This keeps prior stored value in the cell unchanged.

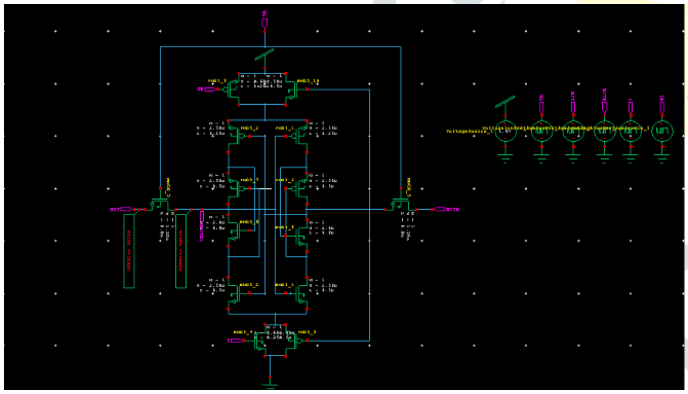


Fig.7: SRAM cell using SK-LCT Technique

The power and delay of the Voltage Latch Sense Amplifier (VLSA) is reduced using SK-LCT Technique. Here, additional transmission access transistor is inserted along with bit lines (BL & BLB). During read mode, the PMOS sleep transistor is set to „1" and the NMOS sleep transistor is set to „0"; thus turning on the transmission gate and switching off the PMOS transistor whereas in standby mode the transmission gate is turned off and PMOS transistor turns on. Fig.8 shows latch type sense amplifier using SK-LCT Technique.

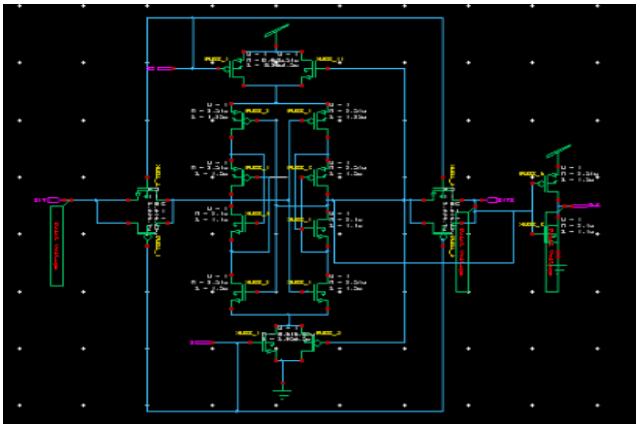


Fig.8: Sense Amplifier using SK-LCT Technique

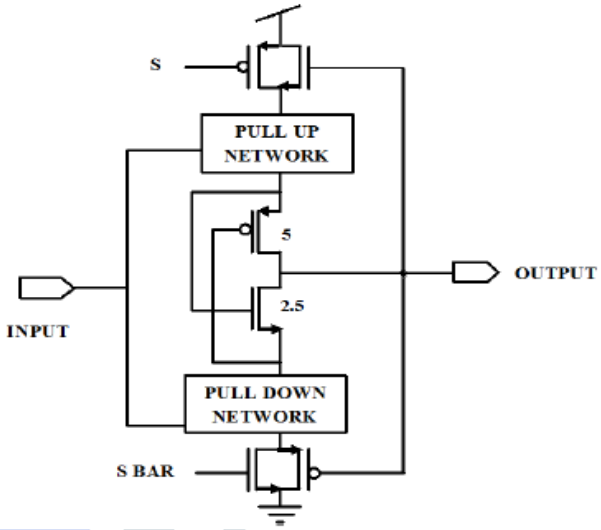


Fig.9 (a)

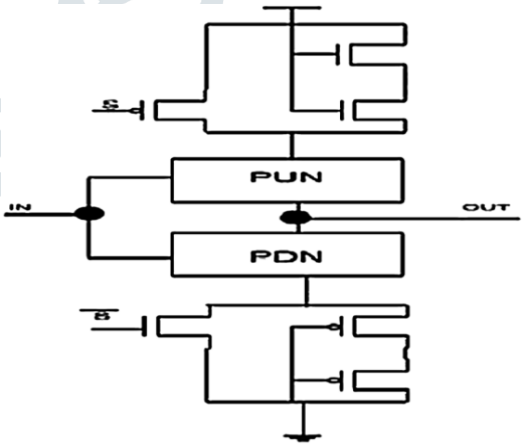


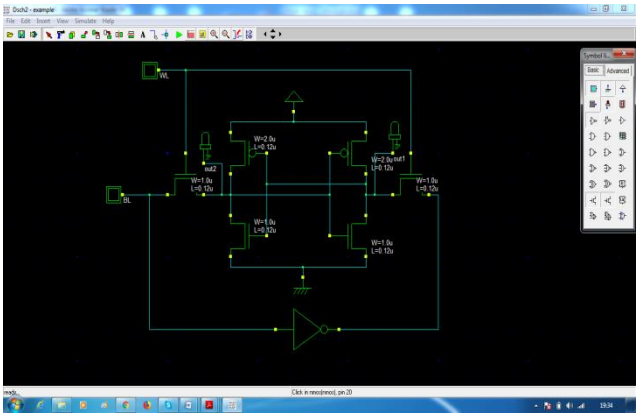
Fig.9. (b)

Fig.9: Proposed Dual Sleepy Stacked LECTOR SRAM

The top and bottom transistor sets are changed to dual stack to avoid ground bounce noise as shown in fig.9. It combines the advantages of both dual sleepy stacked design and LECTOR techniques.

5. SIMULATION RESULTS

The designs are developed in Digital Schematic, where their functional verification is performed. Also the corresponding Layouts are developed in 120nm technology and are simulated.



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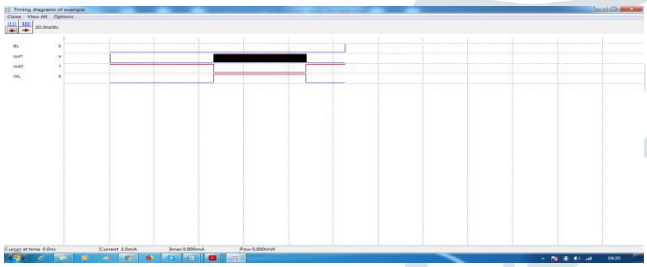
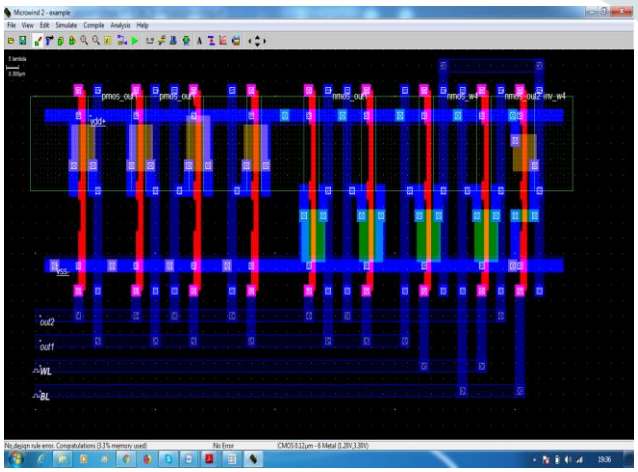


(b)

Fig.10: The schematic and the corresponding functional simulation of existing SRAm design.

The figure 10 shows the design of SRAM in digital schematic and the functional verification of the SRAM Design where the outputs are represented by out1 as q and out2 as qb.

The layout of the schematic developed for existing design is shown in figure 11 (a). this layout is developed in 120nm and the corresponding waveforms are simulated as shown in figure 11(b).



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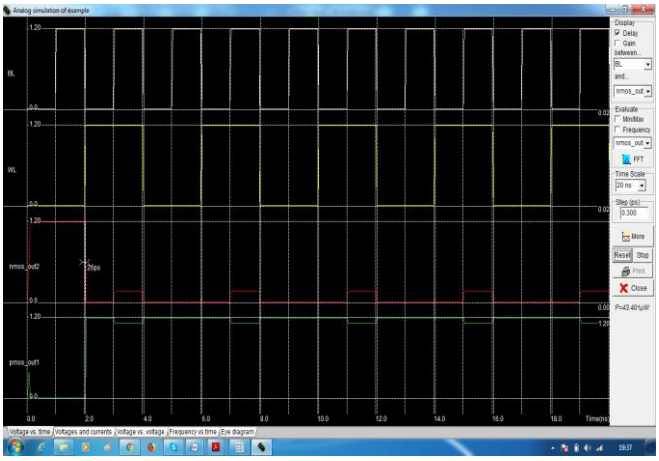
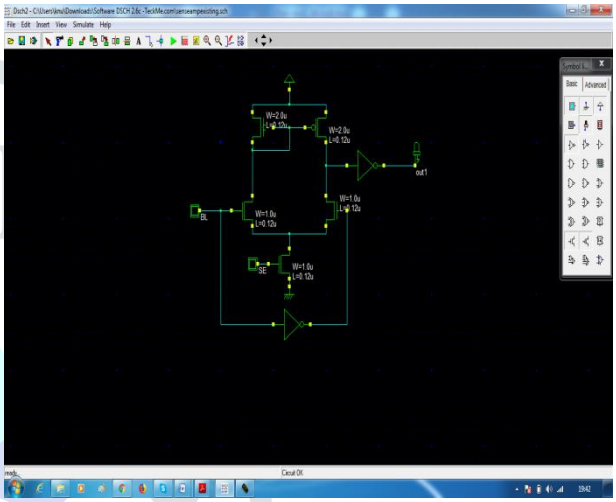


Fig.11: The layout and simulation waveform of the existing SRAM design for the schematic shown in fig.10.



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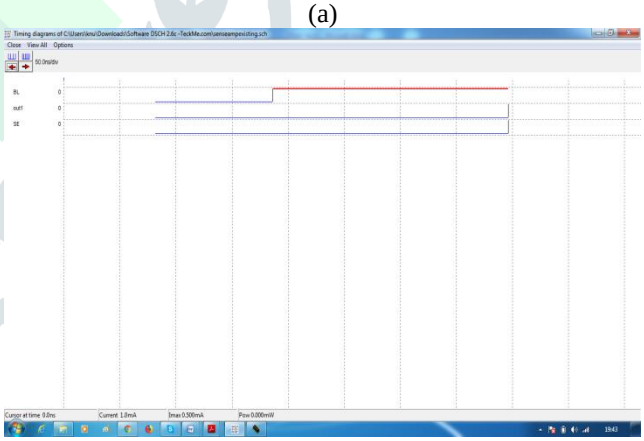
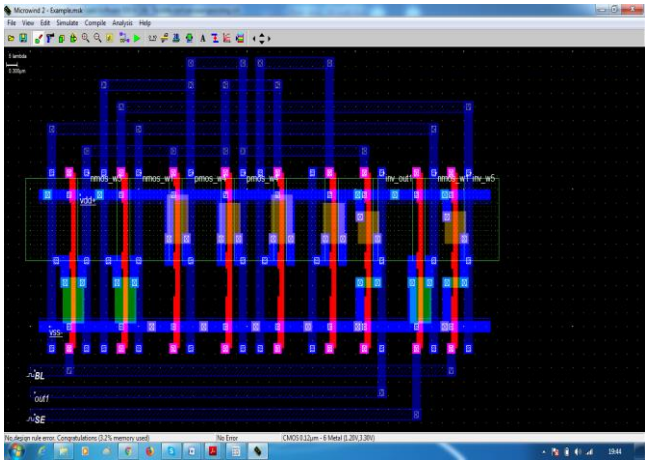


(b)

Fig.12: The schematic and the corresponding functional simulation of existing sense amplifier design.

The figure 12 shows the design of Sense Amplifier in digital schematic and the functional verification of the Sense Amplifier Design where the output is represented by out1. The layout of the schematic developed for existing sense amplifier design is shown in figure 13 (a). this layout is developed in 120nm and the corresponding waveforms are simulated as shown in figure 13 (b).



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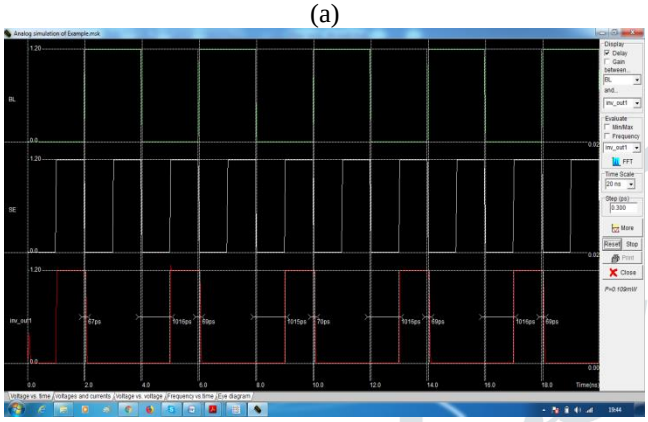

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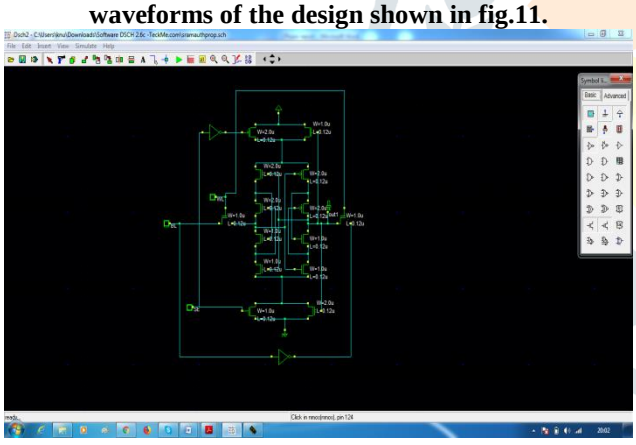
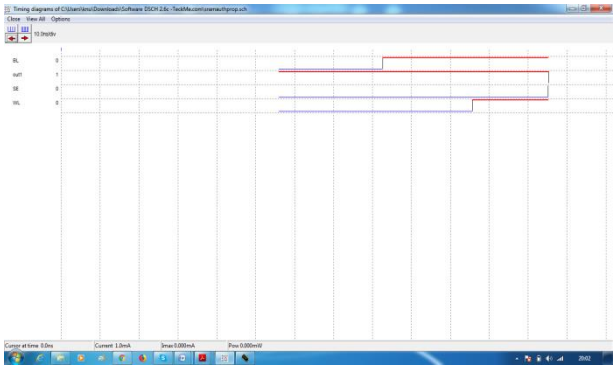
Fig.13: The layout and the corresponding simulation waveforms of the design shown in fig.11.



(a)

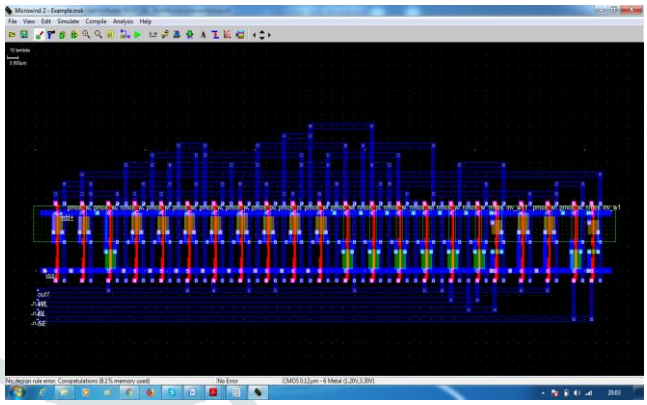


(b)

Fig.14: The schematic and the corresponding functional simulation of existing SRAM design-2.

The figure 14 shows the design of SRAM in alternative form by using digital schematic and the functional verification of the SRAM Design where the outputs is represented by out1.

The layout of the schematic developed for existing design - 2 is shown in figure 15 (a). this layout is developed in 120nm and the corresponding waveforms are simulated as shown in figure 15 (b).



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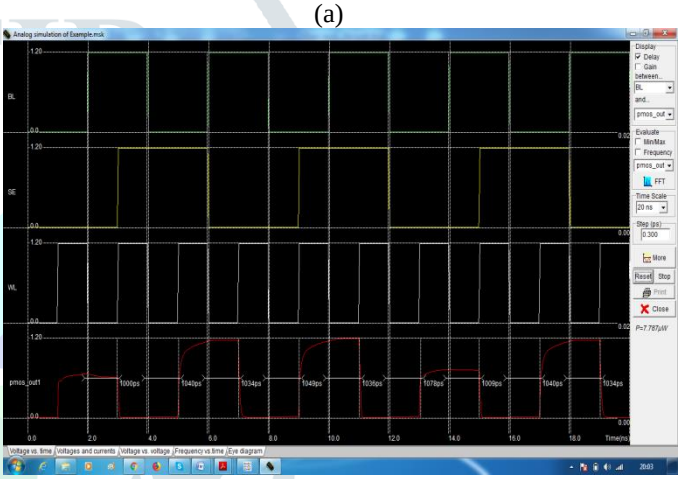

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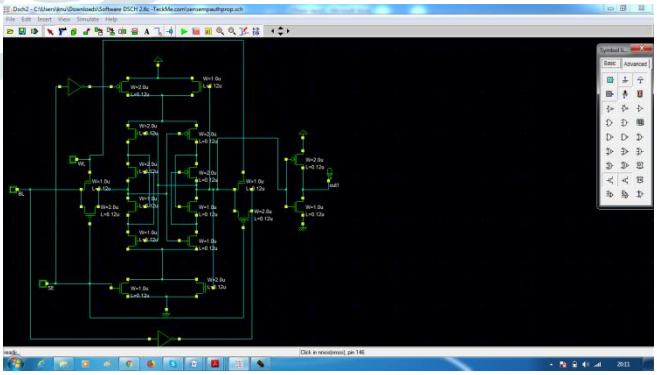
Fig.15: The layout and the corresponding simulation waveforms of the design shown in fig.13.



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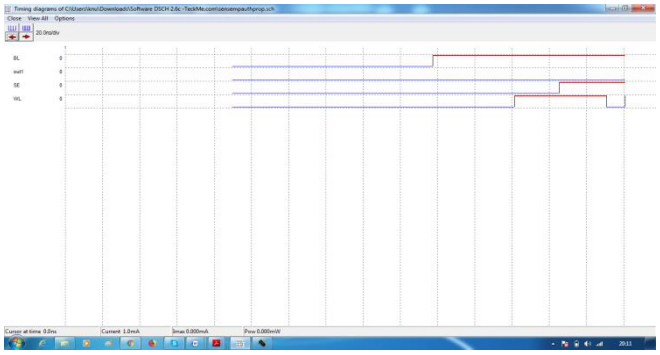
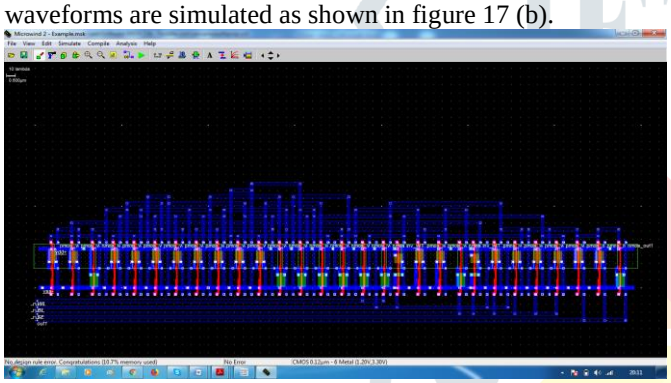


(b)

Fig.16: The schematic and the corresponding functional simulation of existing sense amplifier design-2.

The figure 16 shows the design of Sense Amplifier in alternative form by using digital schematic and the functional verification of the Sense Amplifier Design where the outputs is represented by out1.

The layout of the schematic developed for existing Sense Amplifier design - 2 is shown in figure 17 (a). this layout is developed in 120nm and the corresponding waveforms are simulated as shown in figure 17 (b).



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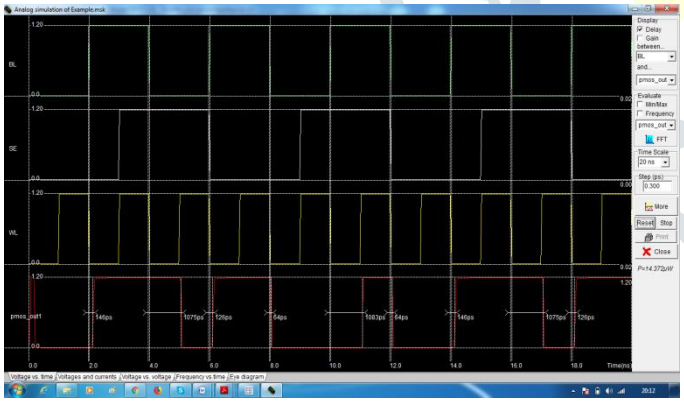
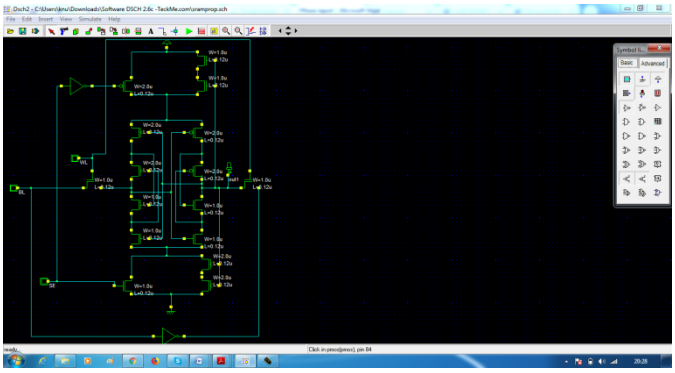


(b)

Fig.17: The layout and the corresponding functional simulation of existing sense amplifier design-2shown in fig.15 .

The figure 18 shows the design of proposed SRAM by using digital schematic and the functional verification of the Proposed SRAM Design where the outputs is represented by out1.



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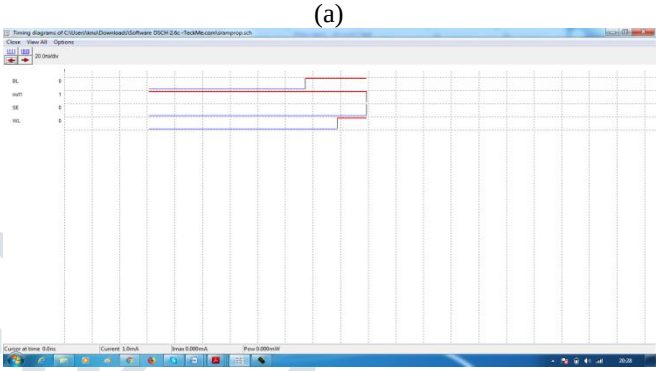
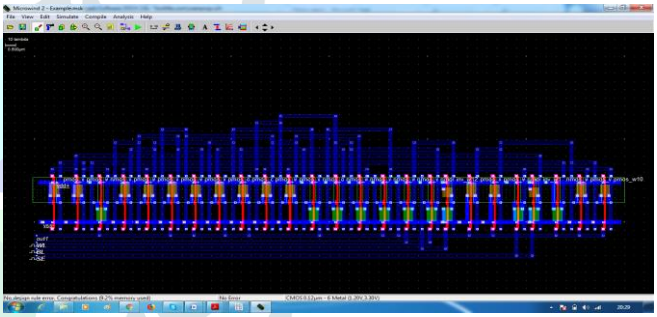


(b)

Fig. 18: The schematic and the corresponding functional simulation of Proposed SRAM design.



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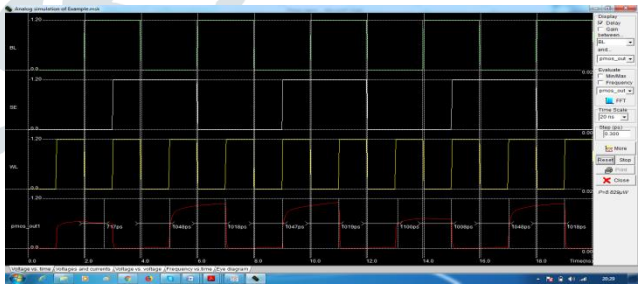
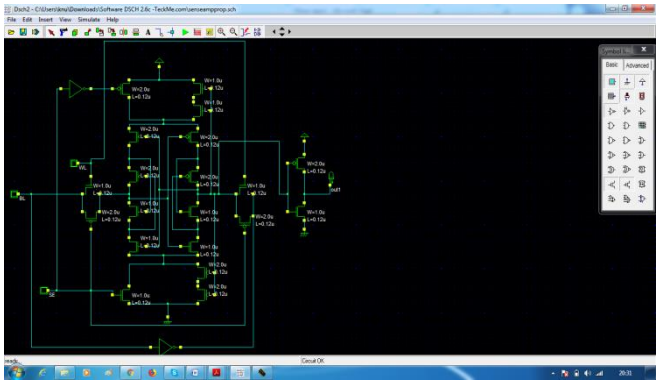


(b)

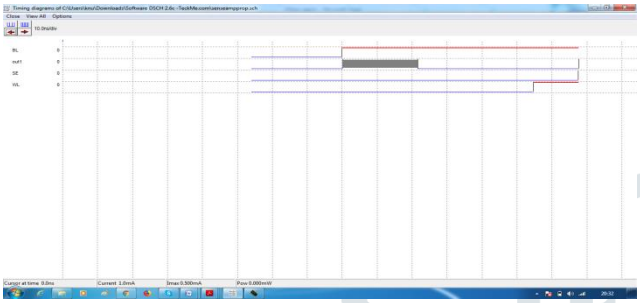
Fig.19: The layout and the corresponding simulated waveforms of design shown in fig.18.

The layout of the schematic developed for proposed SRAM design is shown in figure 19 (a). this layout is developed in 120nm and the corresponding waveforms are simulated as shown in figure 19 (b).

The figure 20 shows the design of proposed Sense Amplifier by using digital schematic and the functional verification of the Proposed Sense Amplifier Design where the outputs is represented by out1.

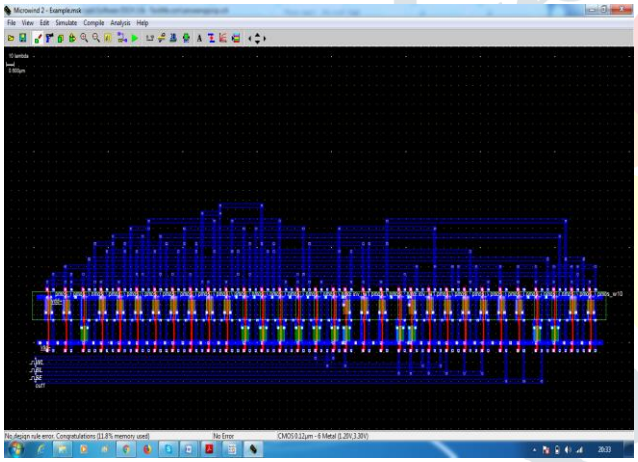


(a)

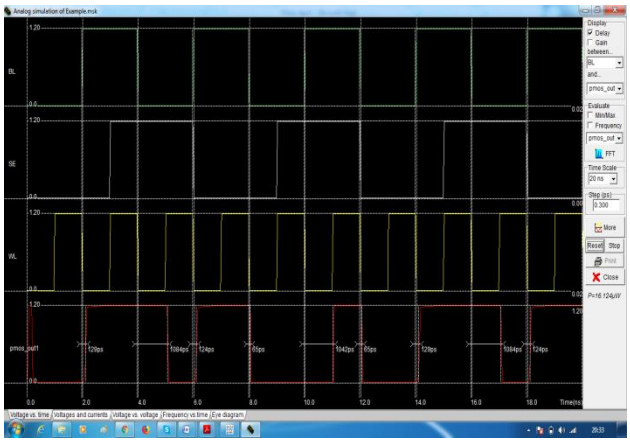


(b)

Fig.20: The schematic and the corresponding functional simulation of Proposed Sense Amplifier design.



(a)



(b)

Fig.21: The layout and the corresponding simulated waveforms of design shown in fig.20.

The layout of the schematic developed for proposed Sense Amplifier design is shown in figure 21 (a). this layout is developed in 120nm and the corresponding waveforms are simulated as shown in figure 21 (b).

Table .I: Comparison Table

Parameters	SRAM Existing Design -1	SRAM Existing Design - 2	SRAM Proposed Design
Area Occupied	3.3%	8.1%	9.2%
Power Dissipated	43.401µW	7.787µW	8.8829µW
Rise Time	0	1040pS	1042pS
Fall Time	26Ps	1000pS	1019pS
Output	Acceptable	Distorted	Acceptable
Effect of Noise	Exists	Controlled to Some Extent	Controlled to an cceptable level

Table 2: Comparison of various Sense Amplifier Designs

Parameters	Sense Amplifier Existing	Sense Amplifier Author Proposed	Sense Amplifier Proposed
Area Occupied	3.2%	10.7%	11.8%
Power Dissipated	0.109mW	14.372µW	16.124µW
Rise Time	1016pS	126pS	124pS
Fall Time	69pS	64pS	65pS
Output	Acceptable	Distorted	Acceptable
Effect of Noise	Exists	Controlled to Some Extent	Controlled to an cceptable level

From the tables 1 and 2, The proposed designs i.e., the design of SRAM and Sense Amplifier using Dual Stacked LECTOR SRAM and Sense Amplifier reduce the ground bounce noise to an acceptable level with slight tradeoff in power dissipation and area occupied.

5. CONCLUSION

A Low power and high speed SRAM architecture is designed using sleepy keeper leakage control transistor technique (SK-LCT). The two main components of the SRAM architecture are SRAM cell and Sense Amplifier which are designed using SK-LCT technique for new low power high speed memory architecture. In this paper, the designs are developed by using the Dual Staked LECTOR SRAM technique which proves to be efficient design particularly for the SRAM and Sense Amplifier Architecture which can be used in various application such as PC, Personal Communications, Consumer Electronics and other fields.

REFERENCES

[1]. Andrea Calimera, Alberto Macii, Enrico Macii & Massimo Poncino (2012), "Design Techniques and Architectures for Low-Leakage SRAMs", IEEE Transactions on Circuits and Systems, Vol. 59, No. 9 , Sep 2012, pp.1992-2007

[2]. Yeap G. K. et al (1998), "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers", Norwell, MA, ISBN: 0792380096, pp-233.

[3]. F. Catthoor, S. Wuytack, E.DeGreef (1998), "Custom Memory Management Methodology Exploration of Memory Organization for Embedded Multimedia System Design", Kluer Acadamic Publishers, Boston.

[4]. J. M. Rabaey, A.P. Chandrakasan (2003), "Digital Integrated Circuits: A Design Perspective", Upper Saddle River, NJ, USA: Prentice-Hall.

[5]. Hina Malviya and Sudha Nayar (2013), "A new Approach for Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS circuit for VLSI Application", IEEE Int. Solid State Circuits Conf. (ISSCC) Dig. Tech, Vol.3 Mar 2013, pp. 11–16.

[6]. Anu Tonk and Shilpa Goyal (2015), "A Literature Review on Leakage and Power Reduction Techniques in CMOS VLSI Design", International Journal of Advanced Research in Computer and Communication Engineering, Vol.3, Issue.2, pp.554-558.

[7]. J. Park (2014), "Sleepy Stack: a New Approach to Low Power VLSI and Memory", Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, May 2014.

[8]. Narender Hanchate (2011), "LECTOR: A Technique for Leakage Reduction in CMOS Circuits", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol.12, No. 2, Feb 2011, pp.198-205

[9]. M. Geetha Priya, Dr. K. Baskaran and D. Krishnaveni (2012), "Leakage Power Reduction Technique in Deep Submicron Technologies for VLSI Applications", Elsevier-Sciverse Science Direct, Procedia Engineering, Vol. 30, Dec 2012, pp.1163-1170

[10]. Taehui Na, Seung-Han Woo, Jisu Kimg, Hanwool Jeon, and Seong-Ook Jung(2013), "Comparative Study of Various Latch-Type Sense Amplifiers", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 12, No. 6, Sep 2013, pp.1-5