Design and Implementation of Carry Skip Adder based on low power Techniques

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Abstract— This paper proposes a new method for implementing a low power and high speed Carry Skip Adder by means of a set of Gate Diffusion Input (GDI) cell-based multiplexers. Full adder is a very common example of combinational circuits and is used widely in Application Specific Integrated Circuits (ASICs). It is always advantageous to have low power action for the sub components used in VLSI chips. The explored technique of realization achieves a low power high speed design for a widely used subcomponent- full adder. Simulated outcome using state-of-art simulation tool shows finer behavioural performance of the projected method over general CMOS based Carry Skip Adder. Power, speed and area comparison between conventional and proposed Carry Skip Adder is also presented. It is founded that power dissipation is major problem in the electronics device so the goal of this project is to analyse and compare the performance of Carry skip adder using NMOS pass transistor logic configuration and the logic we used in this paper is NMOS pass transistor the configuration in terms of power dissipation, area, and delay. The paper also signifies more than 50% decrement in interconnect length, area, and number of transistor count while using a pass transistor logic in comparison of 4-bit carry skip adder with a CMOS logic configuration.

Keywords: Low power full adder, 2-Transistor GDI MUX, ASIC (Application Specific Integrated Circuit), 12-TFA, CMOS (Complementary Metal Oxide Semiconductor), Carry Skip Adder, NMOS pass transistor logic, power dissipation, area, delay.

I.INTRODUCTION

Addition is one of the common and widely used fundamental arithmetic operation in many VLSI systems. Other similar arithmetic operations are subtraction, multiplication, division, address calculation etc. Using binary adders the full adder is designed and improving 1-bit full adder performance plays an important role in VLSI. Different varieties of full adders exploit completely different logic designs and technologies, which are unremarkably aim at increasing speed and reducing power dissipation. To improve the performance of adder there we have two methods. One is 'System Level viewpoint' method and second method is critical Style view point'. In system level viewpoint it consists of finding the longest signal path in the ripple adders and reduce the trail so as to scale back the full signal path delay. The longest signal path is where the carry out bit of the most significant bit has to be calculated in most things. The second method is 'Circuit Style Viewpoint' in transistor level, that is, semiconductor device level design skills are supported by designing of high performance full adder.

II. EXISTED TECHNIQUE

2.1 BINARY ADDERS

Adder circuit is a combinational digital circuit that is used for adding two numbers. A typical adder circuit produces a sum bit (denoted by S) and a carry bit (denoted by C) as the output. Typically adders are realized for adding binary numbers but they can be also realized for adding other formats like BCD (binary coded decimal, XS-3 etc. Besides addition, adder circuits can be used for a lot of other applications in digital electronics like address decoding, table index calculation etc. Adder circuits are of two type:

- Half Adder
- Full Adder

2.1.1 Half Adder

Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. From this it is clear that a half adder circuit can be easily constructed using one X-OR gate and one AND gate.

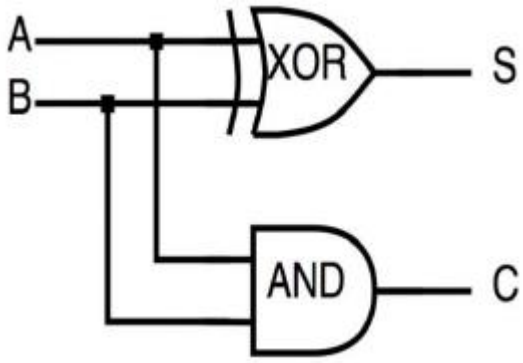


Figure: 1 logic design of half adder

2.1.2 Full Adder

One way to implement the full adder circuit is to take the logic equation and equation and translate them directly into complementary CMOS circuit. Some logic manipulations can help to reduce the transistor count. For instance, it is advantageous to share some logic between the sum and carry –generation sub circuits, as long as this does not slow down the carry generation, which is the most critical part as stated previously. The following is an example of such as reorganized equation set:

$$SUM = A.B.Cin + CARRY\ (A + B + Cin)$$

$$CARRY = A.B + B.Cin + A.Cin$$

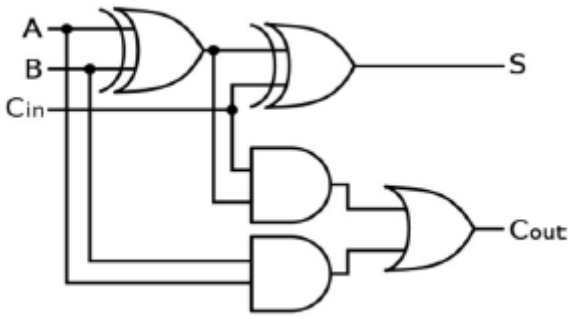


Figure 2: logic design of full adder

2.2 TRANSMISION GATE FULL ADDER

The transmission function full adder, which uses 16 transistors, for the realization of the circuit, is shown in figure 3. For this circuit there are two possible short circuits paths to ground. This design uses pull-up and pull-down logic as well as complementary pass Logic to drive the load. It gives the same delay for sum and carry. A rather different implementation of an adder uses a novel exclusive–or (XOR) gate. The schematic for this XOR gate is shown in figure 3.

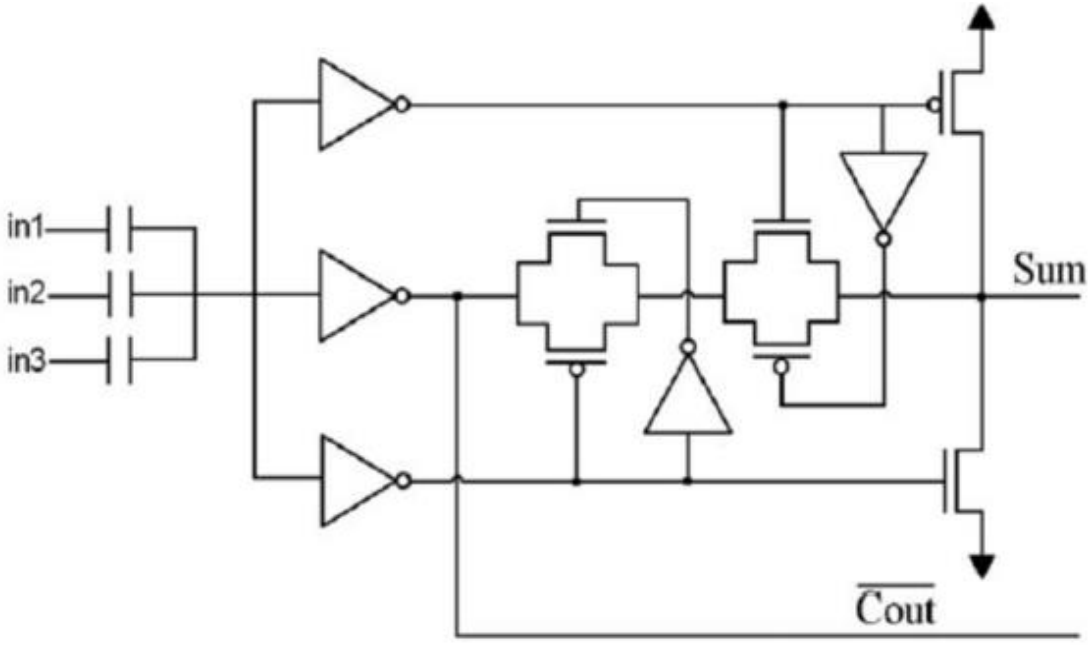


Figure 3: Transmission gate full adder

2.3 PASS TRANSISTOR LOGIC

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output.

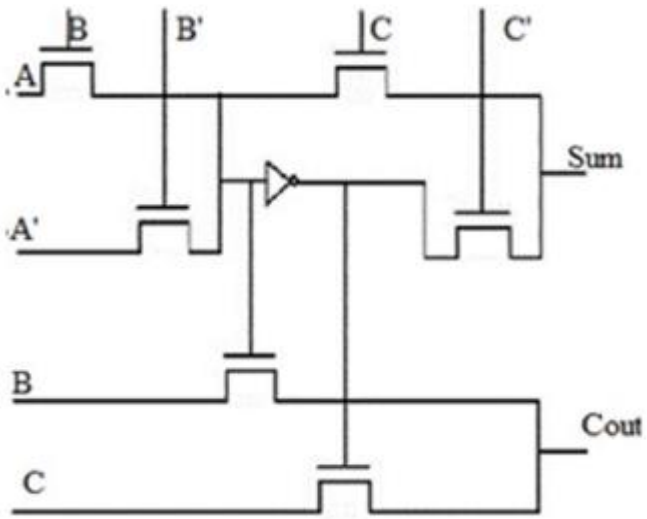


Figure 4: Pass Transistor Full Adder

III. PROPOSED GDI TECHNIQUE

The main purpose of this work is to implement a low power GDI based full adder & to draw a detailed comparative study with a CMOS full adder. The purpose of implementing the low power full adder is to show that using fewer number of transistors in comparison to the conventional full adder, the propagation delay time & power consumption gets reduced. It also helps in reducing the layout area thereby decreasing the entire size of a device where this adder is used. Power consumption is becoming the major tailback in the design of VLSI chips in modern process technologies. These are evaluated from an industrial product development perspective. It is an ultra-low power circuits my using GDI method. It is implemented and briefly discussed shown in figure .GDI-MUX design is a new approach by eliminating the use of XOR and XNOR gates.

Now we are implementing the low power full adder circuit with the help of 2T MUX, made by GDI technique. It require total 6 numbers of 2T MUX having same characteristics to design a 12T full adder and connected as above in figure.

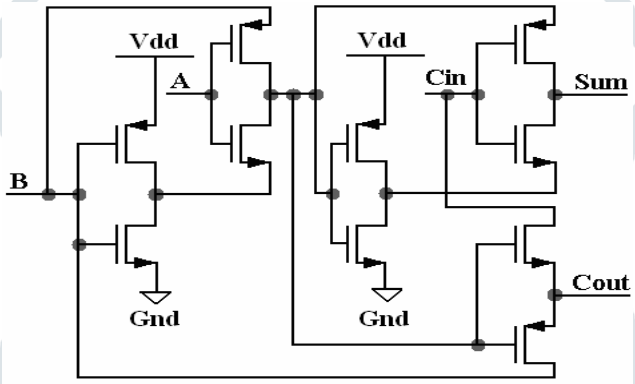
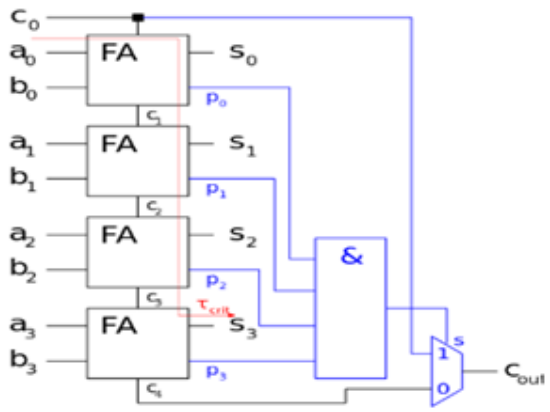


Figure 5: Logic Design for proposed GDI full adder

IV. IMPLEMENTATION of CARRY SKIP ADDER

The Carry skip adder is a skip the logic in propagation of carry and its implementation is to speed up the additional operation and to adding the propagation of carry bit around portion of entire adder. In this paper the effect of change in architecture of carry skip adder in terms' of power dissipation, area, delay, is analysed. The observed result indicates that the power dissipation, area, delay and other parameters vary with change in transistor technology. And this paper analysis the behaviour of carry skip adder in pass transistor logic and conventional CMOS logic architecture using cadence tool technology. And supply voltage 180nm and 1.8v are considered from experimental result. The result shows that carry skip adder is implemented in pass transistor logic architecture perform better then comparison to CMOS logic configuration, reference, mainly in terms of area, delay, power dissipation, and number of transistor counts.



Input Data A				Input Data B				Addition				
A4	A3	A2	A1	B4	B3	B2	B1	C	S4	S3	S2	S1
1	0	0	0	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0
1	0	1	0	1	0	1	1	1	0	0	1	0
1	1	1	0	1	1	1	1	1	1	0	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1

Figure 6: 4-Bit Carry skip adder.

V.SIMULATION RESULT

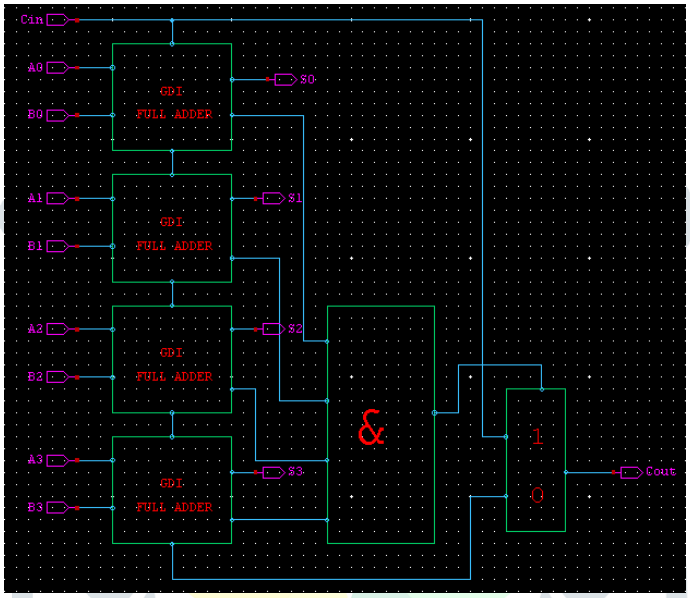


Figure 7: 4-Bit CSKA Schematic Diagram

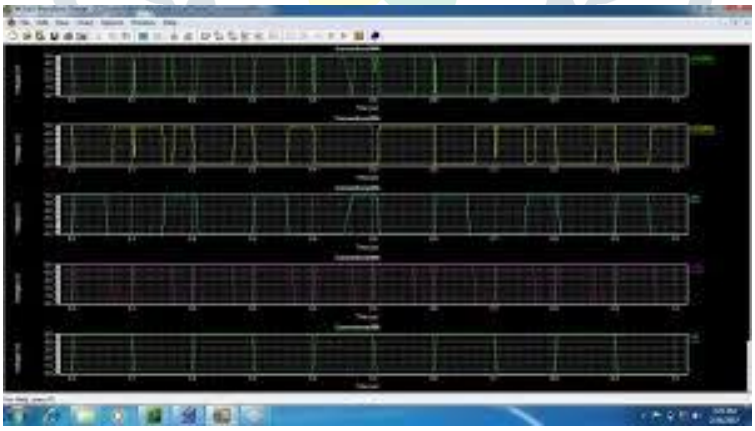


Figure 8: 4-Bit CSKA Output Waveform

Parameters	Using GDI logic	Using TG Logic
Power	289.9 µW	320.2 µW
Delay	94.46 ps	78.84 ps
Chip Area	Less	More
Transistor Count	88	136
Power Delay Product	0.062 pW	0.022 pW

V. CONCLUSION

An extensive performance analysis of modified primitive cells of AND, OR, NAND, NOR, XOR and XNOR has been presented. The performance of these GDI was analyzed in terms of transistor count, delay and power dissipation using Tanner EDA with TSMC MOSIS 250nm technology and it is compared with conventional GDI and CMOS logic. The simulation results reveal better delay and power performance of proposed primitive cells as compared to existing GDI cell and CMOS at 0.250µm technologies. Subsequently different 1-bit full-adder cells have been presented. From this analysis it is observed that the full adder cells designed with MGDI has the transistor count of 16T, 14T, 12T, 10T and 8T whereas in GDI it occupies 18T,16T, 14T, 12T and 10T, this significant change occurs due to the design of XOR and XNOR gate. In GDI the number of transistor to implement XOR will take 4 transistors whereas in modified GDI it is implemented with3 transistors. In case of CMOS the transistor count is approximately double that of MGDI adders. The performance in terms of power dissipation the pass transistor logic consumes much power when compare to MGDI, GDI and CMOS because of reduced output swings due to the threshold drop across a single-channel pass transistor. Overall the simulation results shows the modified primitive and all adder topologies has least delay, low power consumption and less transistor count when compare to existing GDI, CMOS and pass transistor logic.

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