Implementation of FIR Filters Using Low Power Multiplier and D-FlipFlop

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Abstract— In this paper, presents the application of minimize the Power, Area in CMOS VLSI circuits. The proposed FIR Filter is designed by using full adder and multiplier. The design of full adders for low power is obtained and low power units are implemented on the proposed multiplier and the results are analyzed for better performance. The FIR filters are designed in both direct form method and Transposed form method. The low power filters are simulated for linear phase. A new technique called folded filters is also designed in linear phase. The designs are done by using TANNER S-EDIT tool and simulated using T-SPICE.

Index Terms— Adder, Multiplier, FIR filter, Direct form-1, Direct form-2, D-flip flop.

I.INTRODUCTION

Recent advances in the development of portable devices requires low power used for data communication, High speed digital circuit. VLSI circuit design Deep submicron technology structure for better achievement. The design of analog circuit is very low power consumption. Now a day's VLSI design process is used for analog and digital circuit design. The low power chips are designed by technical purpose. The market is giving the important of low power electronic products. The digital chips increased device pressure, difficulty and speed and decreased power dissipation. The analysis and optimization are classification of VLSI low power design problems. The low power VLSI chips are need for arises from such evolution strength of integrated circuits. The need for low power chips are increased market request for portable consumer electronics powered by the batteries and some other factors that fuel. The low power chip and system comes from another major request for environmental contact. It is devout about the correct power of the manipulation either energy utilization at various aspect of the architecture case. For performance metrics, like faster on smaller chips it introduced a serious problem of digital energy consumption.

In the past decades, there are many papers on the designs and implementations of low-cost or high-speed FIR filters. In order to avoid costly multipliers, most prior hardware implementations of digital FIR filters can be divided into two categories: multiplier-less based and memory based. Memory-based FIR designs consist of two types of approaches: lookup table (LUT) methods and distributed arithmetic (DA) methods. The LUT-based design stores in ROMs odd multiples of the input signal to realize the constant multiplications in MCM. The DA-based approaches recursively accumulate the bit level partial results for the inner product computation in FIR filtering [1]–[2]. In [3], Hou-Jen Ko and Shen-Fu Hsiao proposed the faithfully rounded truncated multiplier design where the maximum absolute error is guaranteed to be no more than 1 unit of least position.

II.LITERATURE REVIEW

A novel full adder design using as few as ten transistors per bit. Compared with other low-gate-count full adder designs using pass transistor logic, the proposed design features lower operating voltage, higher computing speed and lower energy (power delay product) operation. The design adopts inverter buffered xor/xnor designs to alleviate the threshold voltage loss problem commonly encountered in pass transistor logic design. This problem usually prevents the full adder design from operating in low supply voltage or cascading directly without extra buffering. The proposed design successfully embeds the buffering circuit in the full adder design and the transistor count is minimized.

Also, minimizing power of the most commonly used circuit module, will lead to a global power reduction. Following these two design philosophies, a low power speed adder has been developed based on a new cell. This cell is a combination of an XOR gate and transmission gate. It offers both low power and high speed performance. The proposed cell has been compared with two other basic common cells. An extensive analysis of three types of adders, namely carry lookahead, carry select and carry skip has proved the superiority of the proposed cell.

The general objective of the work is to investigate the power, delay and power-delay product of low voltage full adder cells in different CMOS logic styles for the predominating tree structured arithmetic circuits. In DSP and ASIC rely on the efficient implementation of arithmetic circuits to execute algorithms such as convolution, correlation and digital filtering. As the complexity of arithmetic circuits grows with increasing processor bus width, energy consumption is becoming more important now than ever due to the increase in the number and density of transistors on chip and the faster clock. Different CMOS logic styles have evolved for the development of cell libraries. They are likely to perpetuate the ability to further reduce the cost-per-function and improve the performance of integrated circuits.

III. FIR FILTER

Digital finite impulse response (FIR) filters are frequently used in digital signal processing by virtue of stability and easy implementation. Although programmable filters based on digital signal processing cores can take an advantage of flexibility, they are not suitable for recent consumer applications demanding high throughput and low-power consumption. The application specific digital filters are frequently adopted to meet the constraints of performance and power consumption in such a consumer applications. The adders and multipliers play an important role in FIR filter while considering the power. The FIR filter consists of ‘n’ number of adders and ‘n+1’ number of multipliers. However, these filters are suffering from a large number of additions and multiplications, leading to excessive area and power consumption even if implemented in full custom integrated circuits. Therefore, the problem of designing digital filters with small area and low-power consumption has received a great attention during the last decade.

The FIR filters show the general classification of figure. The signal x with its response b is analyzed by contort linear time invariant system output y. The sum of the current is a weighted sum of output, the current for a discrete-time FIR filter, and inputs are past values 0 the input. The operation is define the output sequence y[n] in terms of its input sequence x[n], by the following equation,

$$Y[n] = b0X[n] + b1X[n-1] + \ldots\ldots + bN\,X[n-N] \ldots\ldots. 3.1$$

Where bi is the filter coefficients y[n] is the output signal, x[n] is the input signal and N is the filter order and or tap weights.

3.1 DIRECT FORM-I

The FIR Direct form Transposed architecture is replacement direct form application for FIR filters. The essential distinction is in the locating of delay elements. In direct form the inputs are first delayed and then multiplied with the coefficients, whereas in transposed form the coefficients are delayed multiplied with input and then only they are delayed.

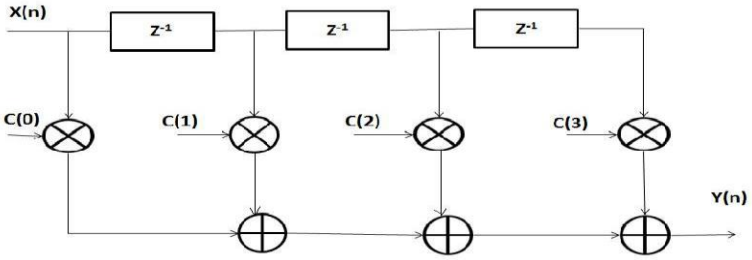

Figure 1: Direct Form-I FIR filter

3.2 DIRECT FORM-II

The alternate direct form II only needs *N* delay units, where *N* is the order of the filter – potentially half as much as direct form I. This structure is obtained by reversing the order of the numerator and denominator sections of Direct Form I, since they are in fact two linear systems, and the commutatively property applies. Then, one will notice that there are two columns of delays that tap off the center net, and these can be combined since they are redundant, yielding the implementation as shown below.

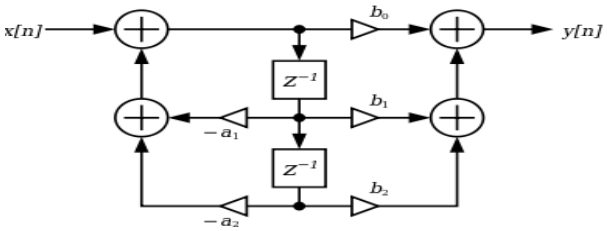

Figure 2: Direct Form-II FIR filter

3.3 TRANSPOSED FORM

The FIR Direct form Transposed architecture is replacement direct form application for FIR filters. The essential distinction is in the locating of delay elements. In direct form the inputs are first delayed and then multiplied with the coefficients, whereas in transposed form the coefficients are delayed multiplied with input and then only they are delayed.

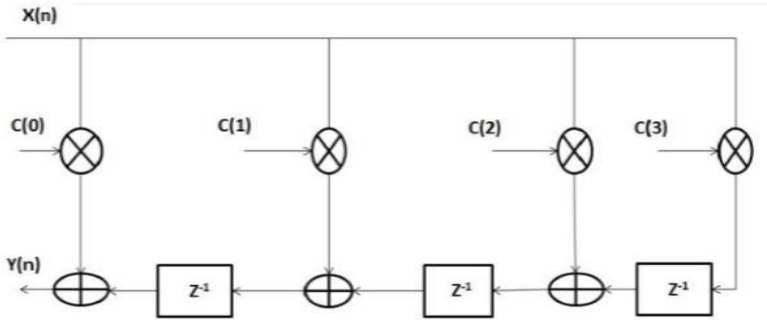

Figure 3: Transposed Form FIR filter

IV. SIMULATION AND RESULTS

4.1 SIMULATION RESULT:

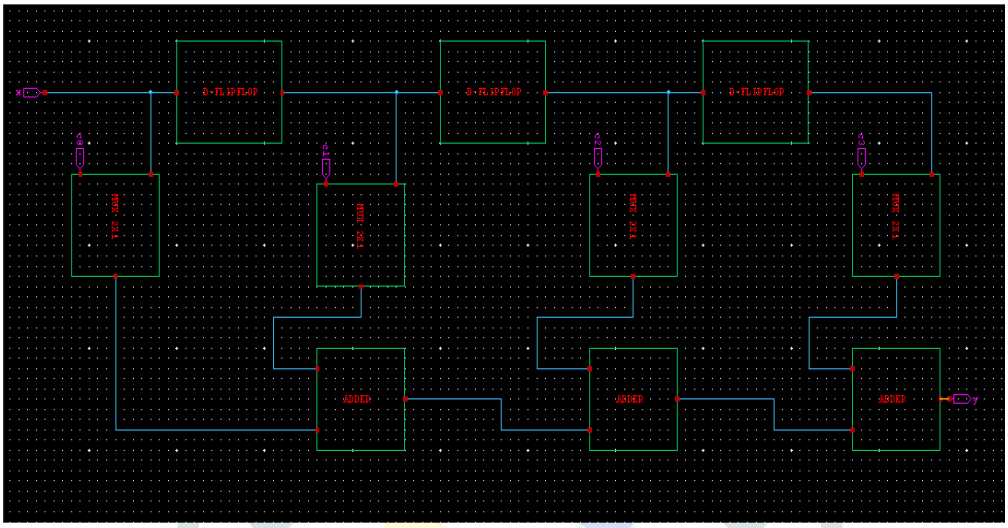

Figure 4 (a): FIR Filter by using Direct Form-1 schematic diagram

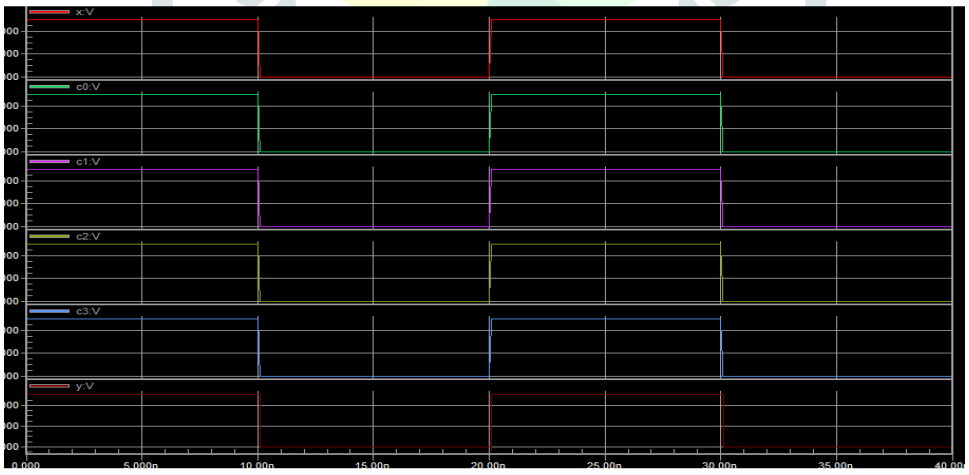

Figure 4 (b)**:** FIR Filter by using Direct Form-1 output waveform

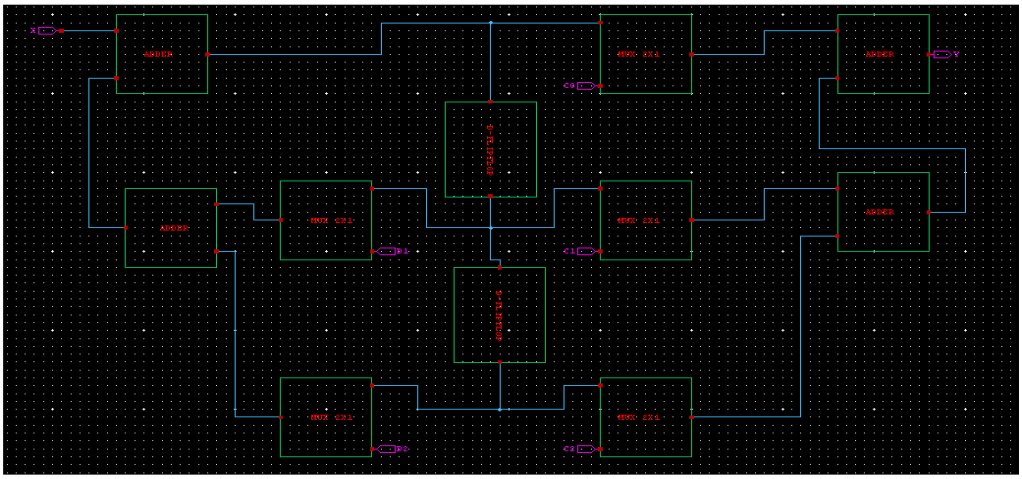

Figure 5 (a)**:** FIR Filter by using Direct Form-2 schematic diagram

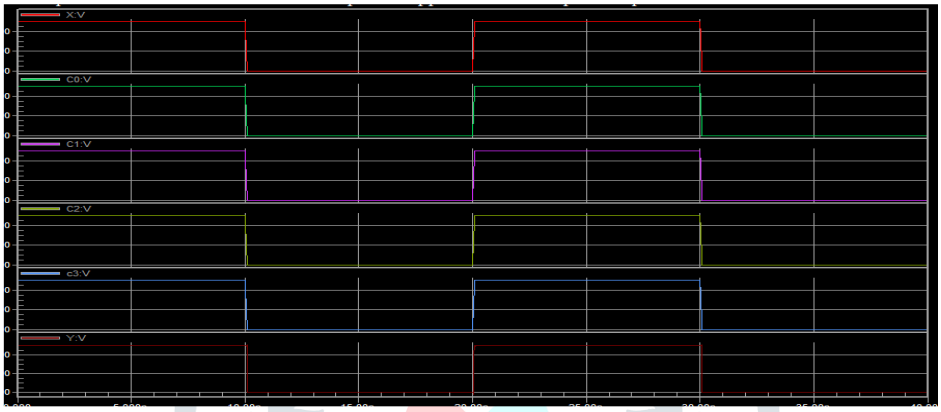

Figure 5 (b)**:** FIR Filter by using Direct Form-2 output waveform

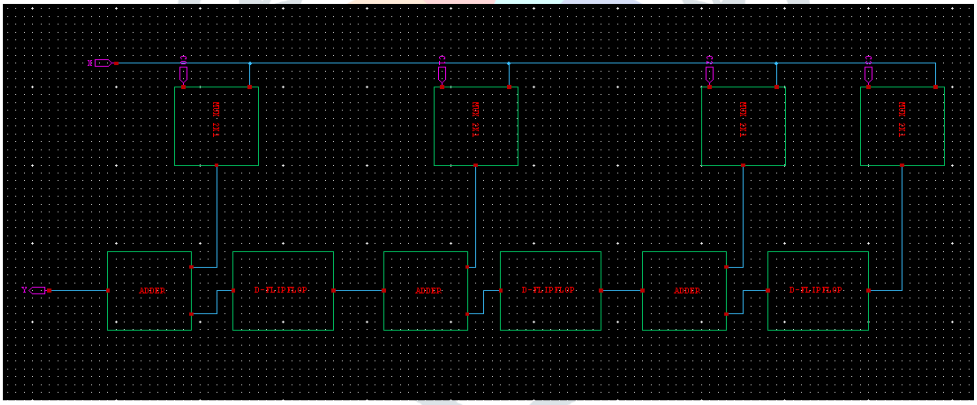

Figure 6 (a)**:** FIR Filter by using Transpose Form Schematic Diagram

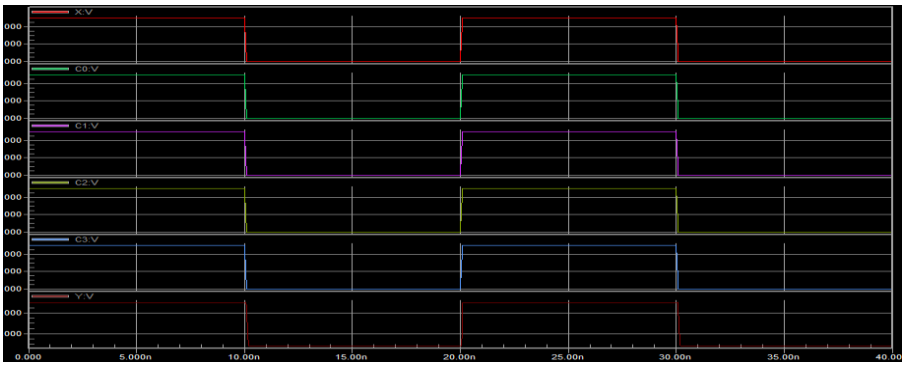

Figure 6 (b)**:** FIR Filter by using Transpose Form output waveform

4.2 COMPARISION RESULTS:

Table 4.1: Delay, power and Area Comparison

	Area	Power	Delay
Direct Form1	**102**	**0.128µW**	**5.38pS**
Direct Form II	**98**	**0.076µW**	**3.312pS**
Transpose Form	**102**	**0.195µW**	**4.212pS**

The filters are designed in linear phase. There are two types of techniques in linear phase they are non-folded filter is designed using normal D flip flop and then linear direct form folded is designed using normal D flip flop and it is compared. The figure and table shows this comparison. The folded filter with D flip flop using MUX is found to be really power efficient and have less transistor count than Non-folded filter with D flip flop using MUX. In the above comparison the filter using proposed Shannon full adder using multiplier is found to have 47% reduction. The Direct form FIR filter the best power reduction obtained is about 80% and for Transposed form filters it is about 83% and it is best result obtained. The comparisons of transistor counts the direct form FIR filter best reduction is about 42% and for the Transposed form filters it is about 30%.

V. CONCLUSIONS

The comparison between the Non-folded filters and folded filters with normal D flip flop are done. For the folded filters with CMOS adder multiplier, the reduction in count is about 42% in direct form where as in Transposed form reduction is 30%. The next comparison has been done between Non-folded filter and folded filter with D flip flop using MUX. In the case of folded filters with Shannon adder multiplier, the direct form has 47% and the Transposed form has 41% reduction in count. For future work the filters can be designed in both parallel loading and serial loading form with the low power multipliers and the delay elements and the results can be compared.

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