AN OPTIMAL DESIGN OF FULL SUBTRACTOR IN QCA NANOTECHNOLOGY

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Abstract - In upcoming years reaching of CMOS technology to the end of its way is expected due to high cost of lithography, Short channel Effect(SCE) , Physical Scalability and heating challenges. An alternative method to overcome the above mentioned challenges is Quantum dot Cellular Automata(QCA), which provides smaller area, high speed and low power consumption. Adders and Subtractors are important in all arithmetic and signal processing circuits. In this paper a full subtractor is proposed with reduced number of cells . The proposed subtractor is designed using two Exor gatse, two inverter gates and one OR and AND gate . The design is simultated and their functionalities are verified using coherence vector simulation in QCA designer 2.0.3.

Keywords* : *Inverter logics, majority gates, Quantom dot Cellular Automata, Subtractor.

I. INTRODUCTION

In the CMOS IC technology , the number of transistors in the integrated circuit (IC) has increased enormously in accordance with the Moore's Law. Due to reduction in the size of transistors , there is an increased number of transistors in ICs. As a result , it increases the power consumption , heat dissipation and also increases the area of the ICs.To overcome these drawbacks, many alternative methods are designed. Among which Quantum dot cellular Automata (QCA) is considered as the most promising technology that can replace CMOS technology. Quantum-dot Cellular Automata was first introduced by C.S.Lent et al. in 1993 and Experimentally verified in 1997.QCA is expected to provide high speed, very small area, high package density and very low energy dissipation.Transistors channel information through current or voltage,while QCA transfers informations through cell to cell or columbic interactions. Due to this QCA has very high switching or processing speed and low power or energy consumption.

This paper provides the implementation of reduced full subtractor circuit using the concepts of QCA. Subtractor is an important block in most of the arithmetic circuit and signal processing circuit.

II. QCA MATERIAL

A. QCA cells

A basic QCA cell consist of four quantum dots each at the four corners of square form .Electrons resides in each dot called as potential well. Each cell has two electrons which moves to the nearby dots through tunneling. Due to repulsive force electrons lies in the opposite corners. These configurations are designated as +1 (logic 1) and -1 (logic 0).

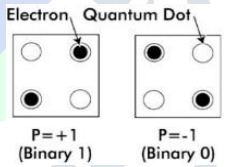


Fig.1 Basic QCA cell

B. QCA wire

Array of QCA cells forms an QCA wire in which the binary signals propagates from the input to output due to electrostatic interactions between cells .These wire has two QCA cell orientations, that is 90° QCA wire and 45° QCA wire . In 45° QCA wire the binary signals alternate between the 2 polarisations.

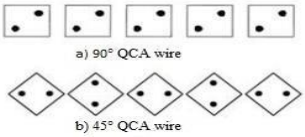


Fig. 2 QCA wire

C. QCA clocking

Any clocking system is required in QCA circuits to provide synchronization and to control the flow of information and mainly to provide the power required to run the circuit.The clock switching contain four phases Switch , Hold, Release and Relax. Proper placing of these zones is very critical to design high efficient circuit.

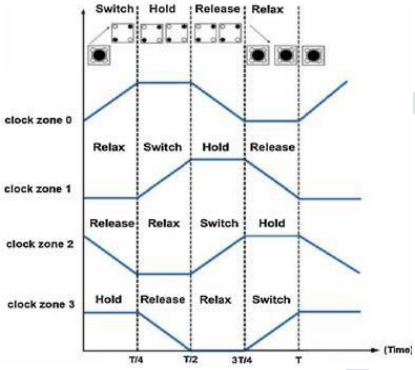


Fig. 3 QCA clock pulse

D. QCA Inverter

QCA inverter is a circuit that provides the reversed output value corresponds to the provided input value. Different types of inverter circuits have been designed in QCA .

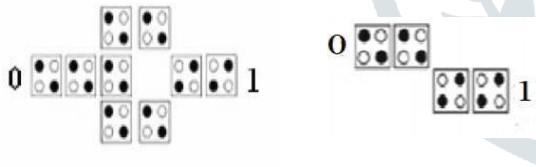


Fig.4 QCA inverters

E. QCA Majority gate

The QCA majority gate is a three input logic circuit .Let A,B and C be the inputs ,then the logic function of the majority gate is given as

M (A, B, C) = AB+BC+CA

Majority gate can be used used as OR gate and AND gate. By fixing one input as 0 it can perform AND operation and by fixing one input as 1 it can perform OR operation.

M (A, B, 0) = AB+A.0+B.0 = AB
M (A, B, 1) = AB+A.1+B.1 = A+B

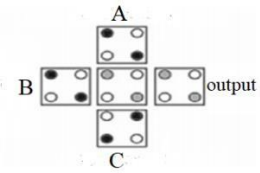


Fig.5 QCA Majority gate

F. QCA XOR gate

The XOR gate is one of the basic gates for the logic circuits. It is used in the design of full adder and full subtractor circuits. 3 input XOR gate is used in this paper for the implementation of full subtractor . The output of the 3-input XOR gate is given by the equation:

XOR(A, B,C) = A ⊕ B ⊕ C
A⊕ B⊕ C= A'B'C+ AB'C+ AB'C'+ABC

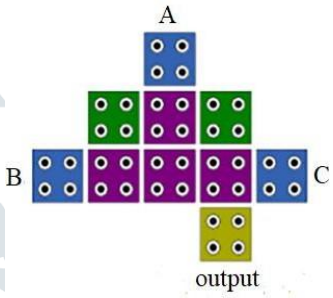


Fig.6 3-input XOR gate

III. FULL SUBTRACTOR

A Subtractor is one of the fundamental logic of arithmetic progressing unit. Subtractors are commonly designed using adders with exor gate. But these structures have high delay when compared with delicated subtractor structures. QCA has only few subtractor implementated designs . A full subtractor is a combinational circuit that performs subtraction of three inputs namely A,B,Bin and two outputs namely, Borrow and Difference.

The Boolean expressions for the Borrow and Difference is given by,

Borrow = A'B + A'Bin + BBin

Difference = A⊕B⊕Bin

In QCA, implementation of direct Boolean expressions requires large number of majority gates and QCA cells. So it is preffered to use the optimized Boolean expressions for the reduced cell logic .

So in this paper, the Boolean Expression for the Borrow function is modified as,

$$Borrow = A'(A \oplus B) + Bin(A \oplus B)'$$

This equation seems more complicated than the original equation but its implementation in QCA is simple and requires no cross wirings. This would reduce the size of the proposed Full subtractor structure.

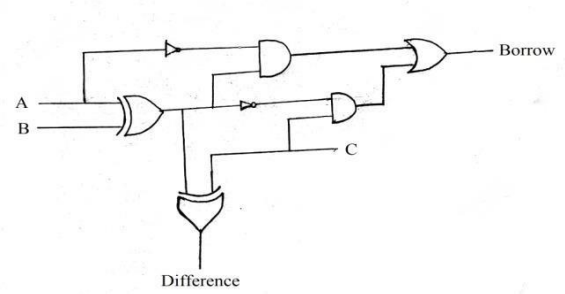


Fig. 7 Schematic of designed full Subtractor

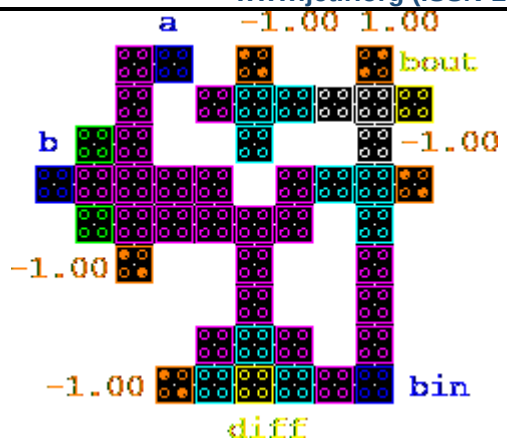
The Schematic diagram of the proposed subtractor is shown in fig. 7 . It consists of two exor gates , AND gates and inverters and one OR gate. Table I shows the simulation settings in QCADesigner tool which is used for implementation.

TABLE.I SIMULATION SETTINGS

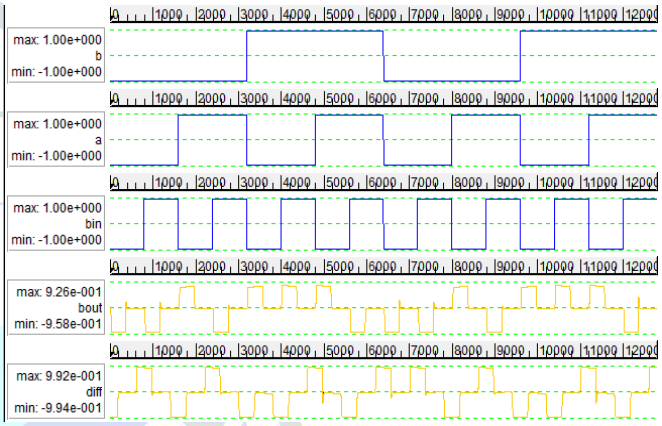
Parameter	Value
Cell dimension	18 nm x 18 nm
Dot diameter	5 nm
Radius of effect	80 nm
Relative permittivity	12.9
Clock High	9.8e-22
Clock Low	3.8e-23
Simulation engine	Coherence vector

IV. QCA IMPLEMENTATION

The QCA layout of the proposed full subtractor circuit is shown in the fig. 8(a) and its simulation results are shown in Fig.8(b). Table II shows the comparision of the results of the proposed subtractor with the other existing subtractor designs.



(a)



(b)

Fig.8. Proposed Subtractor. (a)QCA layout .(b)Simulation results.

TABLE II
COMPARISION OF RESULTS

Design	Cell Count	Area (μm^2)	Borrow delay	Difference delay
Existing Design[6]	63	20.4	3	3
Existing Design[5]	53	17.1	3	3
Existing Design[1]	84	27.2	3	4
Proposed Design	46	14.9	3	6

From Table II , we can understand that the prososed Subtractor has very less number of cells and area when compared with the already existing subtractor designs.

V.CONCLUSION

In this paper , a full subtractor with minimum number of cells has been designed and the area of the proposed design is 14.9 μm^2 , which is much less than the existing model. The performance of the proposed design has been demonstrated as per the truth table. A table has been included to illustrate the comparision between the proposed model and the existing models. This proposed model can be used to design more complex and high performance structure in future at nano scale levels.

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