Modified Dual Multilevel Inverter Topology for High Power and Medium Voltage Applications

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***Abstract*— This paper displays another three phase multilevel inverter arrangement suitable for open winding induction motor. Altered setup contains stranded three phase voltage source inverters are utilized along with one bi-directional switch in every phase. Because of this switch one extra voltage level presented in every phase.**

A modified dabble carrier sine PWM modulation scheme (MDCSM) is developed in such way to overcome the complexity of stranded space vector modulation technique. Hear Phase opposition modulation scheme used to reduce THD. Complete model of multilevel inverters created with basic MDCSM in MATLAB programming.

Keywords. Multilevel inverter; Dual inverter, modulation scheme, space vector modulation; PWM techniques; total harmonic distortion.

I. INTRODUCTION

From the past decades, multilevel inverters have attracted wide in both scientific community and on the industry, the reason is they have viable technogly to implement controlled rotational moment in high power applications [5]. Multilevel converters have a lot of advantages for medium to high voltage range of applications. This is used for variable speed motor and power system application. It's also including arras of power semiconductor switches capacitor voltages sources. The output of which generate voltage with stepped wave forms. The commutation of switches permits the additional of the capacitor voltages which reach high voltage at the output. While power semiconductor must with stand reduced voltages only. [5-1] Disadvantages of multilevel topologies include high number of semiconductor devices, complex control. As a result of the large number of control devices, large number of gate drives circuits. Several DC voltage sources required. [5-2]

They are different types of multilevel circuits involves. The first topology introduced was series hybrid design, this was followed by diode clamped multilevel inverter which utilized a bank of series capacitors and diodes, later invention is the flying capacitor design in which the capacitor were floating rather than series connected. [5] So the multilevel inverters are mainly classified as diode clamped, flying capacitor inverter and cascaded multilevel inverters. In which cascaded multilevel inverter control method is easy compare to other multilevel inverters, it does not require clamping diode & flying capacitor.

In this paper we are using a new topology of conventional VSI multilevel inverters for producing 5 level output voltage. This paper is organized as follows: The inverter configuration presented in section-II, The PWM modulation strategies in sec-III, Simulink results and conclusion in sec-IV and sec-V.

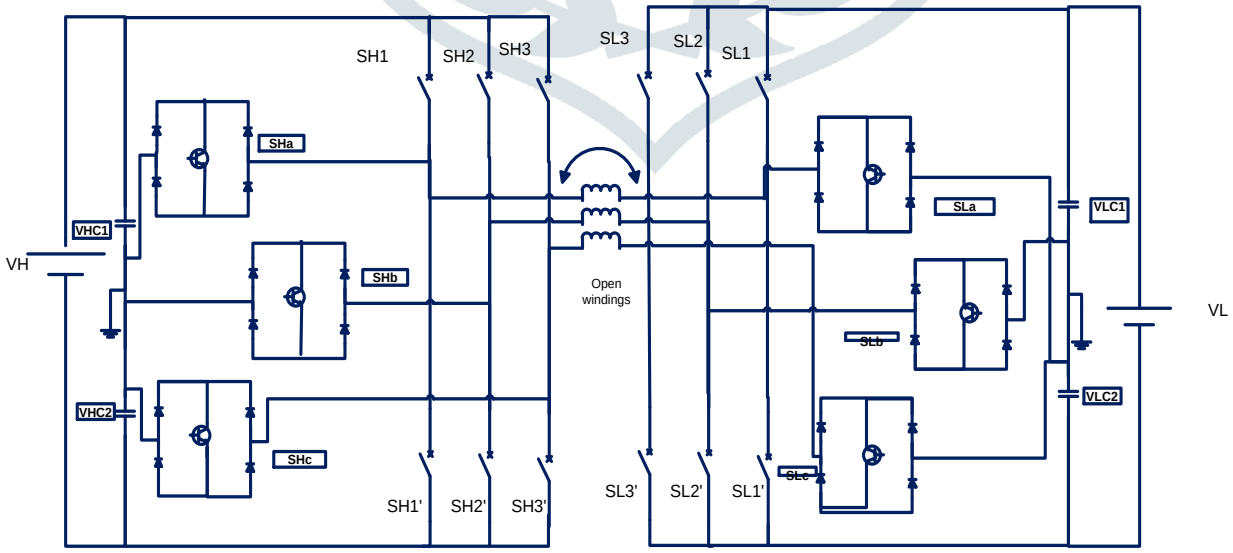

Fig.2.1 Dual inverter configuration for open windings

II. PROPOSED DUAL INVERTER WITH OPEN ENDED WINDINGS

Still standard two level voltage source inverter (VSI) are favored in more applications for simple usage, by appropriate courses of action they can perform has multilevel topologies with all advantages. In such case dual inverters are standers arrangement. This is designed by slight re-course of action of dc source in customary voltage source inverter[5]. These are associated at the two closures of open windings show in fig.2.1

This paper work concentrated on a novel design for dual three phase multilevel inverter suitable for open-winding loads, high power medium-voltage applications. Secluded structure involved routine three-phase voltage source inverter (VSI) alongside one extra bi-directional switch (MOSFET/IGBT) per phase and two capacitors with impartial association for three-phases, for presenting the extra voltage levels in each phase[5]. Proposed VSI is associated on every finishes of the open-windings gives multilevel output voltages 5-level in every leg of inverter.

The PWM modulation strategies:

In this paper added to an adjusted a solitary bearer five level regulation plan show in fig2.1. Where tweak reference sign is analyzed against triangular gives most extreme balance file and capacity to produce 5 level over every leg in three phase inverter, same system is connected to different legs of inverter by keeping legitimate phase shift of 120^{o} in reference signals. Another side also same technique but carrier signal is opposite to the previous ie (first inverter) one. In point of interest for phase A switch "SHa" and "SHb" must be adjusted all through the basic period, it swaps between {1 0} at exchanging period. [21] Switch SH1 must be tweaked a large portion of the key period, first half {1} and holds {0}, second half is material converse to switch SL1

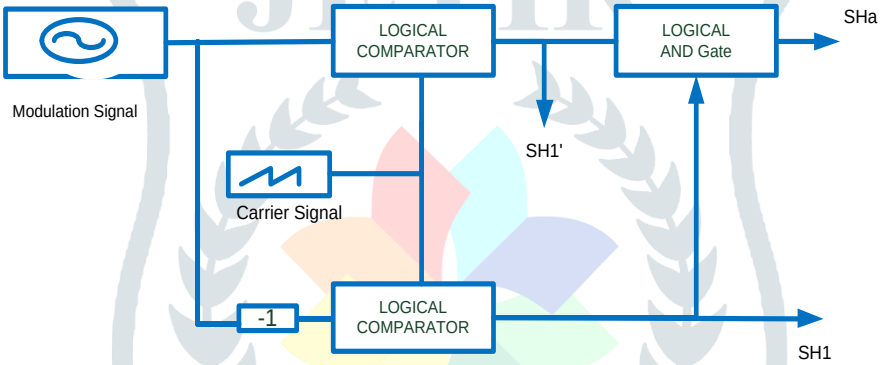

Fig.2.1 PWM Scheme

III. RESULTS

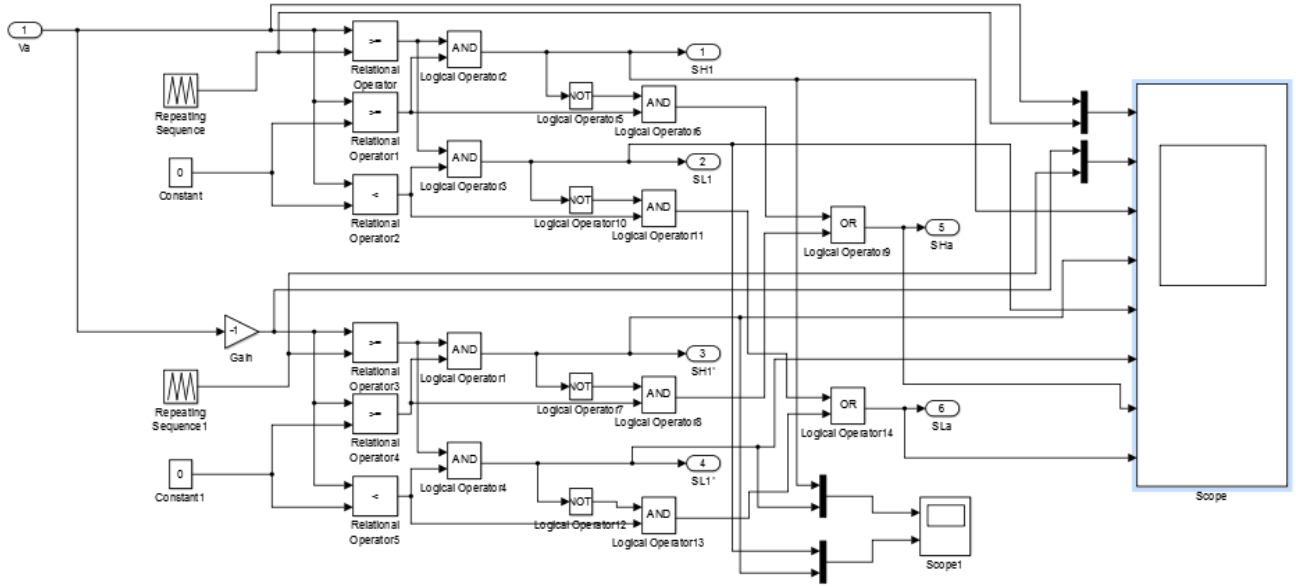

Fig.3.1 Simulation diagram for Modulation scheme

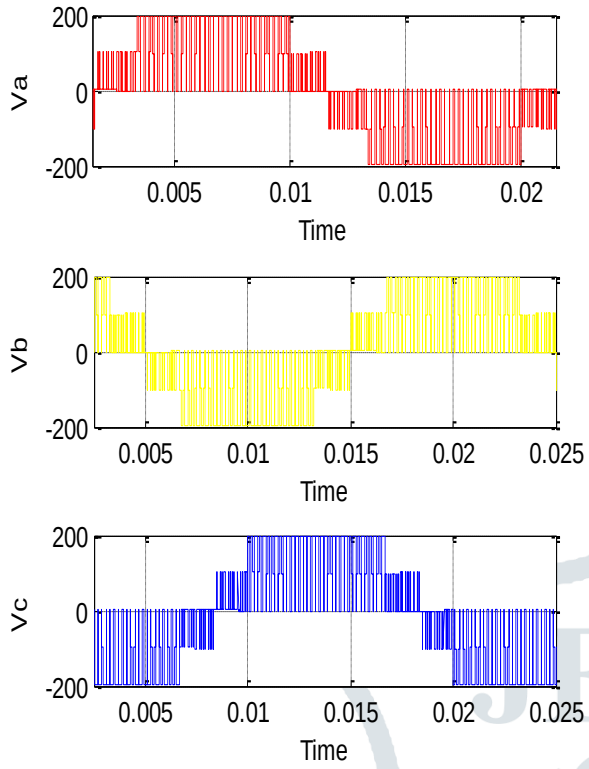

Fig 3.2 Five Level Line to Line Voltage

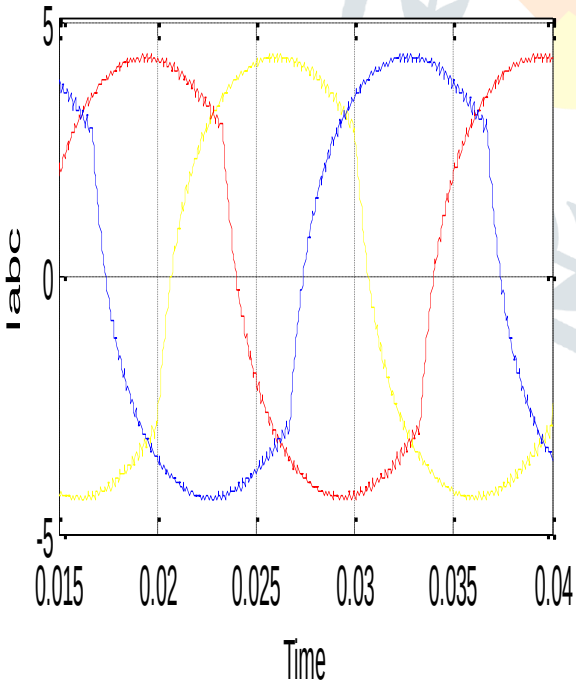

Fig 3.3 Line Currents

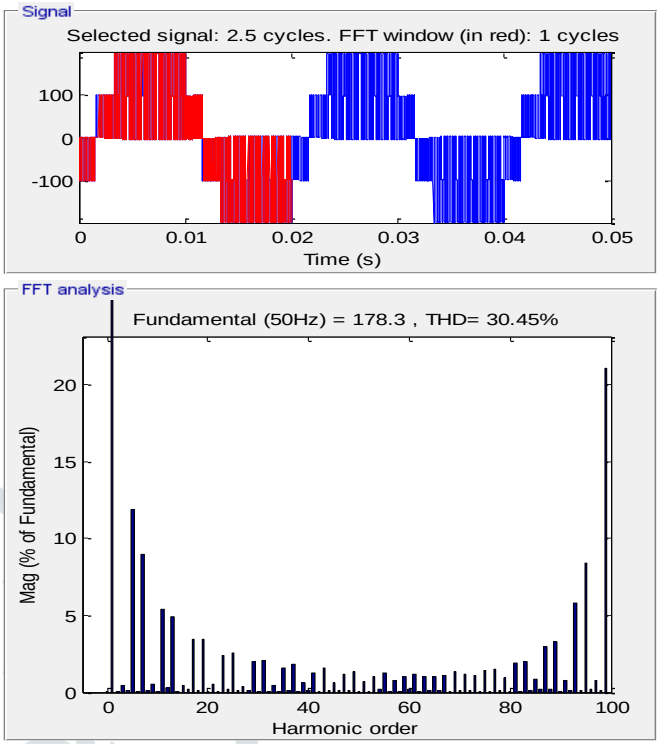

Fig 3.4 Voltage Signal THD

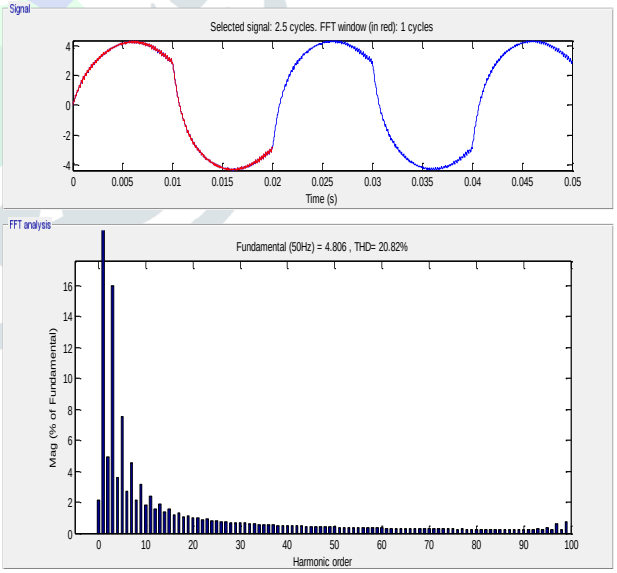

Fig 3.5 Current Signal THD

Table1. Parameters of dual inverter

Parameters of dual inverter	
DC Bus (V_H, V_L)	**200 Volts**
Load Resistances R	**8Ω**
Load inductance L	**10mH**
Fundamental Frequency F	**50Hz**
Switching Frequency F_S	**5KHz**
Capacitors	**2200μF**

In order to verify the results of the proposed dual inverter configuration along with modified single carrier five-level modulation algorithm. The system has to be designed in Mat lab package. Table 1 gives the detailed parameters taken for testing the dual inverter. The modulation index of inverter H and inverter L are fixed to 0.8 and overall modulation index of dual inverter is 0.8. Fig 3.2 denotes the line to line voltages of inverter H and L along with time average fundamental components.

Fig 3.3 denotes the line currents of dual inverter.
The total harmonic distortion is analyzed in FFT Window. Hear for voltage component THD are 30% and current component 20% as shoe in fig 3.4 and fig 3.5. These are low compare to conventional multilevel inverters.

IV. CONCLUSION

This paper displays another three phase multilevel inverter arrangement suitable for open winding induction motor. Some primary simulation results are provided in this paper which shows the suppression of lover order harmonics. Still investigation kept under developments to frame a proper multilevel PWM generation based on carrier based as well as Space vector modulation methods [5].

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