VLSI Design of Sign and Unsigned Irreversible and Reversible Baugh Wooley Multiplier

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ABSTRACT:- Reversible rationale is all that much sought after for the future figuring advancements as they are known not low power dissemination having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and picture preparing. Adders and multipliers are fundamental building blocks in many computational units. In this paper we have presented and implemented irreversible and reversible Baugh Wooley approach using standard irreversible and reversible logic gates/cells. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. It is proved that the proposed multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs and number of transistors required.

Keywords: - Irreversible Multiplier, Baugh Wooley Approach, Reversible Multiplier, Garbage Output, Quantum Cost

1. INTRODUCTION

Multipliers play a pivotal role in many high performance systems such as Microprocessor, FIR filters, Digital Processors, etc. In its early stage, multiplication algorithms were proposed by Burton and Noaks in the year 1968, by Hoffman in the year 1986 and by Guilt and De Mori in the year 1969 for positive numbers. In the year of 1973 and 1979, Baugh-Wooley and Hwang proposed multiplication algorithm for numbers in two's complement form. Multiplication is hardware intensive and the main criteria of interest are higher speed, lower cost and lower power [1]. With development in technology, several researchers have tried multipliers which provide design targets such as low power consumption, increased speed, and regularity of layout or combination of them in one multiplier. This helps making them suitable for achieving compact high speed and low power implementation. The performance of a system is generally controlled by the performance of the multiplier as the multiplier is usually the slowest element in the system. Furthermore, multiplier is normally the most area consuming element in the system [2].

In cutting edge VLSI framework power dissemination is high because of quick exchanging of inside signs. The multifaceted nature of VLSI circuits increments with every year because of pressing more rationale components into littler volumes. Consequently control dissemination has turned into the principle range of worry in VLSI plan. Reversible rationale has its rudiments from thermodynamics of data handling. As per this, customary irreversible circuits create heat because of the loss of data amid calculation. With a specific end goal to keep away from this data misfortune the ordinary circuits are displayed utilizing reversible rationale. Landauer demonstrated that the circuits outlined utilizing irreversible components scatter heat because of the loss of data bits [3]. It is demonstrated that the loss of one piece of data results in dispersal of KT*log2 joules of warmth vitality where K is the Boltzmann consistent and T is the temperature at which the operation is performed. Benett demonstrated that this warmth dissemination because of data misfortune can be stayed away from if the circuit is planned utilizing reversible rationale entryways [4]. An entryway is thought to be reversible if for every single info there is a novel yield task. Thus there is a coordinated mapping between the information and yield vectors. A reversible rationale entryway is a n –input, n-yield gadget showing that it has same number of inputs and yields. A circuit that is constructed from reversible entryways is known as reversible rationale circuit. In this paper, we plan 5×5 piece reversible multiplier that can perform multiplier operations at the same time. Every one of the modules is reenacted in modalism SE 6.5 and integrated utilizing Xilinx ISE 14.

Utilization of reversible rationale entryways to actualize such circuits can altogether diminish the force devoured. This paper covers different viewpoints about reversible registering and reversible rationale doors. We have attempted to plan a reversible execution of eight piece math and rationale unit, ideal regarding number of doors utilized and number of waste yields delivered [5, 6].

The configuration of two programmable reversible rationale entryway structures focused at ALU usage and their utilization in the acknowledgment of a proficient reversible ALU is illustrated. The ALU configuration is checked and its points of interest over the main existing ALU outline are quantitatively broke down [7].

Reversible rationale is all that much sought after for the future figuring advances as they are known not low power dissemination having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and Optical Computing. We have exhibited and executed reversible Wallace marked multiplier circuit in ASIC through changed Baugh-Wooley approach. Steady inputs, waste yields, equipment unpredictability, and number of transistors required are computed [8].

II. BAUGH WOOLEY MULTIPLIER

The Baugh-Wooley duplication is one of the effective techniques to handle the sign bots. This methodology has been created keeping in mind the end goal to plan normal multipliers, suited for 2's supplement numbers [2]. Let two n-bit numbers, multiplier (An) and multiplicand (B), to be duplicated. An and B can be spoke to as

$$M = -m_{n-1}2^{n-1} + \sum_{i=0}^{n-2} m_i 2^i \quad (1)$$

$$N = -n_{n-1}2^{n-1} + \sum_{i=0}^{n-2} n_i 2^i \quad (2)$$

Where $m_i's$ and $n_i's$ are the bits in M and N, respectively, m_{n-1} and n_{n-1} are the sign bits. The product $P = M \times N,$ is given by the equation:

$$P = M \times N = (-m_{n-1}2^{n-1} + \sum_{i=0}^{n-2} m_i 2^i) \times (-n_{n-1}2^{n-1} + \sum_{i=0}^{n-2} n_i 2^i) \quad (3)$$

The last item can be produced by subtracting the last two positive terms from the initial two terms [2]. Rather than doing subtraction operation, it is conceivable to acquire the 2's supplement of the last two terms and add all terms to get the last item. The last two terms are bits in which every that stretch out in double weight from position up to. Then again, the last item is 2n bits and reaches out in double weight from up to. At first cushion each of the last two terms in the item P mathematical statement with zeros to get a 2n-bit number to have the capacity to include it with alternate terms. At that point the cushioned terms stretch out in parallel weight from up to [3].

III. REVERSIBLE MULTIPLIER

A reversible rationale door is a n-information n-yield rationale gadget with balanced mapping. This decides the yields from the inputs furthermore the inputs can be particularly recuperated from the yields. A reversible circuit ought to be planned utilizing least number of reversible rationale doors. From the perspective of reversible circuit plan, there are numerous parameters for deciding the many-sided quality and execution of circuits. The quantity of Reversible entryways (N): The quantity of reversible doors utilized as a part of circuit. The quantity of steady inputs (CI) alludes to the quantity of inputs that are to be kept up consistent at either 0 or 1 keeping in mind the end goal to integrate the given coherent capacity. The quantity of trash yields alludes to the quantity of unused yields present in a reversible rationale circuit. One can't keep away from the trash yields as these are extremely crucial to accomplish A New Approach to the Design and Quantum cost (QC) alludes to the circuit's expense as far as the expense of a primitive entryway. It is figured knowing the quantity of primitive reversible rationale entryways (1*1 or 2*2) required to understand the circuit.
To figure result of two marked numbers we have utilized adjusted Baugh-Wooley approach [8]. Both legitimate and reversible multiplier outline is partitioned into two sections: fractional item era circuit and after that multi-operand expansion circuit.

Design of Logical Multiplier:-

In the first place to register fractional item, we utilized 17 and 8 NAND utilizing the method given in figure 6. After creating fractional items, next step is a multi-operand expansion. We ought to include the bits of every section given in figure 1. To include these bits, we require FA and HA. We need to include these bits in the way that our circuit will give the best results. Figure 6 demonstrates the method for including these bits in our proposed circuit. The Wallace methodology has been utilized to build a circuit with less postpones. To minimize delay in our proposed circuit, P9 is registered by transforming convey yield from prior FA (FA13). The subsequent circuit for multi-operand expansion needs one 1-NOT entryway, 4-HA and 16-FA.

Design of Reversible Multiplier:-

The operation of the 5x5 multiplier is depicted in figure 7. It consists of 25 partial product bits of the form $X_i Y_i$. The reversible 5x5 multiplier circuit has two parts. First, the partial products are generated in parallel using Toffoli gate.

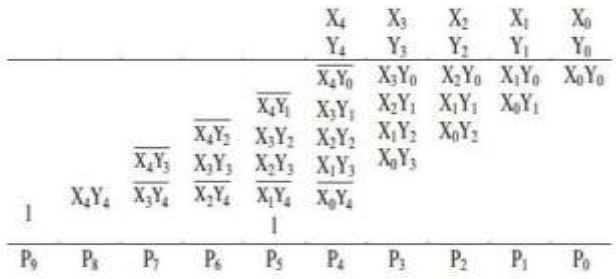

Figure 1: Baugh-Wooley 5 x 5 Signed Multiplier

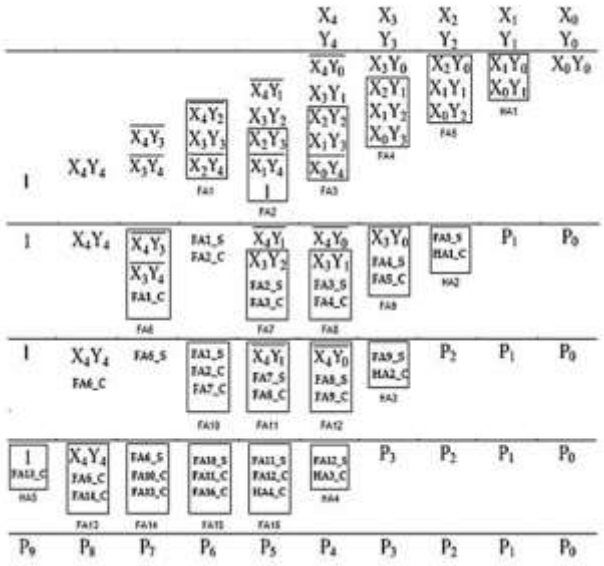

Figure 2: Multiplication by Wallace approach in the circuit

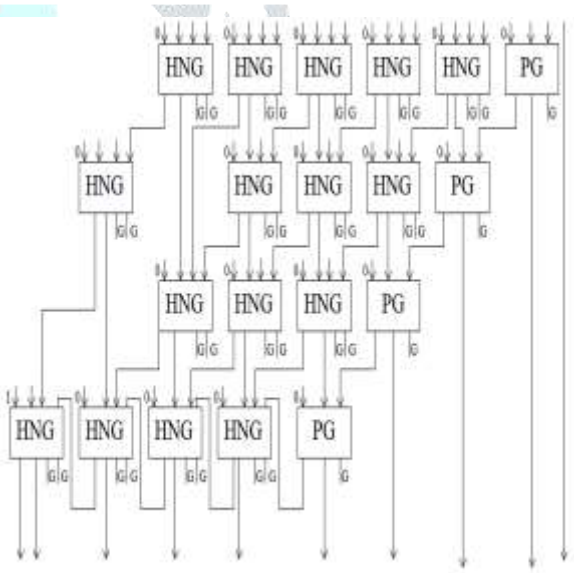

Figure 3: Multi-Operand Addition by Peres and Haghparast-Navi

We utilized 25 Toffoli entryways to make 17 ANDs and 8 NANDs as appeared in figure. The altered halfway the last low supplant by Peres entryway in light of the fact that Peres door has quantum expense of 4 as appeared if figure 3. Next step is a multi-operand expansion. In the wake of creating incomplete items, we ought to include the bits of every section given. To include these bits, we require FA and HA. We need to include these bits in the way that our circuit to give the best results.

IV. PROPOSED DESIGN

The proposed reversible multiplier design into two part i.e. partial product generation by Toffoli Gates and Peres gate

and multi-Operand Addition by Peres and Haghparast-Navi gates, Partial the last low replace by Peres gate because Peres gate has quantum cost of 4 as shown if figure 4. Next step is a multi-operand addition. After generating partial products, we should add the bits of each column. To add these bits, we need FA replace by HNG gate and HA replace by Peres gate. We have to add these bits in the way that our circuit to give the best results.

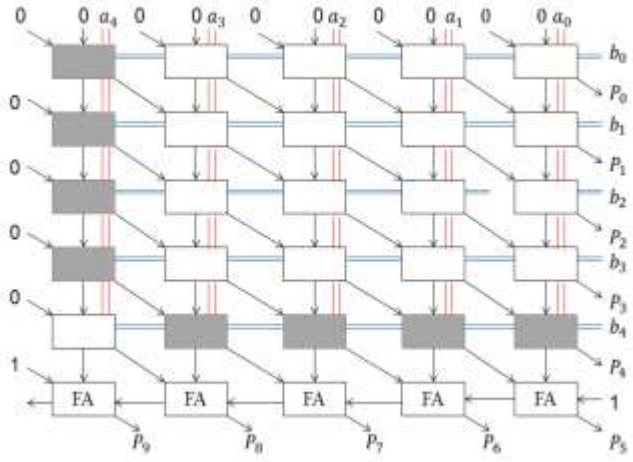

Figure 4: Proposed Design with white and gray cell

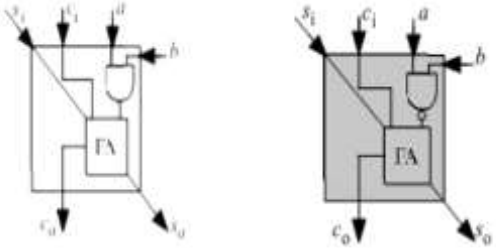

Figure 5: White and gray cell Structure

V. SIMULATION RESULT

The proposed irreversible and reversible multiplier circuit is more effective than the current configuration. The proposed irreversible and reversible multiplier circuit is separated two section i.e. fractional item and multi-operand expansion. The proposed halfway item is minimize 5 quantum cost in the configuration. Build the number piece of the reversible multiplier circuit so lessened the quantum cost.

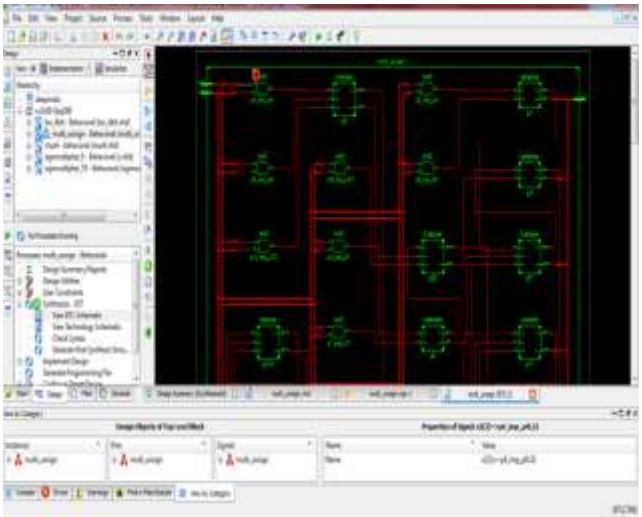

Figure 6: Register transfer level (RTL) using unsigned 8-bit multiplication

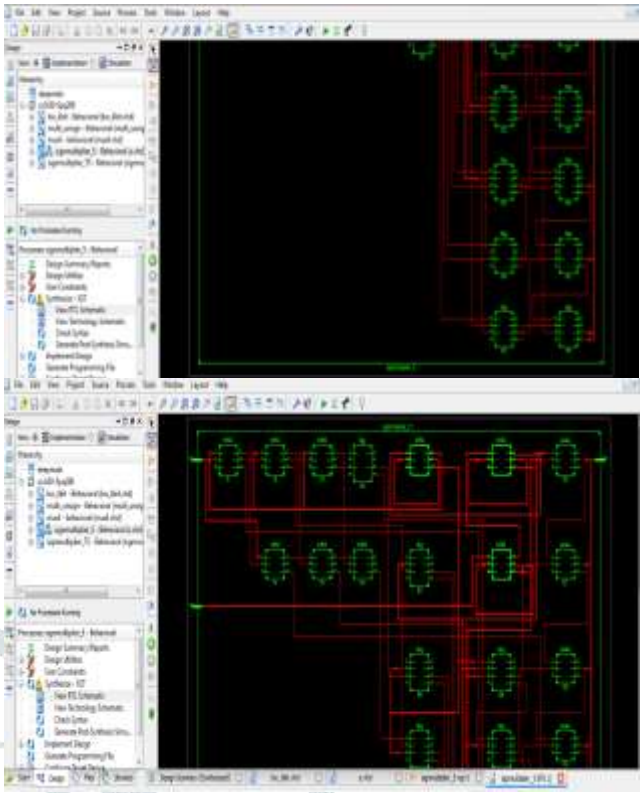

Figure 7: Register transfer level (RTL) using signed 8-bit multiplication

Table 1: Device utilization summary Spartan-3

Design	No of Slice	No of 4 input LUTs	MCPD
Previous Design	108	190	55.050
Modified Irreversible Multiplier	78	143	41.684

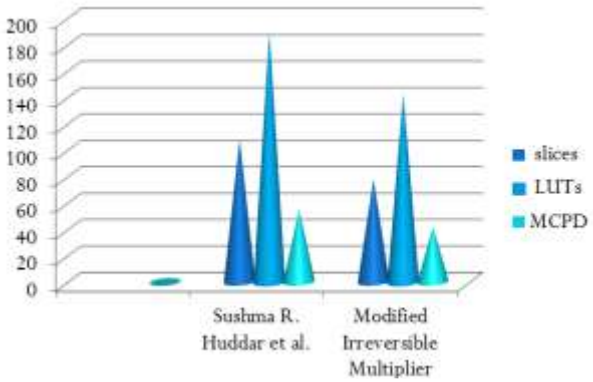

Figure 8: Bar graph of the Irreversible Multiplier

Table 2: Comparative results of reversible signed multiplier circuit

Method	No. of slice	No. of 4-i/p LUTs	No. of I/O switch	MCPD
Proposed	19	34	20	9.924
Previous Design	21	37	20	10.3235

VI. CONCLUSION

The 1-bit, 2-bit, 4-bit, 8-bit, 16-bit and 32bit reversible ALU is designed by integrating various sub modules that include DKG logic Gate. The performance evaluation of the various sub modules are carried out using Xilinx 14.1 ISE Simulator and it was found that the circuits designed using reversible logic showed a reduced delay and power. As a future work more arithmetic and logical function can be used.

Hence in future if reversible multiplier are used in VLSI design we can have low heat dissipation, low power and with comparatively less delay.

In future we can have some other combination of reversible logic gates that provides more arithmetic and logical operations and hence delay can be reduced to some more extent.

VII. REFERENCES

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