Design of Sense Amplifier using Flip-Flops for Memory Applications

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Abstract: **A novel high-speed and highly reliable sense amplifier- based flip-flop with transition completion detection (SAFF-TCD) is proposed for low supply voltage (*VDD*) operation. The SAFF-TCD adopts the internally generated detection signal to indicate the completion of sense-amplifier stage transition. The detection signal gates the pull-down path of the sense-amplifier stage and the slave latch, thus overcoming the operational yield degradation, current contention, and glitches of previous SAFFs.The operational yield, speed, hold time, energy consumption, and area of the proposed and previous FFs are quantitatively compared for a wide range of *VDD* with 22-nm Fin FET technology. It is shown that the minimum *VDD* of the SAFF-TCD is 573 mV lower than that of previous SAFFs, which means the SAFF-TCD can operate even when *VDD* is in the near threshold or sub threshold region. At 0.3–0.4 V, the SAFF-TCD operates twice as fast as the master–slave-based FF (MSFF) with a practical hold time.**

Index Terms **– Flip-flop (FF), low-voltage circuit design, sense amplifier (SA) etc.**

I. INTRODUCTION

Demand for an ultralow-power system on chip (SoC) continues to increase because of the growing interest in highly energy-constrained mobile SoC applications. In particular, for applications where performance is of secondary importance, one of the simplest and most efficient methods to improve energy consumption is to reduce the supply voltage (*VDD)* at the expense of speed loss. As part of this trend, digital circuit design techniques for sub threshold or near-threshold voltage operation have received increased attention [1]. The flip-flop (FF) is a key element as most modern microprocessors operate under the synchronous pipeline structure. In low *VDD* regions, to minimize speed degradation, it is preferable to use a fine-grained pipeline with fewer combinational logics between FFs [2]. This means that the relative portion of the power dissipation and clock cycle time of FFs is significant. Thus, the design of low-power FFs with small input (D) to output (Q) delay, *t*DQ, is essential. In addition, the effect of process variation on the driving strength of a transistor dramatically increases as *VDD* decreases, leading to a large variation in gate delay.

As a result, the setup time, *t*setup, in master–slave-based edge triggered FFs [3]–[6], which is determined by the worst case variation, is significantly increased [7]. In the pulse-triggered FFs proposed in [8]–[11], this problem is resolved. Input D of the pulse-triggered FFs starts to be sampled by the latch right after the clock rising edge, which results in nearzero or negative *t*setup. However, these FFs suffer from conflicting requirements for the width of the sampling window. A very small width cannot guarantee that the input data value properly propagates into the latch, whereas a large width increases the hold time, *t*hold. This so-called sizing problem becomes more severe as variation effects increase in low *VDD* regions, because the pulse width required to reliably propagate the input into the latch and *t*hold are determined by the respective worst variation corners. There are also approaches to achieve low *VDD* operation of FFs by utilizing 28-nm fully depleted silicon on insulator (FD-SOI) with back biasing [12], [13]. With the back biasing, circuit designers are allowed to control *Vth* dynamically, which enables to widen the operating voltage range. Especially in [13], it is demonstrated that nonvolatile FF based on magnetic tunnel junction can be operated with near-*Vth* FD-SOI circuits with the use of multiple *VDD* values. The sense-amplifier-based FF (SAFF) [14], which is composed of a differential SA stage followed by a slave element of NAND-based reset–set (RS) latch, is relatively unencumbered by the aforementioned large *t*setup and the sizing problem. For this reason, SAFF is regarded as an appropriate choice for low *VDD* applications. However, this conventional SAFF suffers from two major problems in low *VDD* environments. First, the NAND-based slave latch operates slowly, because the Q delay depends on the load on /Q and vice versa. Second, the SA stage may latch the wrong data because of the reduced voltage headroom and transistor mismatch. In this paper, a novel SAFF with transition completion detection (SAFF-TCD) is proposed in order to resolve these limitations at low *VDD*.

II. EXISTING METHOD

The proposed SAFF-TCD is designed to resolve the problems of previous SAFFs at low VDD by adopting the transition complete detection signal, TC. Fig 3.1 shows the structure of the SAFF-TC.

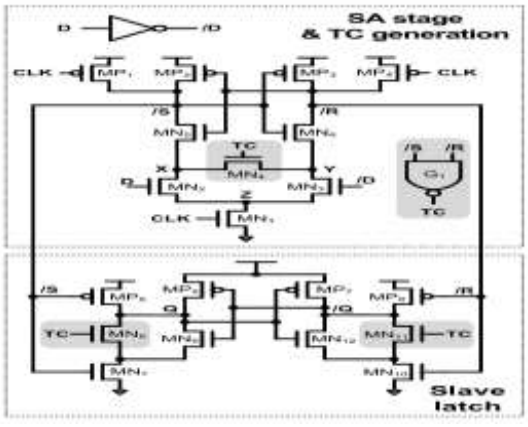


Fig.1. Structure of SAFF-TCD

A. SAFF-TCD

According to the SA stage operation, both /R and /S are precharged to high when CLK is low, which means that TC stays low before the rising edge of CLK. When CLK becomes high, the SA stage starts its transition, and if the transition finishes, one of /R or /S becomes low, which makes TC high. Because TC is connected to the gate of MN4, MN4 is turned OFF during the transition of the SA stage, and is only turned ON after the SA stage transition has finished.

Thus, SAFF-TCD is free from the degradation in speed and operational yield of the SA stage at low VDD caused by the always-turned-ON MN4 in previous SAFFs. This is confirmed by the operational waveforms of SAFF-TCD. Another noticeable feature of the proposed SAFF-TCD is that X and Y are not equalized during the precharge phase (CLK = 0). In the previous SAFFs, X and Y are equalized during CLK = 0 and the voltages of X and Y are same at the rising edge of CLK, which can alleviate the impact of the mismatch. However, in SAFF-TCD, X and Y can be different at the rising edge of CLK, and thus sensing stability can be degraded. Nevertheless, this negative effect of X= Y at the rising edge of CLK in SAFF-TCD is overcome by the positive effect gained by turning OFF MN4 during CLK is high.

This is because the proper voltage difference, which can be obtained between X and Y (according to D and /D) "during" the amplification phase with turn-OFF MN4, is much more important than X = Y "at" the beginning of amplification phase with turn-ON MN4. In addition to MN4 gating, the TC signal is applied to the gate nodes for NMOSs forming the pull-down paths of Q and /Q in the slave latch. The structure of the slave latch in SAFF-TCD is similar to the slave latch in Strollo's SAFF, but not exactly the same. The number of NMOS stacks in the slave latch is three, which is smaller than Strollo's SAFF whose slave latch has four-stacked NMOS path. With this structure, the problems caused by the slave latches in previous SAFFs, First, unlike the conventional SAFF, Q (/Q) can be discharged independently of /Q (Q) with a three-stage gate delay: 1) /R (/S) is discharged; 2) TC is charged up by G1; and 3) Q (/Q) is discharged by the MN8–MN7 (MN11–MN10) path. Thus, even when the load on /Q (Q) is large, the slave latch can rapidly discharge Q (/Q).

Second, unlike Kim's SAFF, no glitches occur in the Q or /Q nodes at the rising edge of CLK. This is because the pull-down path of Q or /Q is not enabled until /S or /R is discharged, respectively. Third, unlike Strollo's SAFF, no contention current occurs when Q or /Q transits. This is also attributed to the nature of TC, which becomes high only after /R or /S falls. In the example of falling Q, when the pull-down path of Q is enabled by TC, /R is already discharged and /Q is charging up, which means that MP6 is being turned OFF. In this way, the current contention between the pull-down paths of Q or /Q and latching PMOS transistors is prevented. The sense-amplifier-based FF (SAFF), which is composed of a differential SA stage followed by a slave element of NAND-based reset–set (RS) latch, is relatively unencumbered by the aforementioned large tsetup and the sizing problem. In this paper, a novel SAFF with transition completion detection (SAFF-TCD) is proposed in order to resolve these limitations at low VDD.

B. DISADVANTAGES OF EXISTING METHOD

- SAFF is regarded as an appropriate choice for low VDD applications. However, this conventional SAFF suffers from two major problems in low VDD environments.
- First, the NAND-based slave latch operates slowly, because the Q delay depends on the load on /Q and vice versa. Second, the SA stage may latch the wrong data because of the reduced voltage headroom and transistor mismatch.

III. PROPOSED METHOD

A. PROPOSED FLASH ADC

Flip-flop is a 1 bit memory cell which can be used for storing the digital data. To increase the storage capacity in terms of number of bits, we have to use a group of flip-flop. Such a group of flip-flop is known as a Register. The n-bit register will consist of n number of flip-flop and it is capable of storing an n-bit word. Here we designing parallel in parallel out registers using the proposed flip flop for high speed operations. By using the sense amplifier structure we are implementing a register. Sense amplifier circuits accept small input signals and amplify them to generate rail-to-rail swings.

As we will see, sense amplifier circuits are used extensively in memory cores and in low swing bus drivers to amplify small voltage swings present in heavily loaded wires. There are many techniques to construct these amplifiers, with the use of feedback (e.g., cross-coupled inverters) being one common approach.

The outputs of front-end are fed into a NAND cross-coupled SR FF that holds the data and guarantees that the differential outputs switch only once per clock cycle. The differential inputs in this implementation don't have to have rail-to-rail swing and hence this register can be used as a receiver for a reduced swing differential bus.

B. PARALLEL INPUT PARALLEL OUTPUT SHIFT REGISTERS:

Parallel In Parallel Out (PIPO) shift registers are the type of storage devices in which both data loading as well as data retrieval processes occur in parallel mode. Figure below shows a PIPO register capable of storing n-bit input data word (Data in). Here each flip-flop stores an individual bit of the data in appearing as its input (FF_1 stores B_1 appearing at D_1; FF_2 stores B_2 appearing at D_2 … FF_n stores B_n appearing at D_n) at the instant of first clock pulse. Further, at the same instant, the bit stored in each individual flip-flop also appears at their respective output pins ($Q_1 = D_1$; $Q_2 = D_2$ … $Q_n = B_n$). This indicates that both data storage as well as data recovery occur at a single (and at the same) clock pulse in PIPO registers.

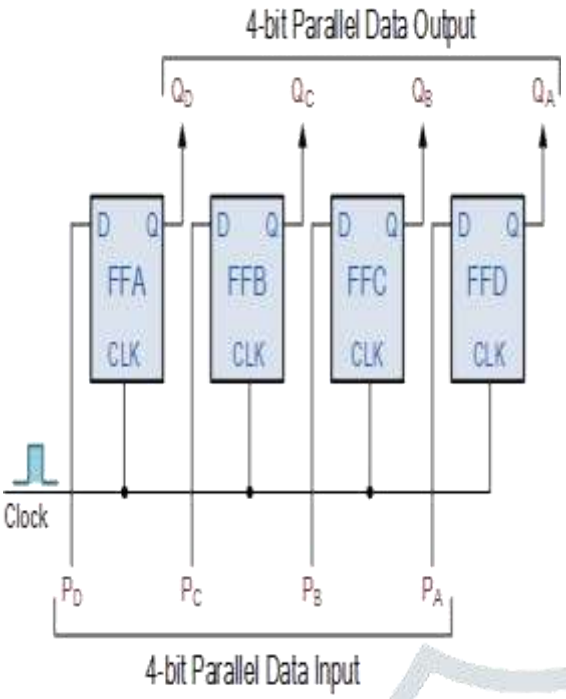
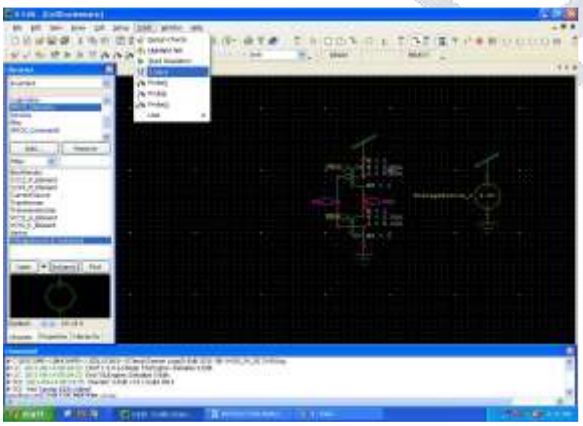


Fig.2: Block diagram of PIPO

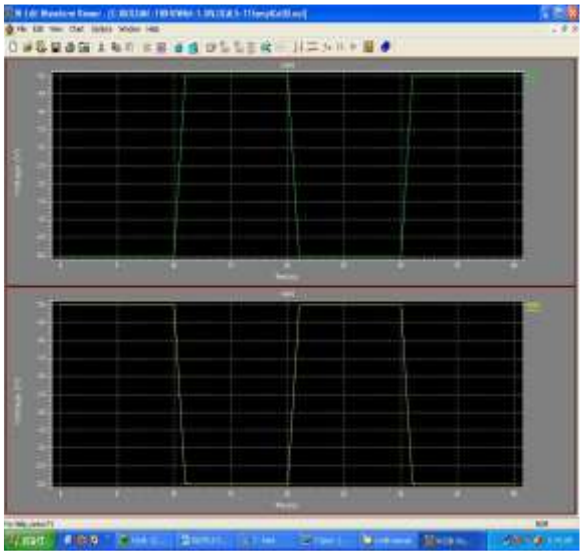
IV. SIMULATION RESULTS

A. Schematic design of Inverter

There are numerous stages or movements of a plan. A typical term you will hear when working with a Designer is "Schematic Design". This stage is early in the structure procedure. Schematic Design builds up the general degree, applied thoughts, the scale and relationship of the different program components. The essential target of schematic structure is to touch base at an unmistakably characterized practical idea dependent on the most encouraging design arrangements.



B. Output Waveform of Inverter



V. CONCLUSION

In the proposed paper, a low power high speed parallel in parallel out shift register is designed using sense amplifier based flip-flops. Replacement of conventional flip-flop with sense amplifier based flip-flop can save appreciable amount of power consumption hence now days it is preferred in low power ASIC design. The trading towards applications using sense amplifier based flip-flop from conventional flip-flop circuits in heavy pipelining, mobile devices or in low power ASIC circuits is immense achievement in field of VLSI designing. The proposed designs have been evaluated and analyzed using tanner EDA tool.

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