Performance Enhancement in Adiabatic Logics Using 16nm CMOS Technology

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Abstract: **To achieve higher performance of the CMOS device circuit along with high densities, there have been reductions in supply voltages, device dimensions and transistor threshold voltages over the years. But, these reductions have also resulted in higher leakage currents that can severely affect power consumption in a circuit. Here in this paper we propose an Adiabatic logic circuits with clock gating causes performance enhancement in terms of area, delay or power. Higher switching of clock causes high power consumptions, to reduce the area and power consumption we can have better logic circuits like Adiabatic logics where it results based on stored energy back to the supply. This proposed designs will be implemented in Tanner EDA and the simulated results will be compared with conventional designs.**

Index Terms – **CMOS Devices, NAND Gate and ECRL Logic, Tanner EDA etc…**

1. INTRODUCTION

To achieve higher performance of the CMOS device circuit along with high densities, there have been reductions in supply voltages, device dimensions and transistor threshold voltages over the years. But, these reductions have also resulted in higher leakage currents that can severely affect power consumption in a circuit. The power consumption of any CMOS VLSI circuit is composed of dynamic power and static power. The dynamic power dissipation is due to the switching activities of the circuit while the static power dissipation occurs due to the leakage components of the circuit during the standby mode. During submicron technology when the feature size was greater than 350nm, the leakage power dissipation was smaller than dynamic power by several orders of magnitude. With technology scaling there is a need of lowering of supply voltage and threshold voltage of VLSI circuits. However lowering of threshold voltage increases the static power dissipation. In ultra-deep submicron technology where the feature size is lesser than 100nm, static power dissipation has dominated the dynamic power. Thus there is need for reducing the static power dissipation in ultra- deep submicron technology. Domino Logic has proved to be a useful circuit in VLSI technology. Domino logic has various advantage like small area and high speed operation as compared to its static cmos counterparts. It uses the best property of static and dynamic logic without suffering from the load capacitance sensitivity as in pure dynamic logic. Domino logic is a clocked logic family which means that there is a clock in every logic gate. The continuous switching of clock in domino logic design leads to the higher power dissipation. Many techniques have been proposed to lower the power dissipation in domino logic module like scaling the supply voltage or using low-swing clock but a little focus has been given to clock gating technique. A clock gating technique has been used in which uses clock enabler circuit. Power dissipation has become a critical design metric for an increasingly large number of VLSI circuits. The exploding market of portable electronic appliances fuels the demand for complex integrated systems that can be powered by light weight batteries with pes" for minimizing power consumption in large-scale digital integrated circuits. The power consumed by a circuit is defined as p(t) = i(t) v(t), where i(t) is the instantaneous current provided by the power supply, and v(t) is the instantaneous supply voltage. Power minimization targets maximum instantaneous power or average power. The latter impacts battery lifetime and heat dissipation system cost, the former constrains power grid and power supply circuits design. We will focus on average power in the remainder of the paper, even if maximum power is also a serious concern. A more detailed analysis of the various contributions to overall power consumption in CMOS circuits (the dominant VLSI technology) is provided in the following section. It is important to stress from the outset that power minimization is never the only objective in real-life designs. Performance is always a critical metric that cannot be neglected. Unfortunately, in most cases, power can be reduced at the price of some performance degradation. For this reason, several metrics for joint power performance have been proposed in the past. In many designs, the power- delay product (i.e., energy) is an acceptable metric.

2. EXISTING METHOD

A domino logic module consist of a pull down network (PDN), dynamically connected, followed by a static inverter as shown in figure 1. The non-inverting output of domino is represented by signal *out* while domino node is represented by *X*. The PDN is built exactly as that in complementary CMOS. The domino module works in two phases – *precharge* and *evaluation*, where the signal *clock* controls the mode of operation as shown below: 000

$$clock = \begin{cases} 0, & \text{precharge phase} \\ 1, & \text{evaluation phase} \end{cases}$$

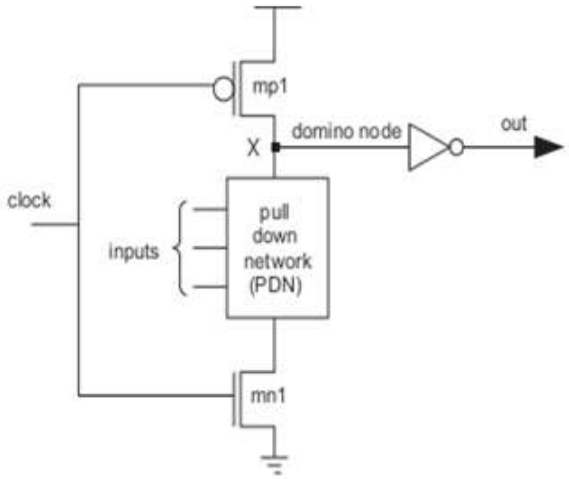

Fig 1: A Standard Domino Logic Module

The existing design uses clock gating in order the pass the clock only during the active state of the circuit. During standby mode, when the inputs of PDN are not changing, clock is not passed to the domino module and the output value of the circuit is hold till the next input transition. Figure 2 shows the proposed design of the domino CMOS logic. Here, a 2:1 multiplexer, mux, is used for clock gating and output hold. Signal clock and output are the inputs of mux while y is the output. The sleep is the control signal of mux. The output of mux i.e. signal y is as follows.

$$y = \begin{cases} clock, & \text{if } sleep = '0' \\ output, & \text{if } sleep = '1' \end{cases}$$

When the inputs of pull-down-network (PDN) are changing and circuit is in active mode, the signal sleep is '0' and y = clock. The clock signal passes to mp1 and mn1 transistors and operates the standard domino logic functionality. When the inputs are not changing, the signal sleep is '1' while y= out. This will hold the circuit state as explained below. Let out = 1 during standby mode. This means that domino node X = 0. Thus PDN is in conducting mode. Now, let sleep changes from '0' to '1'. Signal y will thus changes from clock to out i.e '1'. Thus mn1 is on while mp1 is off. Since PDN is already in conducting mode, the domino node becomes '0' while the value out = 1 is retained.

Figure 2 shows the domino logic with clock gating during standby mode and out = 1. Figure 3.3 shows the waveform of the proposed design for a 2-input NAND gate for A='1', B='1' and sleep signal changing from '0' to '1'. It can be seen that as the sleep signal becomes '1', out stops oscillating preventing the power dissipation. Let out is '0' during standby mode. This means X = 1. Thus PDN is not conducting. Let sleep changes from '0' to '1'. Now the values of y will also changes from clock to out i.e '0'. The value y = 0 puts mn1 to off state while mp1 is on. Thus X charges to VDD retaining the state of the circuit. In the existing design, neither the clock is present in the domino module during standby mode, nor does the output oscillate preventing the power dissipation in the Circuit.

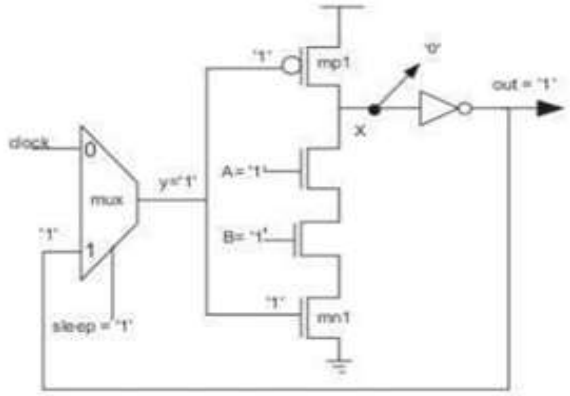

Fig.2: Design for a 2-input NAND gate during standby mode without='1'

3. PROPOSED METHOD

Low power circuits aim at providing best output and utilizing minimum possible power. Need for low power VLSI circuits is increasing day by day due to remarkable success and growth of the class of personal computing devices and wireless communications systems which demand high-speed computation and complex functionality with low power consumption. Large power dissipation requires larger heat sinks hence increased area and cost, and therefore highlight the need and importance of low power circuits. Adiabatic Logic is based on adiabatic switching principle. The term 'adiabatic' refers to a process in which there is no heat exchange with the environment. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.

A. ECRL Logic

ECRL consists of 2 cross coupled PMOS transistors in the pull up section whereas the pull down section is constructed with a tree of NMOS transistors. Its structure is similar to the cascade voltage switch logic with differential signaling. The logic function in the functional block can be realized with only NMOS transistors in pull down section.

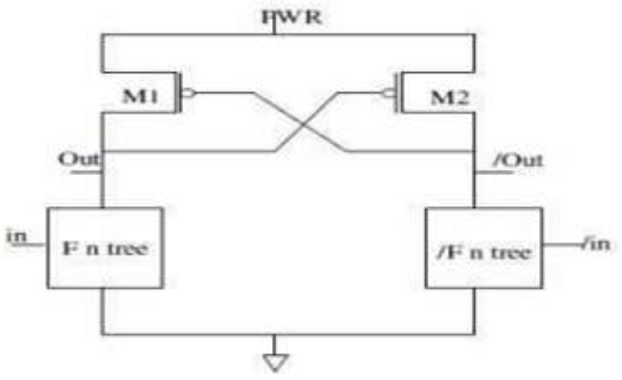

Fig 3: Basic structure of ECRL

ECRL performs precharge diode and dissipates less energy. In ECRL precharge and evaluation are perform simultaneously. VDD is used to recover and reuse the supply energy. The schematic diagram of NOT gate using ECRL is shown in figure 3. The transistors N1 and N2 implement the inverter logic whereas P1 and P2 allowthe output nodes to discharge the VDD. Assume A=1 and A bar =0, when the VDD power clock supply VCLK rises from 0 to VDD, voltage at OUT node remains at VSS i.e. low due to switching ON of the N1 transistor. The voltage at the OUT node capacitance follows the VCLK signal. When the power clock reaches VDD level, the outputs hold valid logic levels. These values are maintained during the hold phase. After the evaluation or hold phase, the VCLK falls down to a ground level, the OUT node capacitance discharges adiabatically into the power clock supply recovering the energy.

B. NAND Gate Using ECRL Logic

The schematic diagram of AND / NAND gate using ECRL is shown in below figure 4. AND / NAND gate multiplies A and B. It comprises of two outputs such that one output OUT gives the operation of AND gate and OUT bar gives the complimentary operation of AND gate i.e. NAND gate.

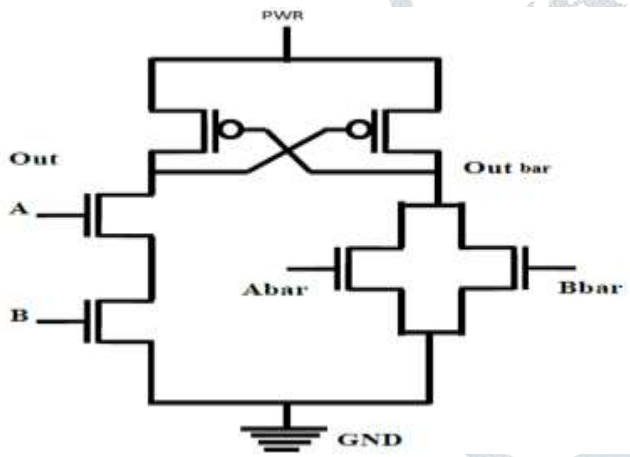

Fig 4: Schematic Diagram of NAND Gate Using ECRL

C. Full adder design using NAND gates

Full adder is a digital circuit used to calculate the sum of three binary bits which is the main difference between this and half adder. Full adders are complex and difficult to implement when compared to half adders. Two of the three bits are same as before which are A, the augend bit and B, the addend bit. The additional third bit is carry bit from the previous stage and is called Carry – in generally represented by CIN. It calculates the sum of three bits along with the carry. The output carry is called Carry – out and is represented by COUT.

NAND gate is one of the simplest and cheapest logic gates available. It is also called a universal gate because combinations of it can be used to accomplish functions of other basic gates. Create a Full-Adder circuit using only NAND gates as shown in figure 5. Based on this structure, we implement the design of NAND gate using full adder with adiabatic logics

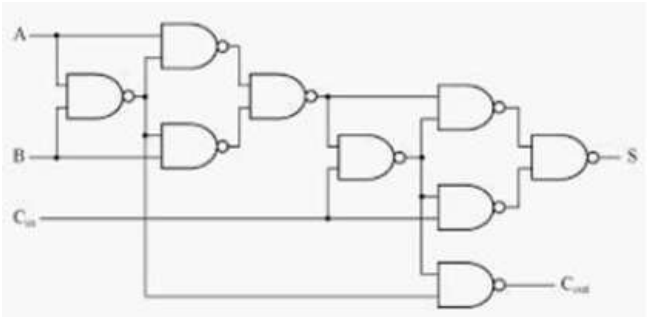

Fig 5: Full adder design using NAND gates

4. SIMULATION RESULTS

i. EXISTING METHOD

A. Full Adder

By using the tanner software, we get the results as shown in below. Figure 6 shows the Schematic circuit of existing full adder; Figure 7 shows the Output graph for existing full adder.

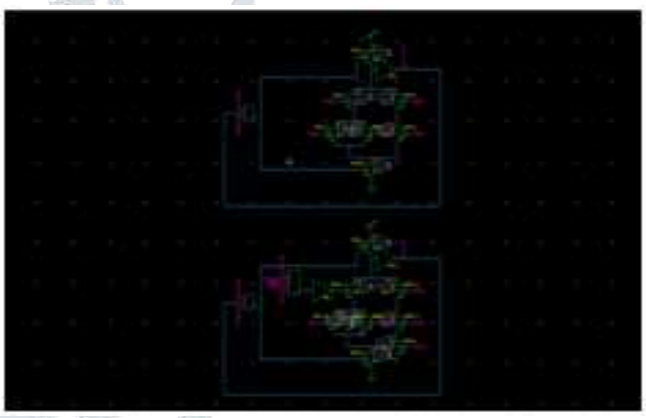

Fig.6 Schematic circuit of Existing Full adder

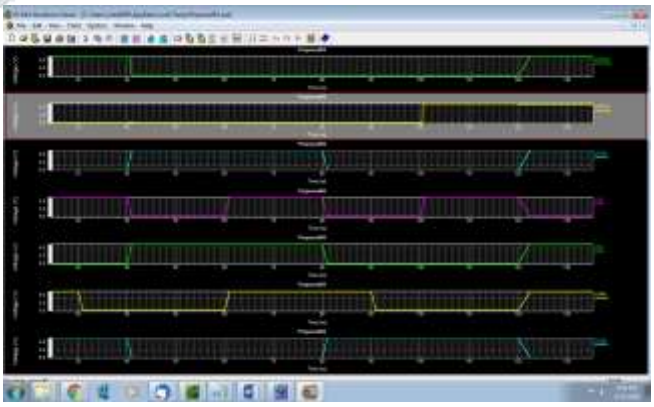

Fig.8.Output graph for Existing Full Adder

B. NAND Gate

By using the tanner software, we get the results as shown in below. Figure 9 shows the Output graph for existing NAND

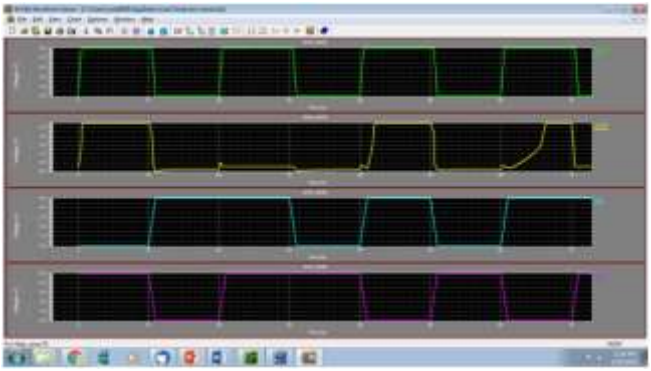

Fig 9.Output graph for Existing NAND

ii. PROPOSED METHOD

A. ECRL FULL ADDER

By using the tanner software, we get the results as shown in below. Figure 10 shows the Schematic circuit of ECRL full adder, Figure 11 shows the Output graph for ECRL full adder.

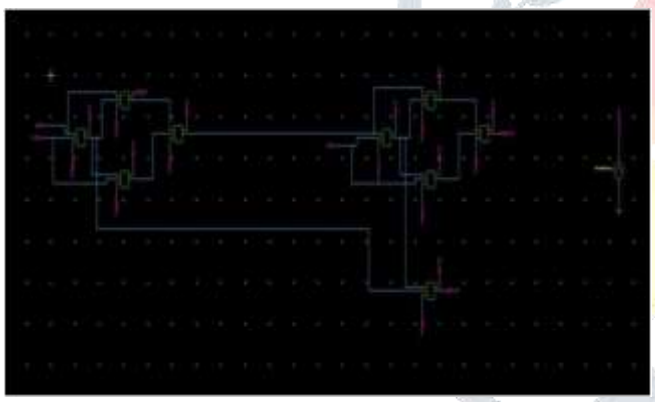

Fig 10.Schematic circuit of ECRL Full Adder

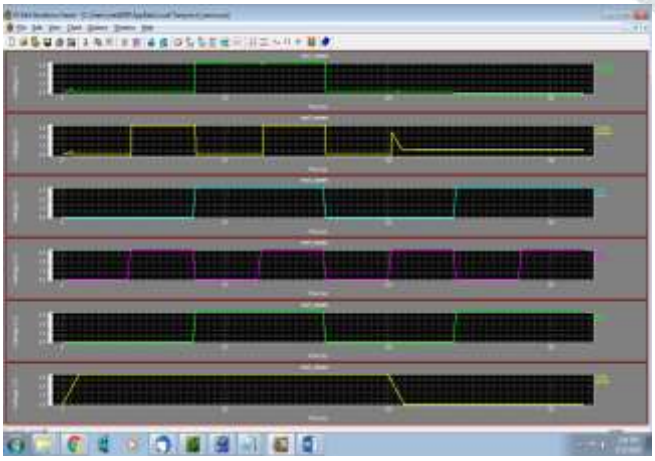

Fig 11.Output graph for ECRL Full Adder

B. ECRL NAND

By using the tanner software, we get the results as shown in below. Figure 12 shows the Output graph for ECRL NAND

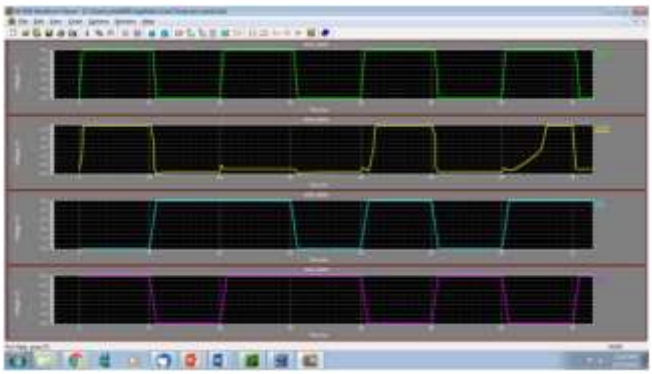

Fig12. Shows the Output graph for ECRL NAND

5. CONCLUSION

A clock gating scheme is applied to the standard domino logic which will bypass the clock during the standby mode of the circuit and will retain the circuit state. A 2:1 multiplexer using transmission gates is used for applying clock gating with output hold circuitry. There is an improvement in static power dissipation in the proposed logic with respect to standard domino logic. There is small increase delay in proposed logic with respect to domino logic. Thus proposed ECRL logic is a very low power design in ultra-deep submicron technology. This design dissipates less amount of power with some loss in performance. Low power devices has the feature of dissipating low power with increased delay. Thus this device is suitable for low power devices.

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