Design and Implementation of a Cascaded H-Bridge Multilevel DC-AC Inverter

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Abstract : In this paper, a multilevel DC-AC inverter is proposed. The proposed multilevel inverter generates seven levels, nine levels and eleven levels AC output voltage with the appropriate gate signals design. Here, the low pass filter is used to reduce the total harmonic distortion of the sinusoidal output voltage. The voltage stress and switching losses of power devices can be reduced in the proposed multi-level inverter. The various operating principles of the proposed multilevel inverter and the voltage balancing method of input capacitors are discussed.

IndexTerms: Multilevel, DC to AC inverter, Cascaded H- Bridge, Simulation, MPPT.

I. INTRODUCTION

A DC to DC converter takes the voltage from a DC source and converts the voltage of supply into another DC voltage level. They are used to increase or decrease the voltage level. This is commonly used in automobiles, portable chargers and portable DVD players. Some devices need a certain amount of voltage to run the device. Too much of power can destroy the device or less power may not be able to run the device. The converter takes the power from the battery and cuts down the voltage level, similarly a converter step-up the voltage level. For example, it might be necessary to step down the power of a large battery of 24V to 12V to run a radio.

A multilevel inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as an input. The term multilevel starts with the three-level inverter introduced in 1981. Multilevel inverters have an arrangement of power switching devices, capacitor, voltage sources. Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low Electro Magnetic Interference (EMI).Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM).The most attractive features of a multilevel inverter are, they can generate output voltages with lower dv/dt, draw input current with very low distortion, generate smaller common-mode (CM) voltage and they can operate with a lower switching frequency. Multilevel inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with limited maximum device rating.

As a result of high technology development, the demand and the quality of electric power is higher than before. Because of the advancement of semiconductor, the specification of power device and power conversion technique is promoted. One of the power converters which can transform DC to AC is called inverter. Inverter is the intermedium which transmit power to other electrical equipment such as uninterruptible power supply, servo motor, air-conditioning system, and smart grid compose of renewable energy shown in Fig. 1. To satisfy different demands and characteristic of loads, the output frequency and voltage have to change with different loads;

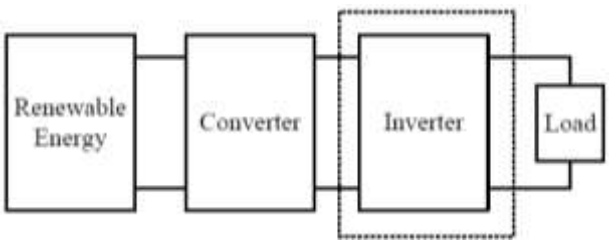


Fig 1. Block diagram of renewable system

In this paper, work has been carried out with the aim of reducing the number of power semiconductor devices and DC voltage sources, while achieving a higher number of levels at the same time. This paper is organized as follows: Section II describes

the related work carried in the past; Section III describes the proposed topology with its extension for a higher number of levels. To set the benchmark of the proposed topology for 7, 9 and 11 Level Section IV elaborates the various experimental results in MATLAB and Section V summarizes the paper.

II. RELATED WORK

In [1] this paper Maximum power point tracker algorithm based proportional-integrator controller (PI-MPPT) makes the solar cell worked at optimal condition by tracking the maximum power of solar cell using a PI controller. The result of the simulation shows that PI MPPT algorithm can control the solar cell to work at the optimal condition with boost converter circuit [2]. The result of the experiment shows that PI MPPT algorithm also can control the solar cell to work at the optimal condition with time sampling of PI MPPT 0.00005 seconds and a load of boost converter use four lamps.

In [2] this paper, a new hybrid model is proposed to control the DC/DC converter, this new controller is built on the fuzzy logic controller (FLC) and artificial neural network (ANN). The pathway taken to build the model is divided into three steps, the first step is to generate a data based on the FLC, the next step is to choose an ANN structure for modelling the FLC and the last step is the test and the validation of the obtained model. The phase of building an ANN is achieved by supervised learning based on back-propagation algorithm. This algorithm is used to train the ANN model by searching of the optimal weights and thresholds that has been a minimal root mean square error between the FLC output and the ANN model. The validation test was performed with various irradiation values between the both intelligent controllers and classical P&O algorithm simultaneously.

In [3] paper proposes the use of an OCC controller to perform the maximum power point tracking based on the constant voltage method to allow a safe battery charging. The proposed controller is compared with the traditional Perturb and Observe method in order to show the advantage of the PV panel constant voltage for the batteries charging without the voltage variations caused by the behaviour of Perturb and Observe method. In addition, the usage of OCC ensures fast response to transients, close to zero steady-state and excellent rejection to disturbances.

In paper [4] maximum power point (MPP) tracking technique for electromagnetic energy harvesters is presented. The concept is based on using a bidirectional AC/DC converter to simultaneously counteract the effect of the output inductance and match the output resistance of the harvester, in order to perform maximum power transfer. The modulating signal for the AC/DC converter is generated by sensing and processing the output current of the harvester without requiring a prior knowledge of the value of the output inductance and output resistance of the harvester. The MPP is located by observing the change of the form factor of the differentiated output current under a perturb-and-observe method. A 12W prototype MPP tracker has been built and evaluated. The experimental results are favourably compared with theoretical predictions.

III. PROPOSED SYSTEM

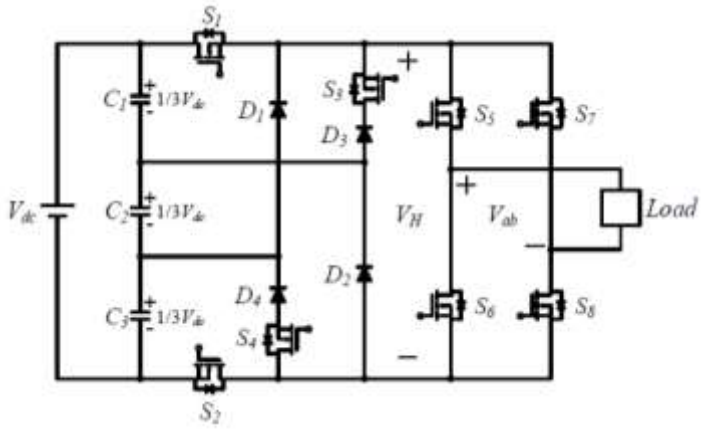


Fig. 2. Proposed topology of multilevel inverter

Fig.2 shows the proposed inverter topology used in all three levels, seven, nine and eleven level inverter. Capacitors C_1, C_2 and C_3 are connected in series and acts as a voltage divider at the input voltage side. Four MOSFET and four diodes are arranged along with four MOSFET switches which forms a cascaded H-bridge at the output terminal. This proposed multilevel inverter generates seven, nine and eleven levels AC output voltage along with appropriate gate signals.

A. Operating Principles

i. The required seven output voltage levels ($+1/3V_{dc}$, $+2/3V_{dc}$, $+V_{dc}$, 0, $-1/3V_{dc}$, $-2/3V_{dc}$, $-V_{dc}$) are generated and the modes of operation for the following are as shown.

Fig.3 shows the current paths for different level of voltages. Fig.3(a), 3(c), 3(e) shows current paths for ($+V_{dc}$, $+2/3V_{dc}$, $+1/3V_{dc}$,) respectively and Fig.3(b), 3(d), 3(f) shows current paths for ($-V_{dc}$, $-2/3V_{dc}$, $-1/3V_{dc}$,) respectively and Fig.3(g) shows that voltage applied to load terminals is zero.

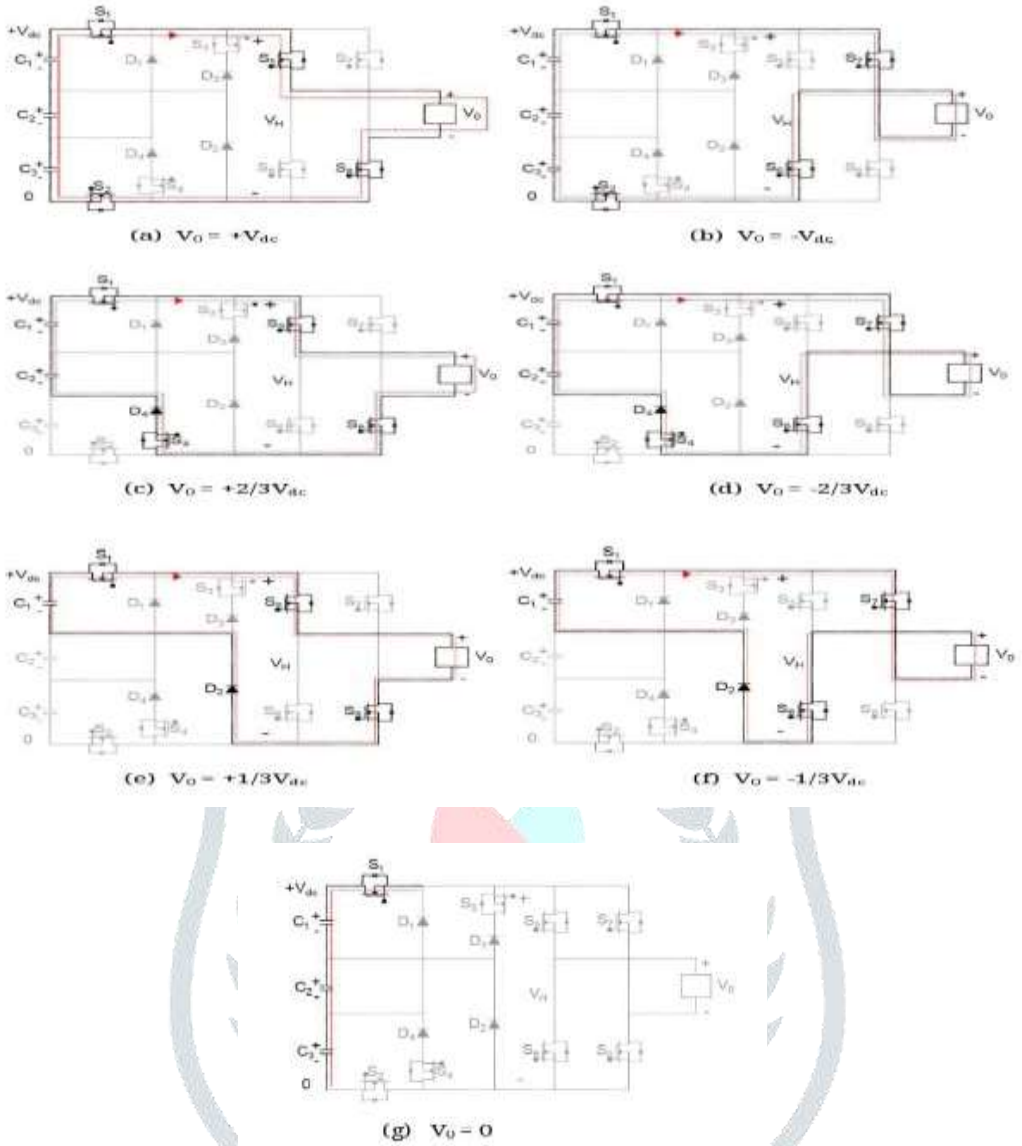


Fig.3 Switching combinations and current flowing path for different states of seven level output voltages

Table I lists the switching combinations at different output levels of Seven Level and the voltage at the capacitors are to be

$$C_1=C_2=C_3=V_{dc}/3 \qquad (1)$$

TABLE I

SWITCHING COMBINATIONS TO PRODUCE SEVEN LEVEL OUTPUT VOLTAGE WAVEFORM

S1	S2	S3	S4	S5	S6	S7	S8	OUT
1	1	0	0	1	0	0	1	Vdc
1	0	0	1	1	0	0	1	2Vdc/3
1	0	0	0	1	0	0	1	Vdc/3
1	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	0	-Vdc/3
1	0	0	1	0	1	1	0	-2Vdc/3
1	1	0	0	0	1	1	0	-Vdc

ii. The required nine output voltage levels ($+4V_{dc}$, $+3V_{dc}$, $+2V_{dc}$, $+V_{dc,}$ 0, $-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$) are generated and the modes of operation for the following are as shown in Fig.4.

Fig.4 shows the current paths for different level of voltages. Fig.4(a), 4(c), 4(e), 4(g) shows current paths for ($+4V_{dc}$, $+3V_{dc}$, $+2V_{dc}$, $+1V_{dc}$) respectively and Fig.4(b), 4(d), 4(f), 4(h) shows current paths for ($-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-1V_{dc}$) respectively and Fig.4(i) shows that voltage applied to load terminals is zero.

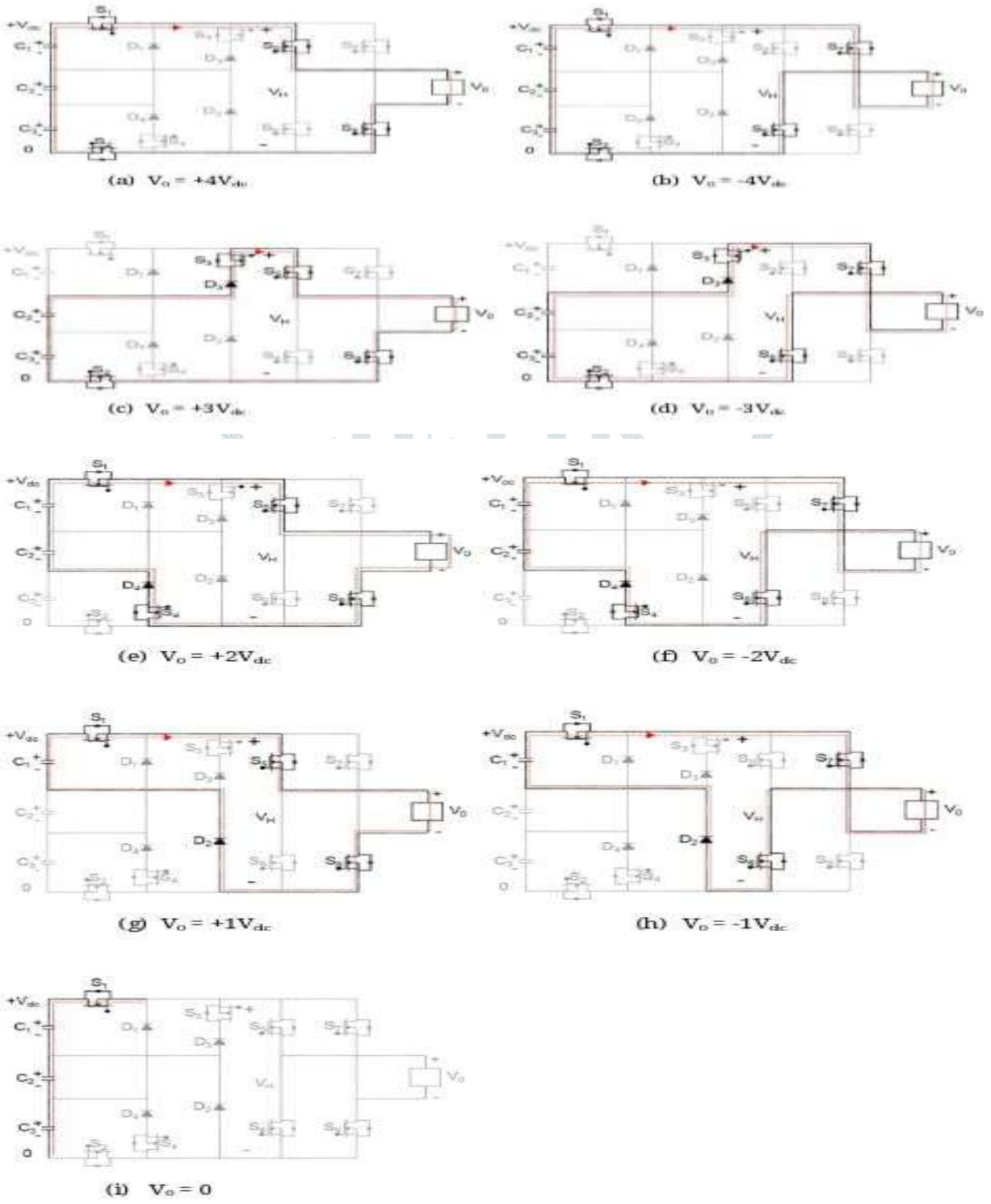


Fig.4 Switching combinations and current flowing path for different states of nine level output voltages

The proposed topologies with three DC voltage sources have been compared in terms of number of switches, number of gate driver circuit required, and the voltage losses. The table II lists the switching combinations at different output levels to generate nine level inverter and voltage at the capacitors are to be

$C_1=C_2=V_{dc}$ (2)

$C_3=2V_{dc}$ (3)

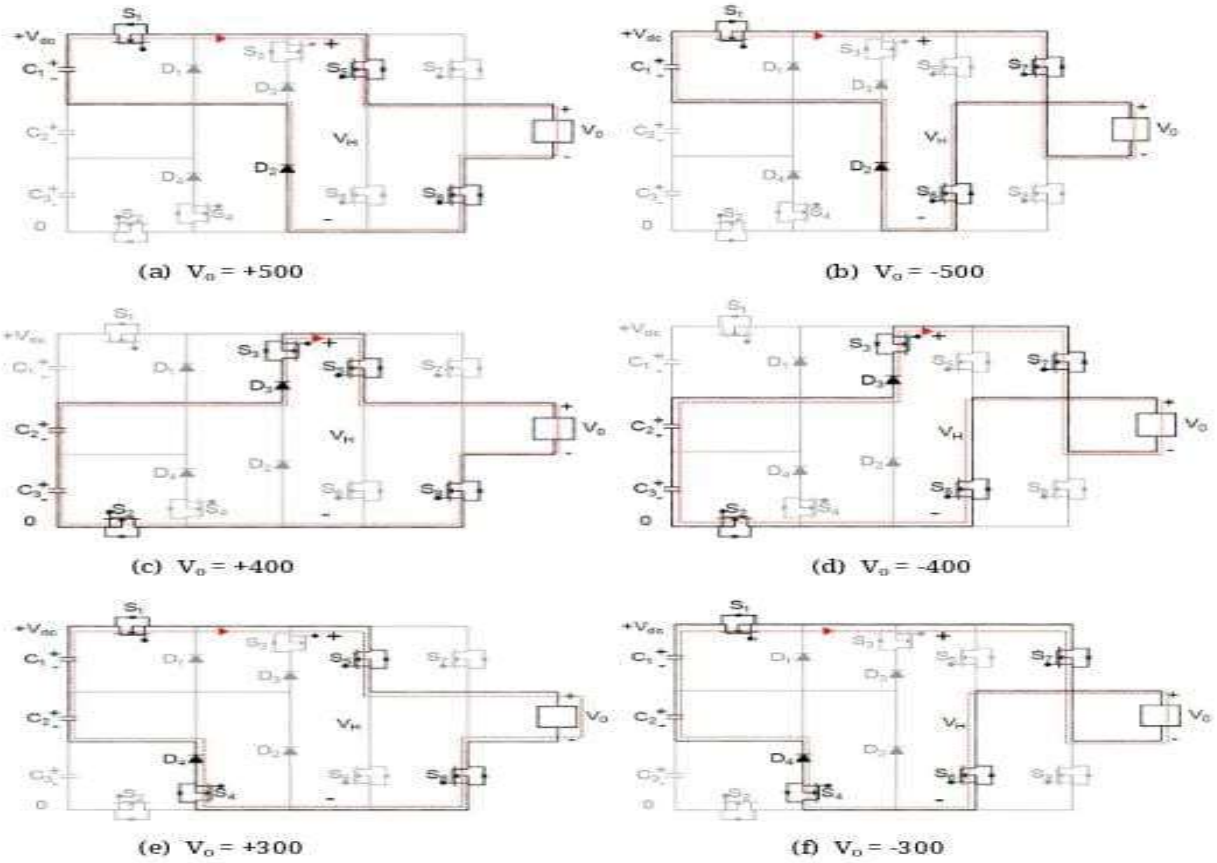
TABLE II

SWITCHING COMBINATIONS TO PRODUCE NINE LEVEL OUTPUT VOLTAGE WAVEFORM

S1	S2	S3	S4	S5	S6	S7	S8	OUT
1	1	0	0	1	0	0	1	4Vdc
0	1	1	0	1	0	0	1	3Vdc
1	0	0	1	1	0	0	1	2Vdc
1	0	0	0	1	0	0	1	Vdc
1	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	0	-Vdc
1	0	0	1	0	1	1	0	-2Vdc
0	1	1	0	0	1	1	0	-3Vdc
1	1	0	0	0	1	1	0	-4Vdc

iii. The required eleven output voltage levels considering V_{dc}=100V are (+500, +400, +300, +200, +100, 0, -500, -400, -300, -200, -100) are generated and the modes of operation for the following are as shown.

Fig.5 shows the current paths for different level of voltages. Fig.5(a), 5(c), 5(e), 5(g), 5(i) shows current paths for (+500, +400, +300, +200, +100) respectively and Fig.5(b), 5(d), 5(f), 5(h), 5(j) shows current paths for (-500, -400, -300, -200, -100) respectively and Fig.5(k) shows that voltage applied to load terminals is zero.



(a) V_o = +500 (b) V_o = -500

(c) V_o = +400 (d) V_o = -400

(e) V_o = +300 (f) V_o = -300

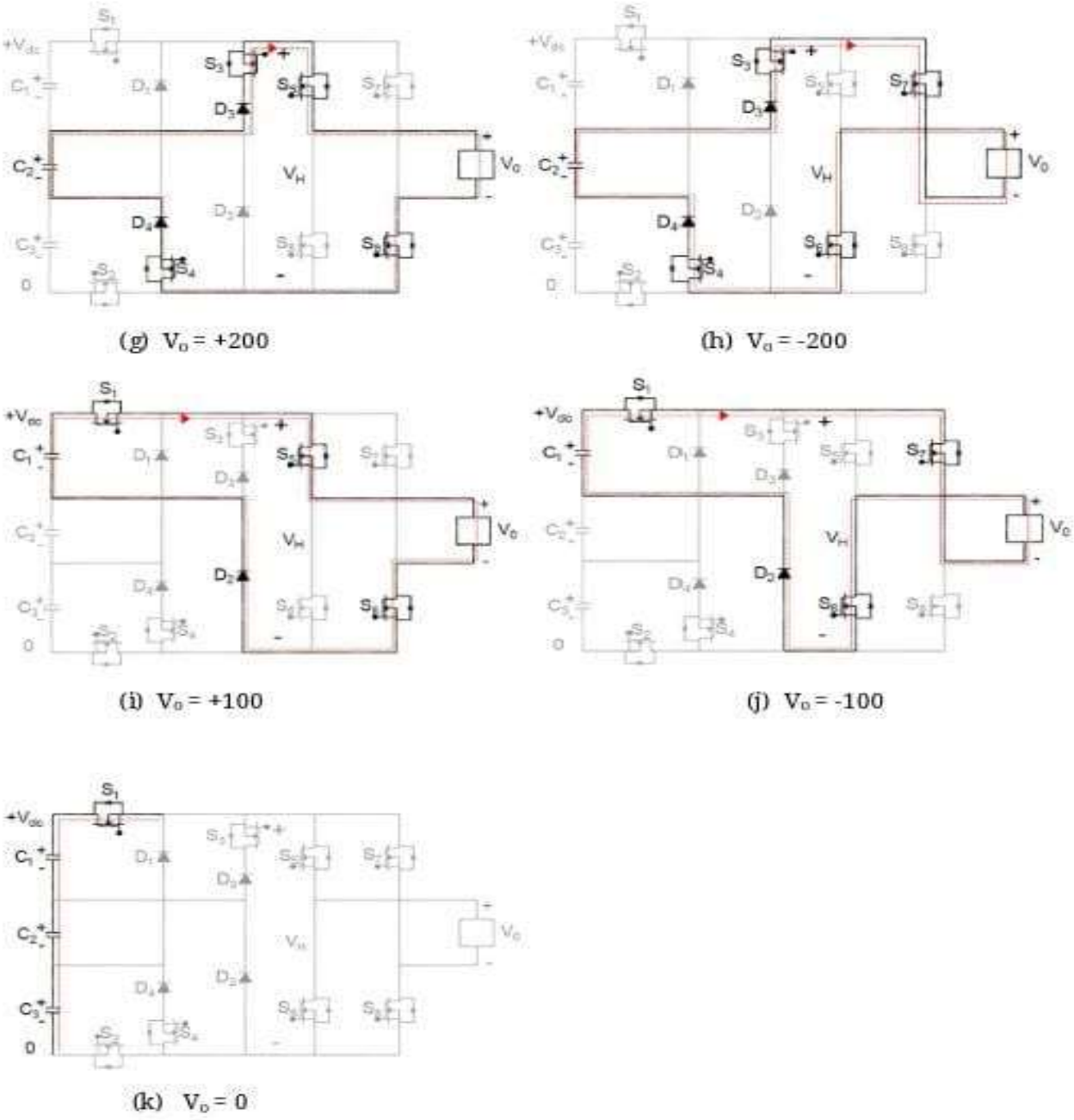


Fig.5 Switching combinations and current flowing path for different states of eleven level output voltages

Table III lists the various switching combinations at different output levels for eleven level

TABLE III

SWITCHING COMBINATIONS TO PRODUCE ELEVEN LEVEL OUTPUT VOLTAGE WAVEFORM

S1	S2	S3	S4	S5	S6	S7	S8	OUT
1	1	0	0	1	0	0	1	5Vdc
0	1	1	0	1	0	0	1	4Vdc
1	0	0	1	1	0	0	1	3Vdc
0	0	1	1	1	0	0	1	2Vdc
1	0	0	0	1	0	0	1	Vdc
1	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	0	-Vdc
0	0	1	1	0	1	1	0	-2Vdc
1	0	0	1	0	1	1	0	-3Vdc
0	1	1	0	0	1	1	0	-4Vdc
1	1	0	0	0	1	1	0	-5Vdc

IV. EXPERIMENTAL RESULTS

The proposed seven level, nine level, and eleven level H-bridge inverter simulation is simulated in MATLAB/SIMULINK platform as shown in Fig. 6. The model is same for all three levels i.e., seven, nine and eleven level, with variation in input voltages. Fig.7 shows the output voltage waveform of simulated seven level cascaded H-bridge inverter. Fig.8 shows the output voltage waveform of simulated nine level cascaded H-bridge inverter and Fig. 9 shows the output voltage waveform of simulated eleven level cascaded H-bridge inverter.

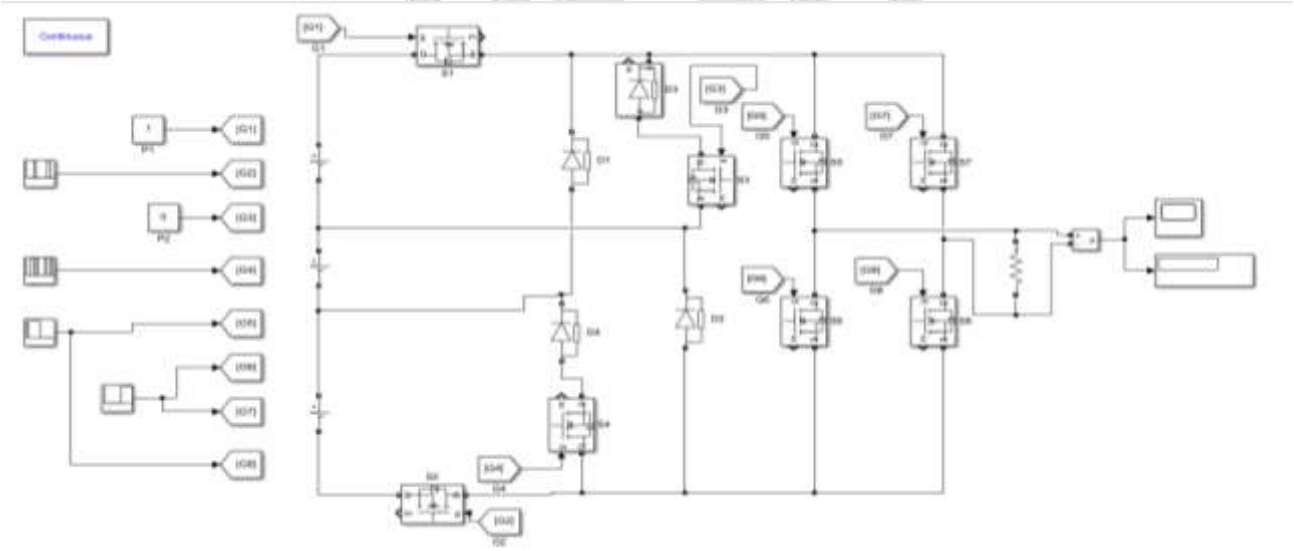


Fig. 6 MATLAB/Simulink model of proposed inverter topology

Fig. 7 Output voltage waveform of simulated seven level cascaded H-bridge inverter

Fig. 8 Output voltage waveform of simulated nine level cascaded H-bridge inverter

Fig. 9 Output voltage waveform of simulated eleven level cascaded H-bridge inverter

V. CONCLUSIONS

This paper presents a new assembly of multilevel inverter topology with consideration of reduced switch count. The proposed topology has been discussed in details with the basic unit with 3S-7L configuration generating 7 levels and 3S-9L generating 9 Levels, and 3S-11L generating 11 Levels. Finally, several experimental results prove the suitability and workability of the proposed topology with different type of loading combinations considering the change of switching combinations.

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