Comparison of MOSFET, MESFET, FinFET and SOI-FinFET

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Abstract:
In this paper we discuss about different transistor devices like MESFET, MOSFET, FinFET, SOI-FinFET. We comparing all devices structures, drain current and voltage characteristics, operating speed, drain induced barrier lowering and delay. Through this analysis we get which device has better characteristics compared to other devices.

I. INTRODUCTION

Now adays growth of technologies is rapid developed. To this growth device structure plays basic and important role. basically, Transistors are two types there are BJT (Bi-polar Junction Transistor) and FET (Field effect transistor). The BJT having two types Npn and Pnp BJT and FET are also different types they are MOSFET (Metal Oxide Semi-Conductor FET), FinFET, SOI-FinFET (Silicon on Insulator FinFET), IGFET (Insulated Gate FET) and MESFET (Metal Semi-Conductor FET) shown in below figure(a). every device having advantages and disadvantages, suppose BJT and FET having some draw backs to overcome this, MOSFET is implemented. Later while decreasing the channel length means reducing the nano meters, MOSFET having drawbacks like short channel effect, parasitic capacitance etc. To overcome these drawbacks FinFET is implemented. FinFET also some drawbacks like DIBL (Drain Induced Barrier Lowering) to over this SOI-FinFET is implemented. SOI-FinFET having good threshold swing compared FinFET and other devices. DIBL is also very less in SOI-FinFET compared to the FinFET. Short channel effect is less in SOI-FinFET compared to the FinFET and other devices. SOI-FinFET gives good parameter in very low technologies. Cut Off Region: In cut, off region transistor is in OFF state. Means current flow through the transistor is '0'.
Saturation Region: In saturation region transistor is in ON state and in this region, transistor acts as a closed switch. Means current flow through the transistor is high.
Active Region: in this active region transistor acts as an amplifier.

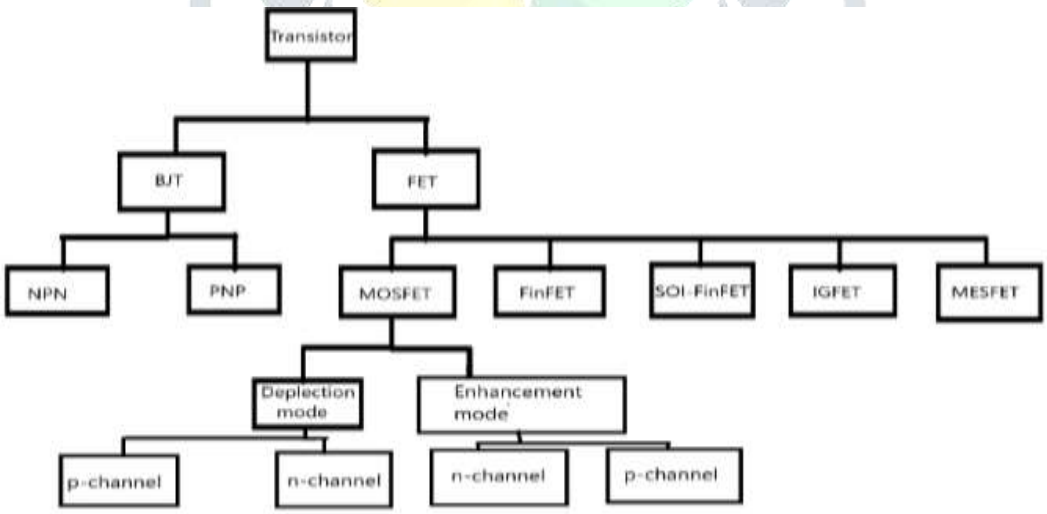

Figure1: Transistor architecture

II. Theory

Basically, Field Effect Transistors (FET) controls the flow of electrons and holes by using electric field. It is a three-terminal device. Terminals are Gate, Source and Drain. These field effect transistor uses electron or holes as charge carriers in operation. The conductivity between source and drain is depending upon the gate voltage 'Vg'. If gate voltage is '1' then the conductivity between source and drain is high. If the gate voltage is '0' then conductivity between source and drain is low. We have different types of FETS, in that MOSFET is most widely used transistor.

2.1 MOSFET

MOSFET is having four terminals Source, Drain, Gate and Body. It is also known as Insulated gate FET. The MOSFET body terminal is always connected with source terminal. So, it forming three terminals like whereas FET. MOSFET is a transistor and

it is used in both digital and analog circuits. It is voltage control device. In MOSFET, gate controls the flow of current from source to drain. MOSFET having two mode, one is Depletion Mode and an-other one is Enhancement Mode. In Depletion mode already inversion layer present without giving any voltage at gate terminal. if the gate voltage is '0' then the current flow between Source and Drain is maximum. Else if gate voltage is not '0' or increasing gradually, then the current flow between Source and Drain is '0' or decreasing gradually. In Enhancement mode, normally there is no inversion layer present without giving gate voltage. If the gate voltage increasing gradually, then the current flow from Source to Drain increasing gradually. If there is no voltage on the gate terminal, then there is no current flow from Source to Drain. In MOSFET, while decreasing the Nano-meter technology short channel effect is increases. It consumes more power compared to the FinFET technology. The fabrication steps are more compared to the FinFET. Current leakage and Drain Induced Barrier Lowering are more compared to the FinFET.

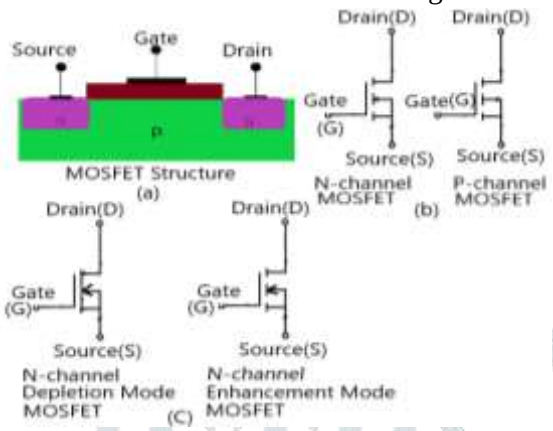

Figure 2: (a) Structure of MOSFET. (b) N, P-channel MOSFET symbols. (c) N-channel Depletion mode and Enhancement mode MOSFET symbols.

2.2 FinFET

FinFET is totally different from the MOSFET. In FinFET source and drain structure is look like a Fin and that Fin is incusing into the substrate is shown in below figure. The channel surface is fully surrounded by the gate. Because to get the good command on the channel. Then gate having good control on the channel. In FinFET, doping of impurities is very less compared to the MOSFET. In FinFET, direct connection between source, drain and substrate due to this connection some amount of leakage takes place. Due to the good control on the channel by gate terminal, leakages are highly reduced. There are two ways to increase the drive current of FinFET device. One way of increasing the width of the channel and another way is construct and connect the multi-Fins together. Short channel effect (SCE) is also reduced due to the less doping and good control by the gate. Compared to the SOI-FinFET, FinFET not gives good parameter of SCE, DIBL, leakages, Power consumption and output current.

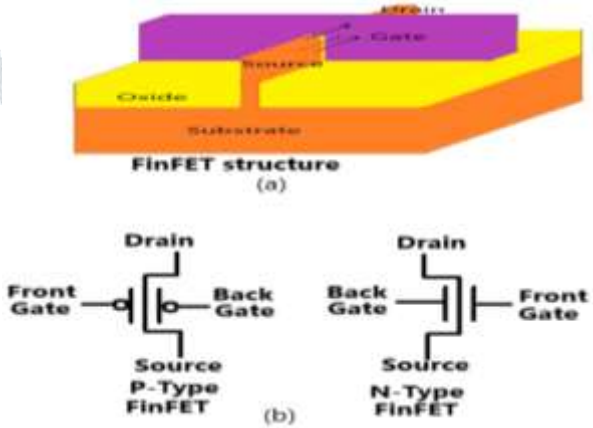

Figure 3: (a) FinFET Structure. (b) FinFET Symbols

2.3 MESFET

MESFET is a Metal Semiconductor Field Effect Transistor. Depletion mode MESFET are widely and mostly used in the circuits. MESFET having no oxide layer present between the gate and substrate. Schottky junction is present in the place of oxide junction. The Schottky metal gate controls the flow of electron from source to drain. MESFET having conducting channel between the source and drain shown in the below Figure4. Compared to the MOSFET, MESFET having higher mobility carriers in the channel. MESFET substrate is semi-insulating substrate means MOSFET substrate is made with silicon, but in MESFET the substrate is made with Gallium Arsenide (GaAs) or Indium Phosphide or Silicon Carbide. In this paper considering semi-insulating GaAs substrate. GaAs substrate provide two advantages compared to Silicon substrate. Frist, at room temperature electron mobility is more than five times large. Second, fabrication of Semi-Insulating GaAs substrate is possible and due to the free carrier absorption, it overcomes the microwave power absorbing problem in the substrate. The flow of current is controlled by varying the depletion region. Due to this, carriers from the surface is separated by depletion region. Schottky diode turn on at 0.7V. if the gate voltage increases, it decreases the current flow between source to drain, due to increasing the width of depletion region.

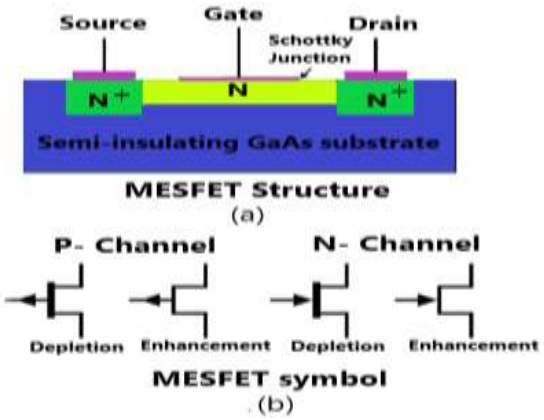

Figure 4: (a) MESFET structure. (b) MESFET symbol.

2.4 SOI-FinFET

SOI-FinFET is almost similar to the FinFET. There is small difference i.e. The substrate of SOI-FinFET is fully occupied by oxide layer or Buried Oxide layer (BOX). But in FinFET source and drain are directly connected with the substrate and there is no oxide layer present between the substrate and source, drain. Due to this BOX layer very, less leakages will occur compared to the MOSFET, FinFET and MESFET. SOI-FinFET switches faster than other devices like MOSFET, FinFET and MESFET. DIBL is also less compared to the MOSFET, FinFET and MESFET. Gate terminal having more control on the channel compared to the MOSFET, FINFET and MESFET. Drain current also more drawn at the output and doping impurities is very less compared to the MOSFET, FinFET and MESFET. The fabrication steps are also very less steps required compared to the MOSFET, FinFET and MESFET.

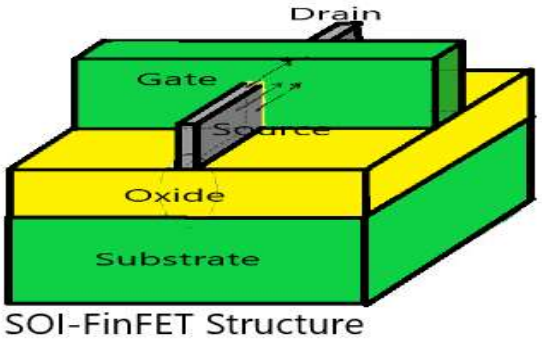

Figure 5: SOI-FinFET Structure

III. RESULTS AND DISCUSSION

3.1 Drain Induced Barrier Lowering

Due to the short channel effect DIBL will occur. If we increasing the drain terminal voltage greater than gate voltage. There is losing of connection between the source and drain. SOI-FinFET having less DIBL value compared to other devices MOSFET, FinFET and MESFET. Because SOI-FinFET doping impurities are very less compared to the MOSFET, FinFET and MESFET. The values of the MOSFET, MESFET, FinFET and SOI-FinFET is shown below tabular form and the graphical represent is also shown below.

Table 1: Comparison DIBL value of different devices.

S.NO	Devices	DIBL (mV)
1	MOSFET	47
2	MESFET	120
3	FinFET	0.000053
4	SOI-FinFET	0.00005

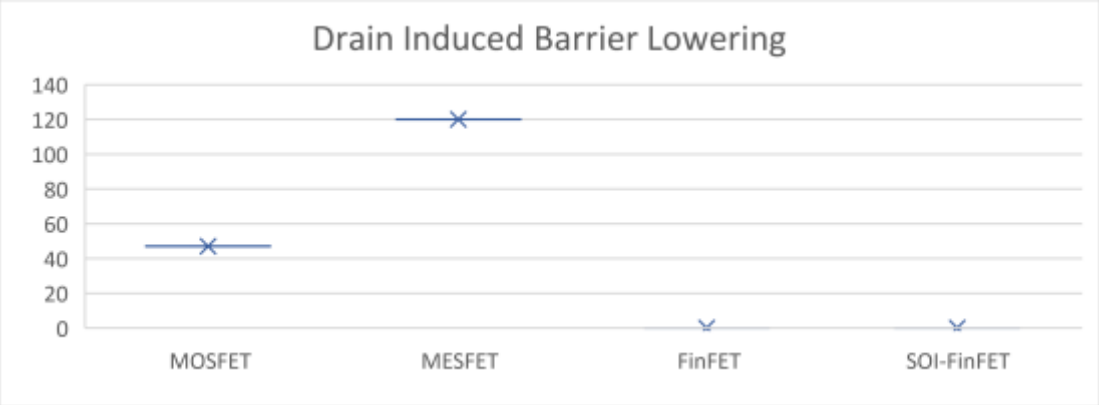

Figure 6: Graphical representation of DIBL of different devices is shown in above.

3.2 Leakage Current

Current leakage is occurring mainly between source and drain when device in OFF state. MOSFET and MESFET current leakage is very high compared to the FinFET and SOI-FinFET. Compared to the SOI-FinFET (7.77x10^-8 nA), FinFET having more leakage is about 8.62x10^-8 nA. Current leakage of MOSFET, MESFET, FinFET and SOI-FinFET is shown below tabular form.

Table 2: Comparison of current leakages of different devices.

S.NO	Devices	Leakage Current
1	MOSFET	High
2	MESFET	High
3	FinFET	Less (8.62x10^-8 nA)
4	SOI-FinFET	Very Less (7.77x10^-8 nA)

3.3 Short Channel Effect

Short channel effect will increase, by decreasing the nano-meter technology. In MOSFET decreasing the nano-meter, SCE will increase rapidly. To overcome this FinFET is used. SCE is very less in FinFET, even nano-meter is decreasing. But compared to the FinFET, SOI-FinFET having less SCE. Because the doping impurities is very less in SOI-FinFET. Comparison of SCE of different devices is shown in below tabular form.

Table 3: Comparison of SCE of different devices.

S.NO	Devices	SCE
1	MOSFET	High
2	MESFET	High
3	FinFET	Less
4	SOI-FinFET	Very Less

3.4 Subthreshold Slope

Subthreshold slope is good swing that device performance better parameter than other devices. The subthreshold slope of MOSFET is 70mV per dec at room temperature. The subthreshold slope is displaying a fast transition between ON and OFF states of the device. FinFET having good subthreshold slope is about 0.982. but subthreshold slope of SOI-FinFET is 0.062, it is better than FinFET. MESFET Subthreshold voltage is also same MOSFET and it is also not better than the SOI-FinFET. Comparison of the Subthreshold slope of different devices is shown below tabular form.

Table 4: Comparison of subthreshold slope of different devices is shown below.

S.NO	Devices	S.S V/dec
1	MOSFET	0.70
2	MESFET	~0.60
3	FinFET	0.982
4	SOI-FinFET	0.062

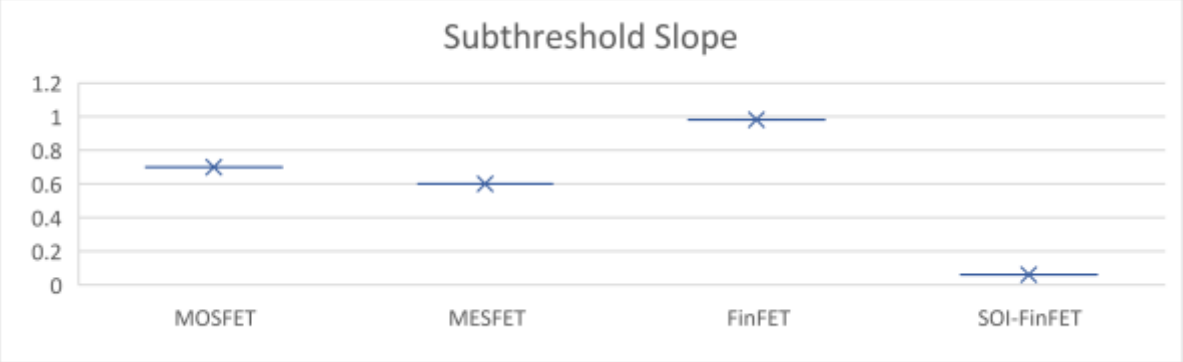

Figure 7: Graphical representation of Subthreshold slope of different devices is shown above.

IV. Conclusion

In this study, by considering all the results SOI-FinFET gives better parameter values compared to other devices MOSFET, MESFET and FinFET. SOI-FinFET shows good performance in subthreshold slope compared to MOSFET, MESFET and FinFET. In DIBL, less value given by the SOI-FinFET only compared to the MOSFET, MESFET and FinFET. SCE is also high reduced by the SOI-FinFET by compared to the MOSFET, MESFET and FinFET. Switching speed is also faster in SOI-FinFET compared to the MOSFET, MESFET and FinFET. Soi-FinFET having very less Current leakages and power dissipation compared to MOSFET, MESFET and FinFET.

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