FPGA implementation of Universal Biquadratic Filter

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Abstract: In this paper, a Universal Biquad Filter is designed with the help of the XILINX FPGA tool. This paper presents concept of universal filter using the FPGA model. Analog filters are basically used in different types of signal processing applications mainly they are used in the designing of greater order filter structures. Biquad filter designing using XILINX is a suitable method of second order "Biquad" analog filter which is taken as a main filter in making of higher order filters. The behavior of Biquad filter makes it very unique in the design of various filtering circuits using various types of active elements because it gives very suitable results. In our proposed design Biquad filter is implemented using XILINX tool. The Biquad filter using the active type of elements, is so chosen as to get greater bandwidth, maximum speed and minimum power consumption since these parameters are major considerations in design of any filter circuit. The simulation results are validating and the layout of the Universal Biquad filter is also designed using XILINX TOOL.

IndexTerms **- CMOS, XILINX FPGA, Static Power, Dynamic Power, Ambient temperature.**

I. INTRODUCTION

Active filter is mainly applied in the stream of electrical engineering. They are mainly found in cross over type network that uses in a three-way higher fidelity loud speaker, portable type ECG detection technique is used in front end circuits and touch-tone telephone are mainly useful for the purpose of tone decoding. Several active devices are basically used to design tunable active filters, i.e. OTA, OP-AMP, CDTA, second generation current-controlled current conveyor. The Biquad filter is helpful in designing all the filter in the same circuit. A significant type of element of main structure is the desirable of three essential filter move capacities, i.e., low-pass (LP), band-pass (BP), and high-pass (HP) at the same time. Likewise, Filter tuning should be possible without altering the quality factor of the circuit. Biquad filter offers low latent and dynamic sensitivities, low segment spread and great dependability. Be that as it may, generally high number of resistors can be an inconvenience of the Op-Amp based voltage-mode working old style structure, other than its recurrence data transmission constraint. So as to beat the constrained recurrence transmission capacity properties of the operational amplifier. The important filter characteristics are band pass frequency range, bands top frequency range, low attenuation in the stop band, large allowable ripple in the pass band, required phase characteristics, desirable transient parameters, input and output impedances and noise ratio parameters etc.

filters are commonly described with the help of a transfer functions. The defined expression for the Biquad filter transfer function is basically obtained in the form as:

$$H(s) = \frac{a_2 s^2 + a_1 s + a_o}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2}$$

These various types of filter low pass filter (LPF), high pass filter (HPF) and band pass filter (BPF), are realized with the help of the numerator coefficients as described in the given equations.

$$H_{LP} = \frac{a_o}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2} \qquad H_{HP} = \frac{a_2 s^2}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2} \qquad H_{BP} = \frac{a_1 s}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2}$$

2. PROPOSED BIQUAD FILTER CIRCUIT

Biquad filter can be designed with the help of Xilinx tool. With the help of Biquad filter all the filter can be designed LPF, HPF and BPF all are designed in the same circuit. The simulation is also performed on the Xilinx tool. The main purpose of this circuit is to initialize the system and to prepare incoming data for further processing. Before exploring the actual design, brief explanations of the I/O ports will be given to help better understanding of this subsystem.

- DATA_IN – This is the pseudo-random test data from DataGen, which are used to evaluate the signal bandwidth.
- COEF_IN – This is the incoming data from Simulink, including the coefficients of the filter and controlling header, all of which are grouped as a frame obeying the established protocol.
- END – This is a signal from the DataGen module identifying the end of one successful run when it is active.
- COEF_OUT – This is the set of cached coefficients that are sent to the memory block in the Biquad module.
- DATA_OUT – The test data which are multiplied by normalization factor g.
- MOD_NUM – This is the total number of SOS sections for the filter module.
- COEF_FEED_EN – The enable signal for feeding coefficients into the Biquad when the data is prepared and ready.
- COEF_INI – An initialization signal for all modules to reset their RAMs.

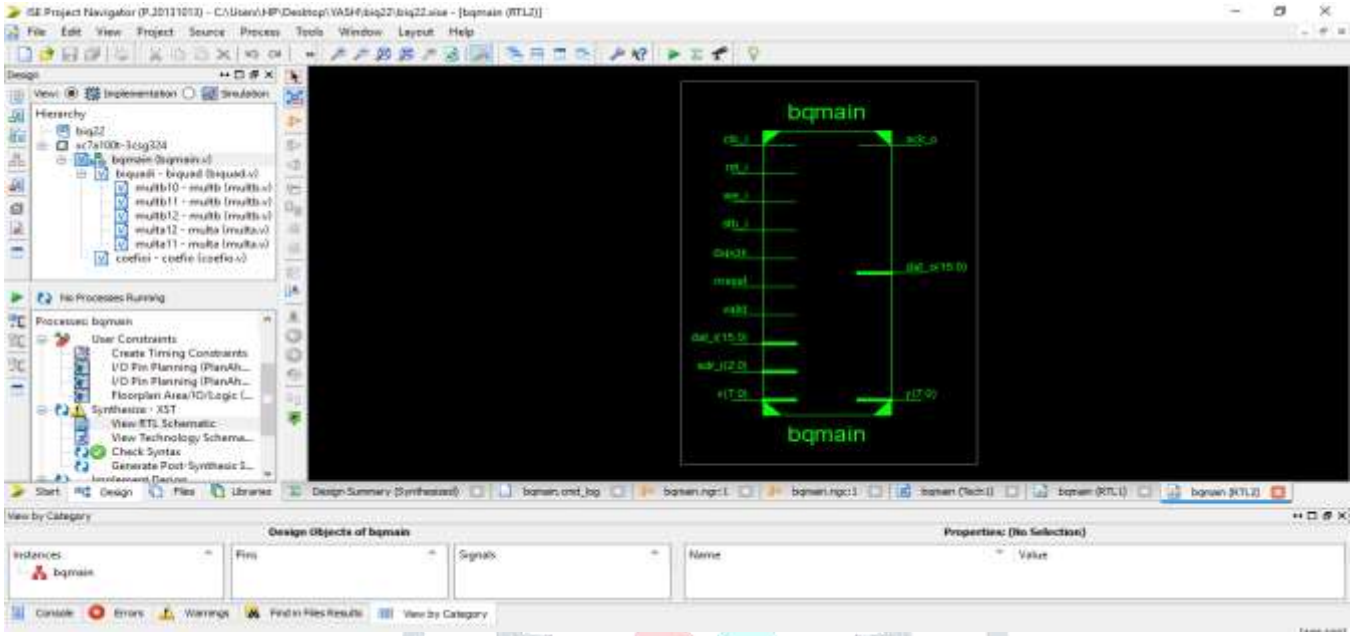

Figure 1: Biquad filter circuit designing on Xilinx 14.7 tool

2.1 BIQUAD FILTER RTL SCHEMATIC DIAGRAM

The RTL schematic of Biquad filter has been done using the Xilinx FPGA tool.

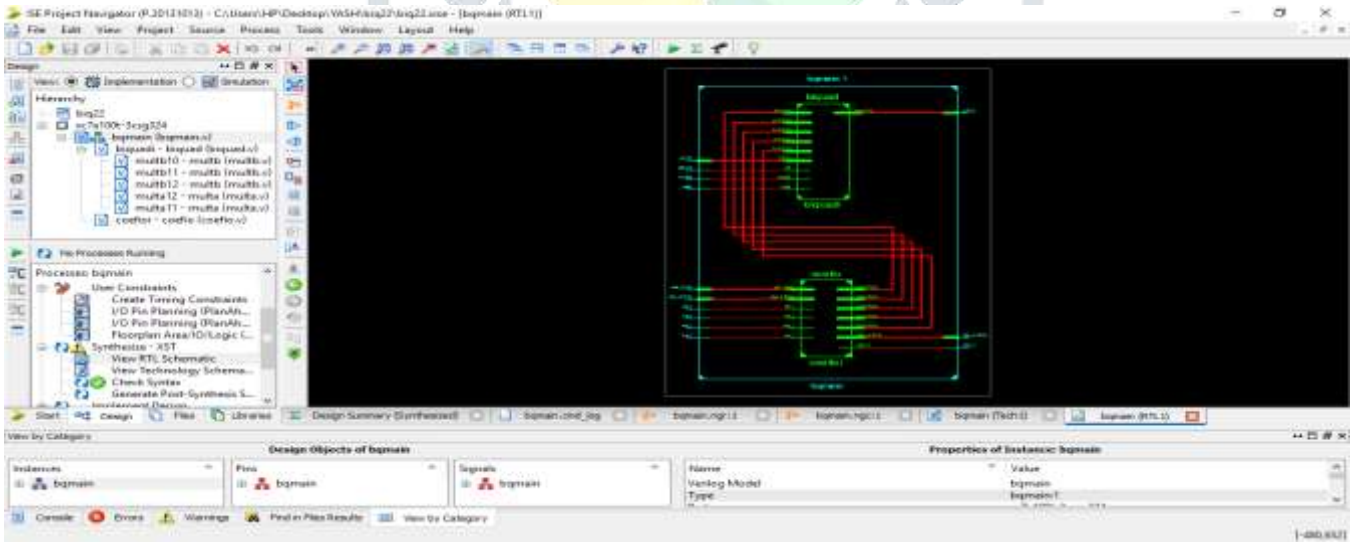

Figure 2: Biquad filter circuit RTL Schematic diagram

2.2 BIQUAD FILTER TECHNOLOGY SCHEMATIC DIAGRAM

The Technology schematic of Biquad filter has been done using the Xilinx FPGA tool.

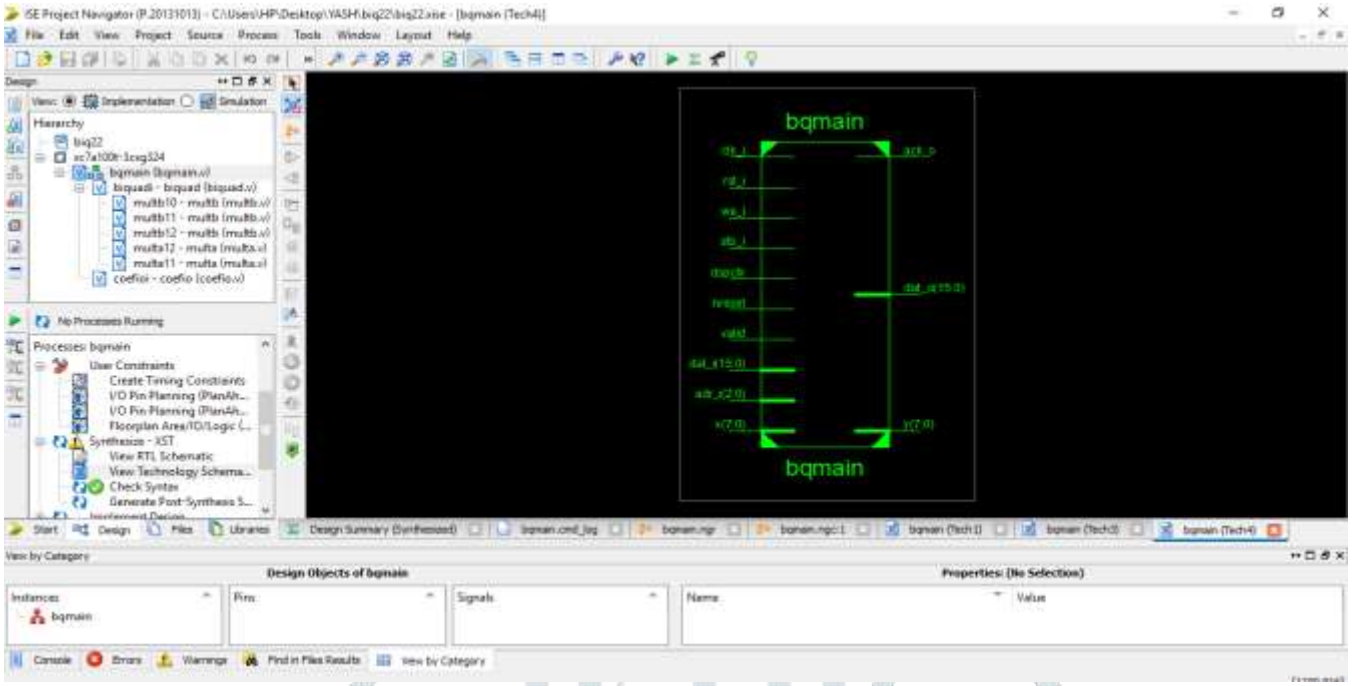

Figure 3: Biquad filter circuit Technology Schematic diagram

2.3 BIQUAD FILTER DETAILED TECHNOLOGY SCHEMATIC DIAGRAM

The Technology schematic of Biquad filter has been done using the Xilinx FPGA tool.

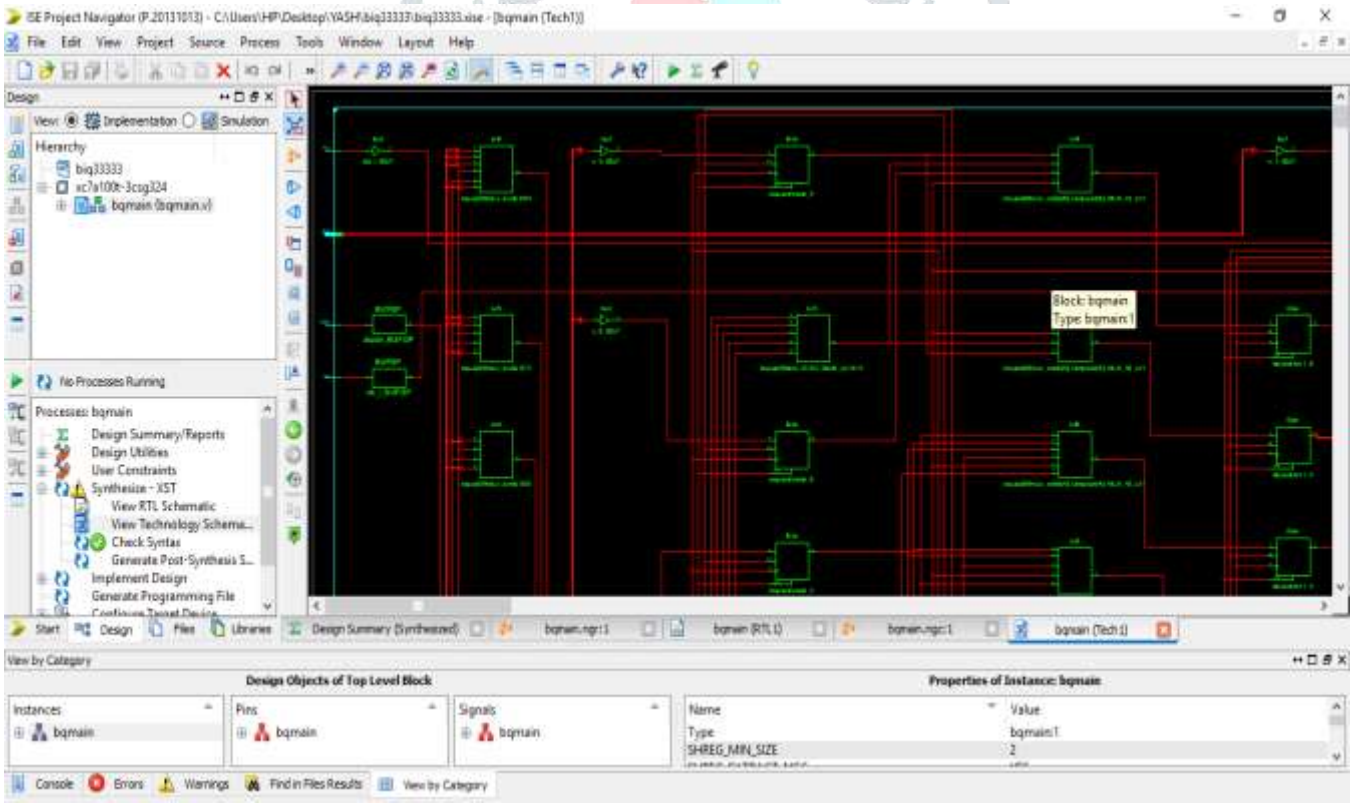

Figure 4: Biquad filter circuit detailed Technology Schematic diagram

2.4 BIQUAD FILTER FULL SCHEMATIC DIAGRAM

The full schematic of Biquad filter has been done using the Xilinx FPGA tool. For an FPGA design, extra circuits mean higher costs of area, power and delay. After comparing the costs, complexities and performances from simulations was selected.

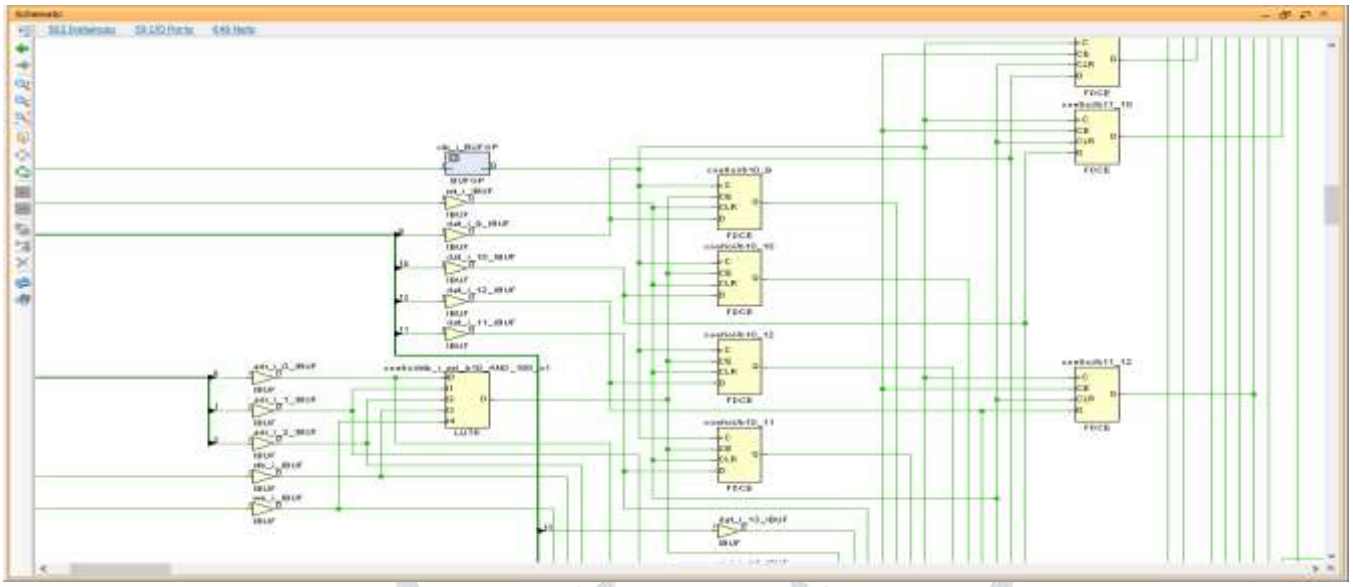

Figure 5: Biquad filter circuit full Schematic diagram

2.5 BIQUAD FILTER DETAILED WIRED SCHEMATIC DIAGRAM

The detailed wired schematic of Biquad filter has been done using the Xilinx FPGA tool.

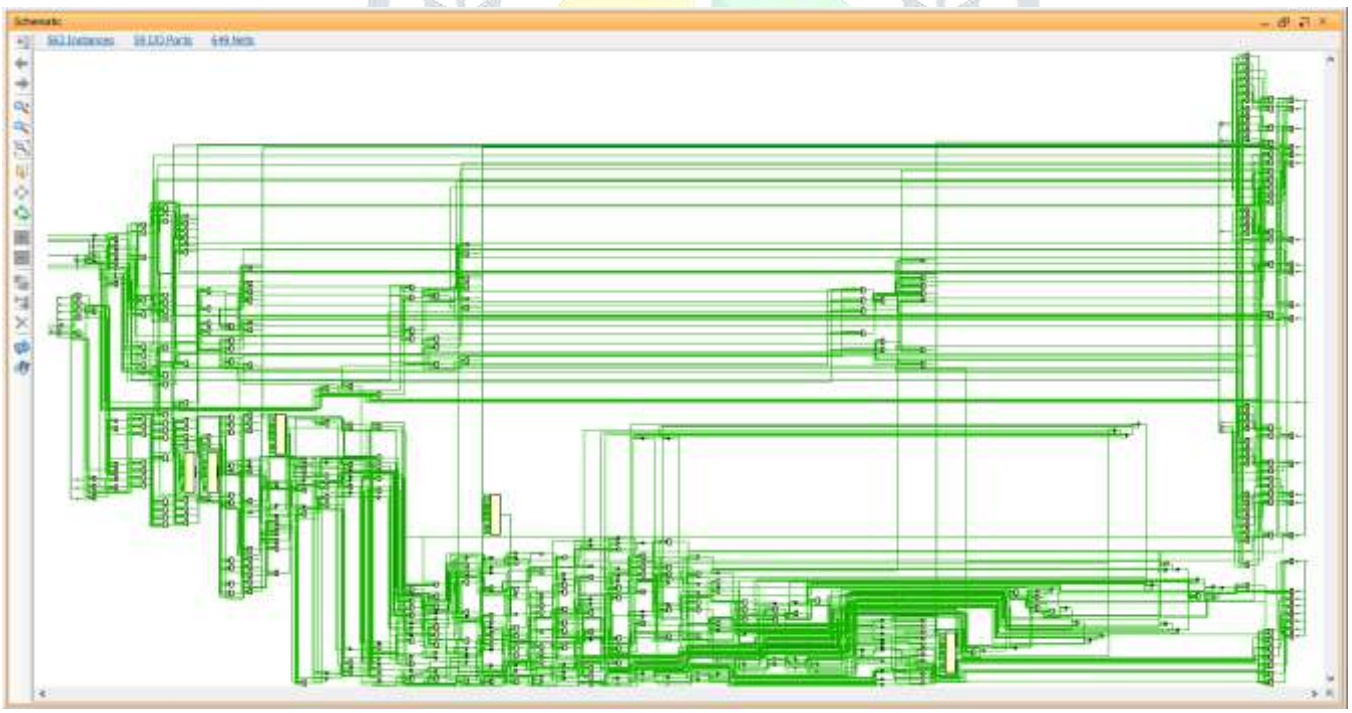

Figure 6: Biquad filter detailed wired schematic diagram

2.6 BIQUAD FILTER WAVEFORM USING XILINX TOOL

The waveform of Biquad filter has been done using the Xilinx FPGA tool.

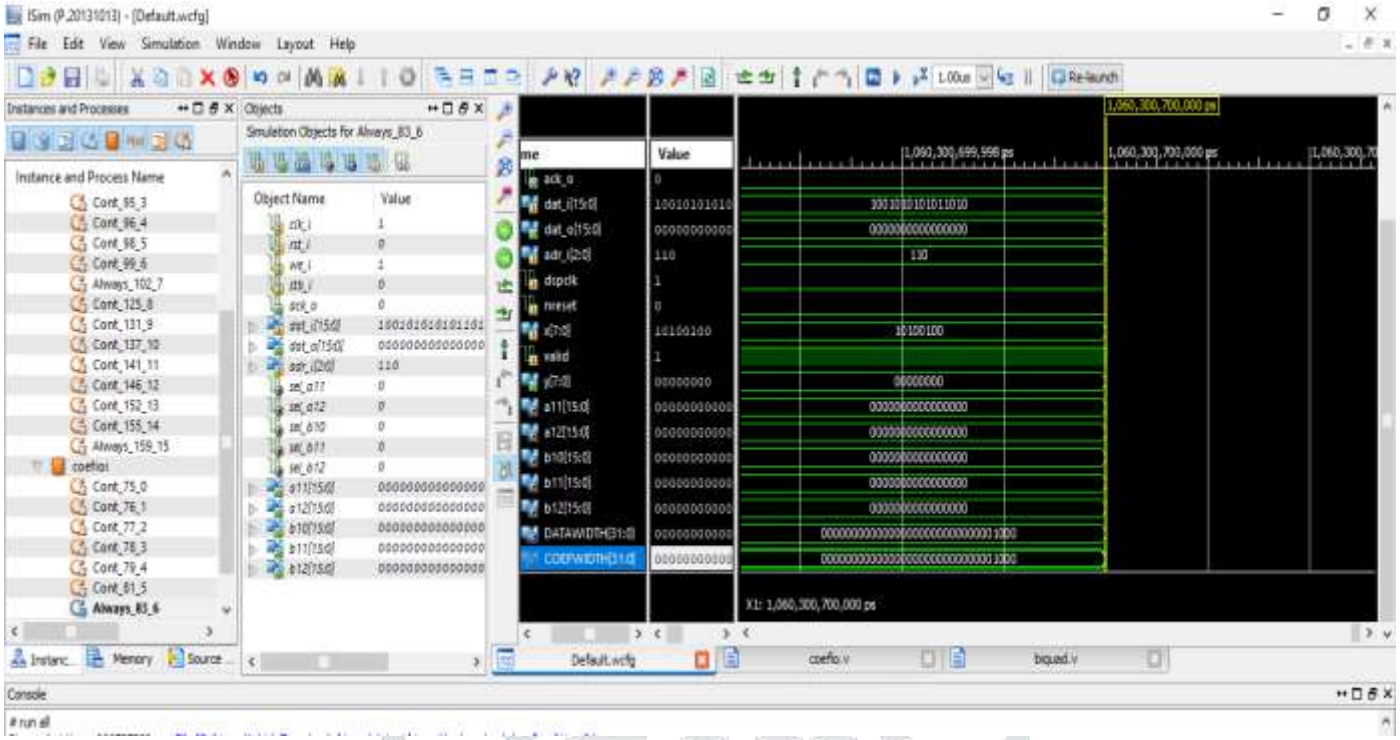

Figure 7: Biquad filter waveform using Xilinx tool

3. SIMULATION AND RESULTS:

The propose circuit are validate using XILINX FPGA tool. This mechanism prevents the hardware implementation from wasting power to refresh the cache memory for an identical set of coefficients. It significantly reduces the power consumption, which is one of the crucial criteria for evaluating the performance of an FPGA design. The analysis is taken on the basis of power calculated with the help of the tool. Various other parameters of Biquad filter are also being determined with the help of this tool. Overall power is being calculated, clock variation report, HDL synthesis report, timing and delay report, toggle analysis are also calculated. The layout of the Biquad filter is also shown in the analysis portion.

3.1 POWER CALCULATION USING VARIOUS TOOLS:

The power of Biquad filter has been calculated with the help of XILINX FPGA tool.in the below figure (8) the power comes under the biquad filter using XILINX tool is 0.1777amp. The thermal properties and ambient temperature are shown in the figure (8).

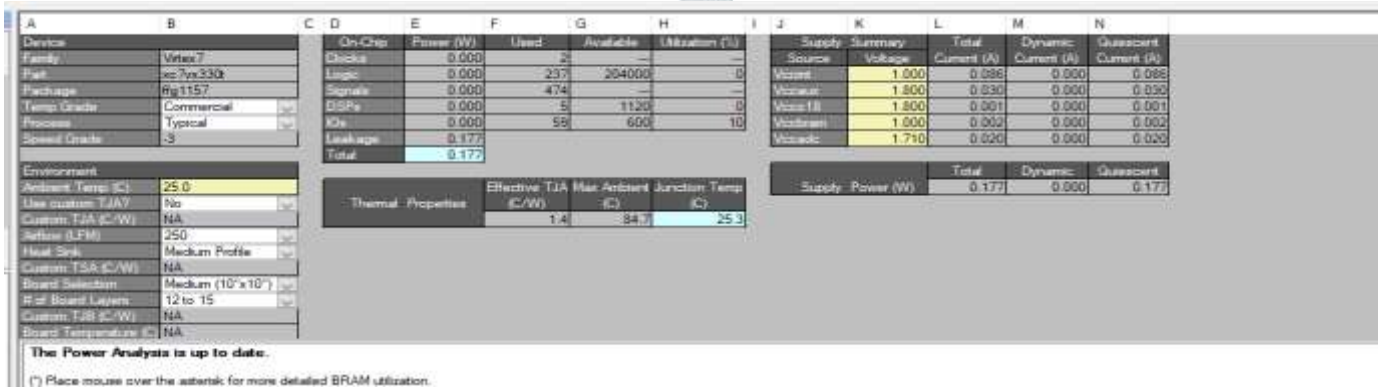

Figure 8: Calculation of the power in the Biquad filter

In the figure (8) power calculation using the XILINX tool is presented.

3.2 CLOCK VARIATION REPORT

The proposed circuit values under the clock variation has been shown. It basically shows all the source rise time and the fall time of the given circuit.

```
Clock to Setup on destination clock dspclk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk_i          |    5.518|         |         |         |
dspclk         |    5.025|         |         |         |
---------------+---------+---------+---------+---------+
```

Figure 9: Clock variation report

3.3 PROPOSED CIRCUIT DESIGN SUMMARY REPORT

The proposed circuit design summary report has been shown. It basically shows how many flip flops, clock buffers and IO buffers are present in the circuit while designing.

```
*                            Design Summary
=========================================================================

Top Level Output File Name          : bqmain.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                              : 302
#      GND                          : 1
#      INV                          : 11
#      LUT1                         : 1
#      LUT2                         : 5
#      LUT3                         : 30
#      LUT4                         : 62
#      LUT5                         : 37
#      LUT6                         : 33
#      MUXCY                        : 59
#      VCC                          : 1
#      XORCY                        : 62
# FlipFlops/Latches                 : 198
#      FDCE                         : 198
# Clock Buffers                     : 2
#      BUFGP                        : 2
# IO Buffers                        : 57
#      IBUF                         : 32
#      OBUF                         : 25
# DSPs                              : 5
#      DSP48E1                      : 5
```

Figure 10: Proposed circuit design summary report

3.4 PROPOSED CIRCUIT HDL SYNTHESIS REPORT

The proposed circuit HDL synthesis report has been shown. It basically shows how many registers, adders and multiplexers are present in the circuit while designing.

```
=========================================================================
HDL Synthesis Report

Macro Statistics
# Multipliers                                          : 5
 11x7-bit multiplier                                   : 2
 7x7-bit multiplier                                    : 3
# Adders/Subtractors                                   : 12
 14-bit addsub                                         : 4
 32-bit adder                                          : 8
# Registers                                            : 17
 12-bit register                                       : 1
 14-bit register                                       : 4
 16-bit register                                       : 5
 8-bit register                                        : 7
# Multiplexers                                         : 16
 1-bit 2-to-1 multiplexer                              : 7
 14-bit 2-to-1 multiplexer                             : 1
 16-bit 7-to-1 multiplexer                             : 1
 32-bit 2-to-1 multiplexer                             : 6
 8-bit 2-to-1 multiplexer                              : 1
# Xors                                                 : 5
 1-bit xor2                                            : 5
```

Figure 11: Proposed Circuit HDL Synthesis report

3.5 PROPOSED CIRCUIT TIMING AND DELAY REPORT

The proposed circuit timing analysis report has been shown. It basically shows the clock period of 5.027ns and the total number of paths and ports in the circuit while designing. All the delays in the circuit are necessary for the synchronization between different components in the circuit. They are also helpful to increase the driving ability and to reduce the probability of having timing issues after realization.

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 5.027ns (Maximum Frequency: 198.938MHz)
   Minimum input arrival time before clock: 1.194ns
   Maximum output required time after clock: 1.605ns
   Maximum combinational path delay: 1.479ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'dspclk'
  Clock period: 5.027ns (frequency: 198.938MHz)
  Total number of paths / destination ports: 20863 / 110
```

Figure 12: Timing and delay report

3.6 PROPOSED CIRCUIT FAN IN FANOUT REPORT

The proposed circuit fan in fanout analysis has been shown. It basically shows all the signal rate and the slice fanout of the given circuit.

Name	Power (W)	Signal Rate	% High	Fanout	Slice Fanout	Clock
biquadi/nreset_inv	0.00000	0.0	1.0	118	33	Async
nreset_IBUF	0.00000	0.0	99.0	1	1	Async
rst_i_IBUF	0.00000	0.0	1.0	80	20	Async

Figure 13: Proposed circuit fan in fanout report

3.7 PROPOSED CIRCUIT TOGGLE RATE REPORT

The proposed circuit toggle rate analysis has been shown. It basically shows all the toggle rate and the reset toggle values of the given circuit.

Name	Value	Range
FF Toggle Rate (%)	12.5	0.0 to 200.0
I/O Toggle Rate (%)	12.5	0.0 to 200.0
Output Load (pF)	5.0	0.0 to 1000000.0
I/O Enable Rate (%)	100.0	0.0 to 100.0
BRAM Write Rate (%)	50.0	0.0 to 100.0
BRAM Enable Rate (%)	50.0	0.0 to 100.0
Set/Reset Probability (%)	1.0	0.0 to 100.0
Set/Reset Toggle Rate (%)	1.0	0.0 to 200.0
Enable Probability (%)	99.0	0.0 to 100.0
Enable Toggle Rate (%)	1.0	0.0 to 200.0
DSP Toggle Rate (%)	12.5	0.0 to 200.0

Figure 14: Proposed circuit toggle rate analysis report

3.8 PROPOSED CIRCUIT LAYOUT DIAGRAM

The proposed circuit Biquad filter zoomed layout diagram has been shown. It basically shows all connections of the layout of the given circuit.

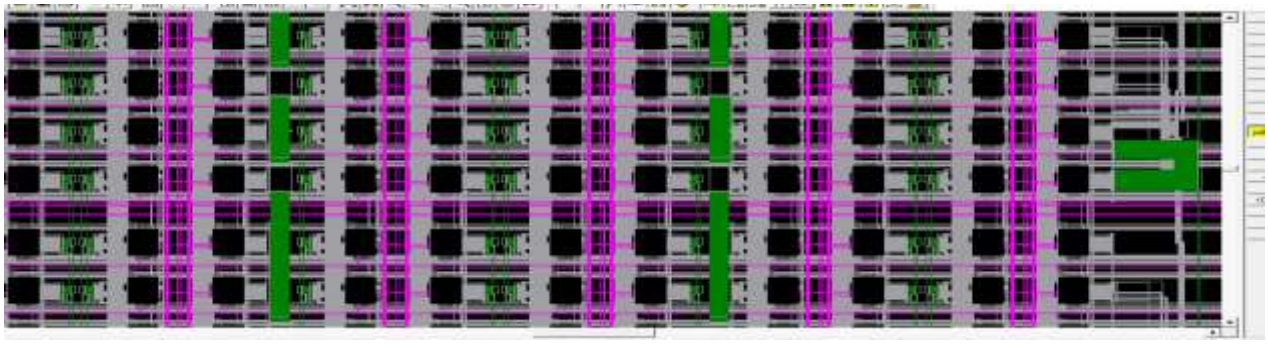

Figure 15: Layout of proposed Biquad circuit using OTA

4. CONCLUSION

In this paper the modification in the Biquad filter circuit is been designed according to the optimization to a combination of power, delay and area consumption for the FPGA. Design method is useful in adding an extra input port for the hardware model to allow the inputting of test data from external sources, such as an analog-to-digital converter. It would also be desirable to migrate all of the software modules to the hardware design including the evaluator or even the DE optimization engine. The main purpose of this design is to create a System-on-a-Chip (SOC) that contains everything in this paper which can accelerate the optimization of a circuit. The power of the Biquad filter is also calculated using the XILINX tool and the layout is also presented for understanding the path of the various signal.

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