Experimental Validation of Asymmetric Multilevel Inverter with Single Phase Transformer

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Abstract— In this paper, the hardware implementation of the modified asymmetric multilevel inverter with a single-phase transformer is presented. The multilevel inverter has been enforced for reducing the bulkiness of the LC filter size as well as the cost of the system. Since the inverter is fed by a three asymmetric DC source, asymmetry is enforced providing multiple redundant switching patterns to synthesize an output signal of 13 levels. Optimum switching patterns are developed for the proposed ratio which allows reducing typical switches count as well as harmonics to 5% under IEEE standards. .The concept of reduced device count ensures the size of hardware as well as the cost and complexity of the hardware. The main drawback of multilevel inverters is, requires a high number of switching devices leads to complex control. The proposed topology utilizes three asymmetrical dc voltage sources alongside, ten power semiconductor switches to accomplish thirteen levels at the output. Compared to the conventional topologies, the proposed inverter has less number of switches as well as fewer harmonics content. Transformer based multilevel inverter is expected to give isolation protection. The proposed cascaded H-bridge topology has high efficiency as well as balanced power distribution quality. The simple PWM technique is utilized for the generation of pulses to the multilevel inverter switches which increase the simplicity of the control. Further, extensive hardware validation shows the effectiveness of the system.

Keywords— multi level inverter, THD, CHB topology, asymmetric transformer.

I. INTRODUCTION

The idea of multilevel inverter (MLI) advanced path back in 1981 with creators of [1] proposing a novel topology for expanding the quantity of levels in a traditional two level inverter in this manner enhancing the power quality. Nowadays the demand of MLI growing rapidly in the field of power conversion i.e. from DC/AC, AC/DC & DC/DC, conversion of frequency with varying output etc. and their applications. These converters offers a better

and more sinusoidal output voltages indicating low THD, high efficiency and power factor. In Conventional topology, there are mainly three types of multilevel converters- diode clamped type, Flying Capacitor type (single common source & neutral point clamped).

Diode Clamped type inverters have the advantages of increased efficiency, simple control & less harmonic content with increased level without the necessity of filters. But having drawbacks due to using excessive no. of clamping diodes with increasing steps & difficult to control real power flow of individual converter in multi converter system. Cascaded Inverters have advantages of using least nos. of components to achieve the same amount of voltage levels in comparison with diode clamped & flying capacitor type inverters.

Another advantages of using optimized circuit layout & possible packaging due to having same structure of each level & also having soft switching techniques. Cascaded multilevel converter could further be classified as symmetrical CHB converter and asymmetrical CHB converter. Symmetrical CHB converter uses a number of equal dc voltage sources while asymmetrical counterpart uses unequal voltage sources. The CHB topology has attracted researchers attention because of some shortcomings associated with NPC and FC including large capacitor requirement, unbalancing in the dc links and large stress on the power switches

An asymmetrical configuration can obtain greater number of levels at the output voltage with same number of component compared with the symmetrical counterpart.

It also improves the reliability by reducing the number of dc voltage sources. Several work has been carried out in literature notably on novel topologies for asymmetric and symmetric configuration using isolated dc voltage sources and the connection of H-bridge circuits.

The present project suggest a new hybrid MLI topology with reduction in number of p
ower switches along with dc voltage sources. Fig 1 shows the proposed block diagram.

I. PROPOSED SYSTEM

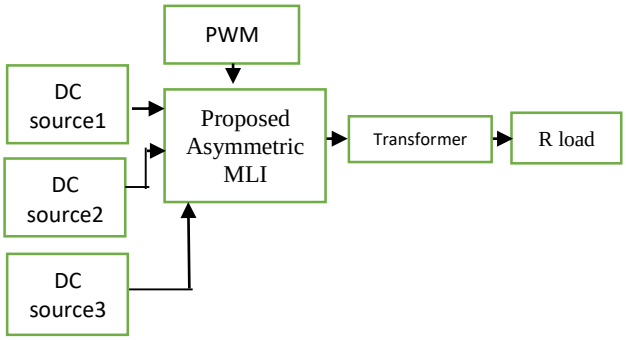

Fig 1. Block Diagram of Proposed System

The proposed system shown in figure 1 consists of three asymmetrical DC source in the ratio 1:2:3 fed to the proposed asymmetric MLI. The asymmetric MLI have the capability of producing 13 level of output voltage with the help of simple PWM control techniques. The transformer is used for the isolated protection circuit.

II. MODELS

A. *Proposed asymmetric MLI*

The proposed asymmetric MLI circuit shown in figure 2 consists of dual unit structure. One unit is responsible for the generation of voltage levels and other is responsible for the generation of AC waveform by changing the polarity of current flow through the load. The switches Q1-Q5 are responsible for the 13 level output and H1-H4 are responsible positive and negative polarity waveform.

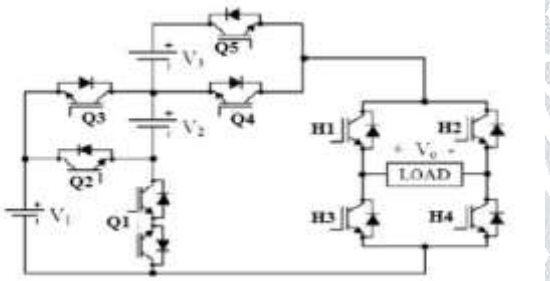

Fig 2. Circuit diagram of proposed asymmetric MLI

The circuit operation involves when switches H1&H4 are ON the positive cycle is produced likewise when the switched H2&H3 are ON the negative cycle is produced. When switches Q3&Q4 are ON the V1 (2nd level) and –V1 (8th level) are produced. Q1&Q4 are turned ON simultaneously to get the V2 (3rd level) and –V2 (9th level) are produced. Q2&Q4 are turned ON to produce the (V1+V2)4th and –(V1+V2)10th level of output voltage.Q3&Q5 are turned ON to generate the (V1+V3)5th and –(V1+V3)11th level. Q1&Q5 are turned ON to generate (V2+V3)6th and –(V2+V3)12th level. The (V1+V2+V3)13th&-(V1+V2+V3) 7th level is attained by turning ON the switches Q2&Q5. In 1st level output voltage is 0 so all the level generation switches are turned OFF during this period of level generation.

The common structure equation is given by,

$$\text{Number of switches} = \frac{1}{3}[Number\ of\ levels + 17] \quad (1)$$

$$\text{Number of sources} = \frac{1}{6}[Number\ of\ levels + 5] \quad (2)$$

The table 1 shows the switching table for the proposed asymmetric MLI switches.

Table 1. Switching table

Q1	Q2	Q3	Q4	Q5		H2	H3	H4	LEVEL
0	0	0	0	0	1	1	0	0	1
0	0	1	1	0	1	0	0	1	2
1	0	0	1	0	1	0	0	1	3
0	1	0	1	0	1	0	0	1	4
0	0	1	0	1	1	0	0	1	5
1	0	0	0	1	1	0	0	1	6
0	1	0	0	1	1	0	0	1	7
0	0	0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	1	0	8
1	0	0	1	0	0	1	1	0	9
0	1	0	1	0	0	1	1	0	10
0	0	1	0	1	0	1	1	0	11
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0	1	0	0	1	0	1	1	0	13

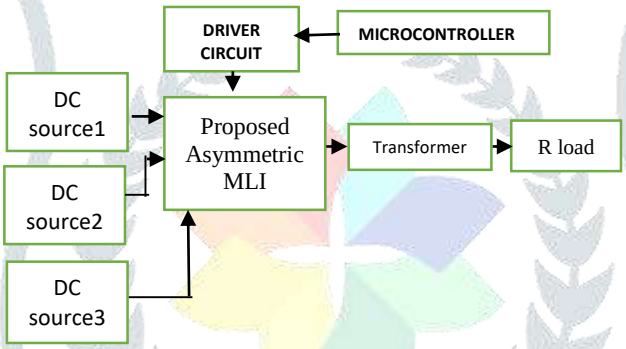

Fig 3. Block diagram of hardware implementation

Figure 3 shows the block diagram depicting hardware implementation. Three input DC voltage sources are 9v, 18v and 27v. PIC16F877A CMOS FLASH-based 8-bit microcontroller along with a driver circuit are used in the hardware implementation.

B. DRIVER CIRCUIT

A driver is an electrical circuit or other electronic component used to control another circuit or component, such as a high-power transistor, liquid crystal display (LCD), and numerous others. They are usually used to regulate current flowing through a circuit or to control other factors such as other components, some devices in the circuit.

The term is often used, for example, for a specialized integrated circuit that controls high-power switches in switched-mode power converters. Typically the driver stage(s) of a circuit requires different characteristics to other circuit stages. For example in a transistor power amplifier circuit, typically the driver circuit requires current gain often the ability to discharge the following transistor bases rapidly, and low output impedance to avoid or minimize distortion.

C. MICROCONTROLLER(PIC16F877A)

The term PIC, or Peripheral Interface Controller, is the name given by Microchip Technologies to its single – chip microcontrollers. PIC micros have grown to become the most widely used microcontrollers in the 8- bit microcontroller segment. The PIC16F877A CMOS FLASH-based 8-bit microcontroller is upward compatible with the PIC16C5x, PIC12Cxxx and PIC16C7x devices. It features 200 ns instruction execution, 256 bytes of EEPROM data memory, self-programming, an ICD, 2 Comparators,

8 channels of 10-bit Analog-to-Digital (A/D) converter, 2 capture/compare/PWM functions, a synchronous serial port that can be configured as either 3-wire SPI or 2-wire I2C bus, a USART, and a Parallel Slave Port.

III. SIMULATION RESULTS

Proposed asymmetric MLI produces 13 level output voltage of V0=54V with three different sources of V1=9V, V2= 18V, V3=27V.

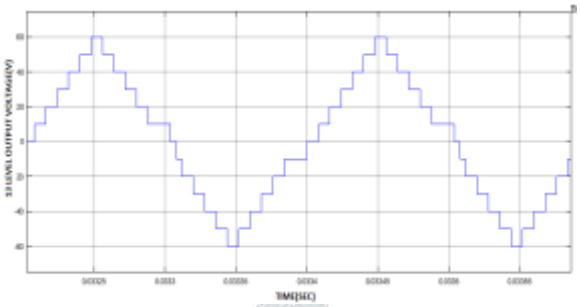

Fig 4. Thirteen Level output voltage of proposed asymmetric MLI

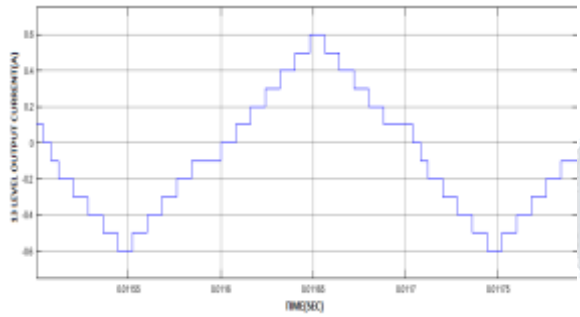

Fig 5.Thirteen Level output current of proposed asymmetric MLI

. Figure 4 and 5 shows the 13 level output voltage and output current waveform. The total harmonic distortion(THD) value shown in figure 6 is evaluated using FFT analysis which shows the value of 5.86%

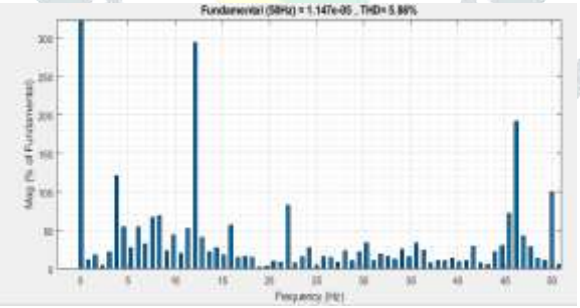

Fig 6. THD percentage

IV. HARDWARE RESULTS

Figure 7 shows the overall hardware setup of proposed asymmetric MLI which produces 13 level output voltage of V0=60V with three different sources of V1=9V, V2= 18V, V3=27V .

Fig 7. Overall hardware setup

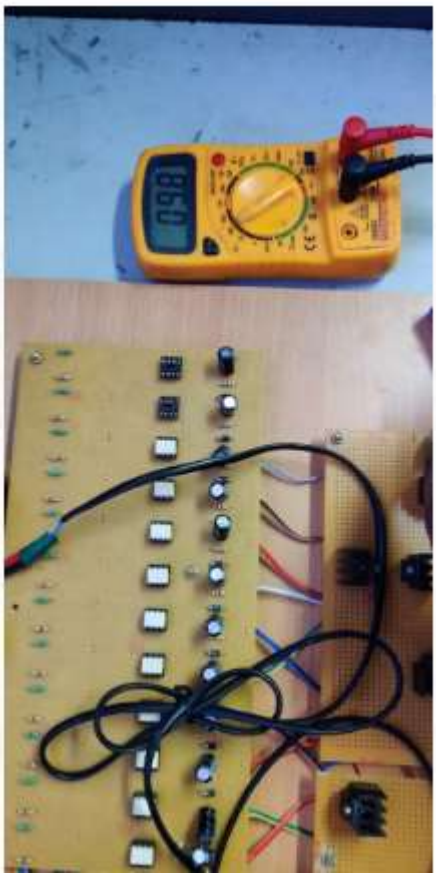

Fig 8. Input voltage1

Fig.9 Input voltage 2

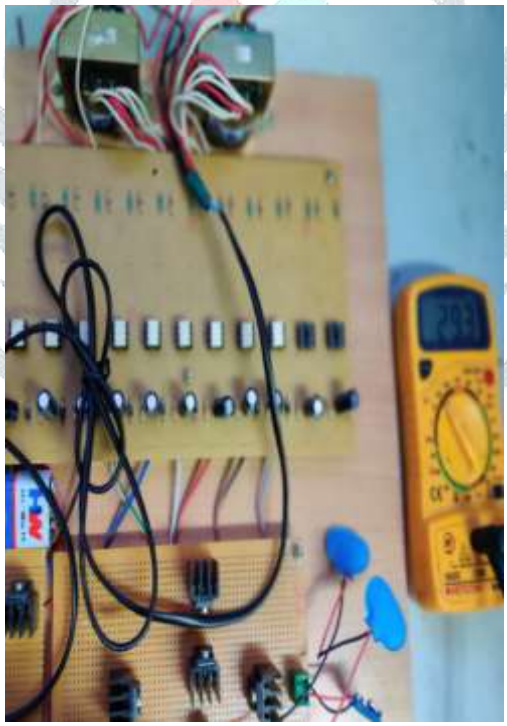

Fig 10. Input voltage3

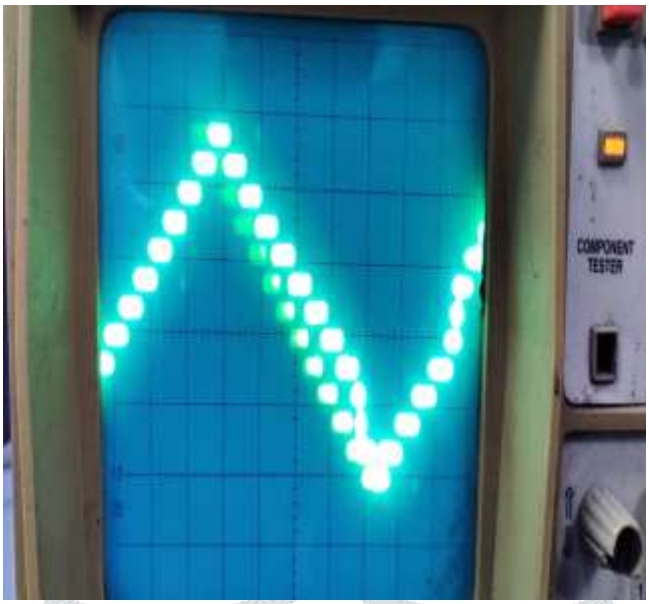

Fig 11. Thirteen Level output voltage of proposed asymmetric MLI

Figure 8, 9 nd 10 shows the input voltage 1,2&3 respectively. Figure 11 shows the thirteen level output voltage waveform. The total harmonic distortion(THD) value is evaluated using FFT analysis which shows the value of 5.86%

V. COMPARISON OF CONVENTIONAL AND MODIFIED MLI

Conventional	Modified
Conventional cascaded multilevel inverter consists of 28 switches	Modified MLI consists of only 9 switches
Conventional cascased multilevel inverter consits of 7 sources	Modified mli consists of only 3 sources
Conventional inverter are symmetrical	Modified MLI are asymmsetrical
Conventional inverter works on high frequency which is on khz	Modified MLI are works on low switching frequency

VI. CONCLUSION

This paper presented a hardware implementation modified asymmetric MLI with isolated protection which is also implemented with the use of microcontroller based control technique. The presented topology has the advantages of less reduced switch count which increases the cost effectiveness of the system. The proposed MLI exhibits the less harmonic distortion with the value of 5.86% and it can operate at low switching frequency which increases the reliability of the system. The power efficiency is also increase with balance power distribution systems.

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