DESIGN OF 7T SRAM FOR LOW POWER APPLICATIONS

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Abstract:

In today's digital era, memory is an inevitable part of any integrated device. Also it has a major part in the total circuit power. As the growing concern for portable devices is increasing day by day, the nano-technology is grabbing the eyes of the chip makers. But the drain of power in portable devices which mainly contains static random access memory. As technology scales down Leakage power places important role compared to dynamic power consumption. Hence we used Power gating technique in our Proposed SRAM memory to lower the power consumption which is the need of the day. Also we added another Feature to reduce the leakage power. Since the leakage current of NMOS is larger than that of PMOS with the same feature size. To further reduce the leakage power consumption, instead of using NMOS, the pass transistors of SRAM cells are replaced by PMOSs.

Keywords: RAM, SRAM, PMOS,NMOS.

I. INTRODUCTION

Memory organizations have become an indivisible part of modern VLSI systems. Semiconductor memory act as a standalone memory chips but also as an integral part of complex VLSI systems. The basic storage elements of semiconductor memory have remained essentially unchanged for quite some time. Time does not imply that other forms of storage cells cannot be conceived of; rather these cells offer the best trade-off between design factors such as layout efficiency, performance, area and noise sensitivity. In this chapter, we are concerned with read and write operations of MOS random access memories (RAMs). Traditional RAMs have been classified into dynamic RAMs (DRAMs) and static RAMs (SRAMs). The former typically implemented using a single-transistor storage element, where the cell state is stored as charge on a capacitor. The term dynamic refers to the need to periodically refresh the charge on no ideal storage capacitors. Static RAMs, in contrast, use a bistable element such as an inverter loop to store the cell state as a voltage differential. These elements can hold their state without the need for refreshing as long as power is applied. The basic SRAM cell is considerably more complex and occupies a larger area as compared to a DRAM cell. There are many reasons to use an SRAM or a DRAM in a system design. The design challenges includes density, speed, volatility, cost and other features. All of these factors should be considered before the selection of memory to a 2 system. This research work, concentrates on the design of read/write static random-access memories (SRAMs). Static Random Access Memory commonly known as SRAM is a type of RAM that holds data in static form but only as long as the power is supplied. An SRAM is typically made of two cross coupled inverters retaining either of the two stable states 0 and 1 and two access transistors to be used while reading and writing operations. To store one memory bit it requires six metal oxide semiconductor field effect transistors (MOSFET). An SRAM has three different states of operations. They are HOLD, READ and WRITE modes If the word line is kept low, the access transistor get disconnected from the bit lines. The two cross coupled inverters will continue to reinforce each other as long as they are connected to the supply. This is the operation in HOLD state. Whereas in READ and WRITE modes, the world line is given high such that there is an access between cross coupled inverters and bit lines. The read cycle is started by pre charging both the bit lines to high voltage. The word line WL which is asserted to high voltage will enable both the access transistors which causes one of the bit lines voltage to slightly drop due to the inverter storing 0 as data. A sense amplifier which senses the voltage levels will determine whether the stored data is 0 or 1. The write cycle begins by applying voltage value to be written into the bit lines. If we wish to write a 1 into the SRAM cell we have to set bit line bar to 0 and bit line to 1. WL is asserted a high voltage then and the value that is to be stored in the cell.

With the aggressive growth of semiconductor market, the usage of on-site static random access memory (SRAM) is also increasing. The key design parameters for SRAM, which needs to be improved, vary according to its applications. For example, Internet of Things (IoTs), body sensor nodes (BSNs), wearable electronics, and image processing applications demand robustness and energy efficiency1 ; while for recent artificial neural networks (ANNs) applications, graphics (GPU) processors, servers, and other high end applications, the energy is traded off to achieve high performance.2 Moreover, in case of wearable IoT applications (such as Google Glass, Fitbit, and Pebble), detecting and reacting to the mobile and ambient context (like speech, occupancy, and motion) from the wireless IoT sensor data has been the key enabler of research. All of these sensors capture and analyze the run time data by temporarily storing it into a memory, and thus, SRAM has been the repetitive architecture of this data storage and occupies the major portion of the system area.3 Therefore, the power consumed by SRAM plays the crucial role in overall power consumed by the system.

As the technology scales down in CMOS, issues like short channel effects, stability of data storage and leakage currents arise. Among the sources of leakage currents sub threshold is the major leakage component because of the low threshold voltage we use in nano-CMOS technology. The intensity of this leakage current is dependent on many factors such as supply voltage, temperature, dimensions and process parameters like (threshold voltage). Besides there are also other source of leakage currents like Gate oxide tunnelling leakage, Reverse-bias, Junction leakage, Gate induced drain leakage, Gate current due to hot-carrier injection.

II. EXISTING METHOD:

The use of cryptographic devices storing sensitive information has grown considerably during the last few decades and has become a crucial part of many applications, such as smart cards, and mobile devices. Side channel analysis (SCA) is a powerful threat to these devices because it exploits the information related to the physical behavior of these devices to extract sensitive data. PA attacks are considered to be one of the most powerful types of SCA methods since they require relatively simple equipment and setups. PA attacks exploit the correlation between the instantaneous current consumed by the power supply of the device and its processed and stored data, to extract secret data or sensitive information. Embedded memories dominate the area and power consumption of many VLSI system-on-chips (SoCs), and are key components of many cryptographic systems, such as smart cards and wireless networks employing cryptography algorithms, where they are used to store instruction code and data. Therefore, the analysis and design of secured memories is of utmost importance. Embedded memories are mostly implemented with the 6T SRAM macrocell, which provides high density, robust operation, and high performance. However, 6T SRAM arrays are traditionally designed and optimized for high density and performance, while their security properties are often overlooked, resulting in a high susceptibility to PA attacks. Previous works have proposed modified SRAM bitcells to reduce the correlation between the dynamic power dissipation and the stored data of a conventional 6T SRAM array [14], [15]. Both of these solutions are based on a two-stage write operation. During the first stage, the internal nodes of the SRAM cell (Q and QB) are pre-charged to a constant voltage to eliminate the correlation between the previously stored data, and the write operation that follows. In the authors suggested performing the pre-charge operation by using two additional PMOS transistors beyond the original 6T SRAM in order to power-cut the supply during the additional pre-charge phase. In the authors proposed a feedback-cut SRAM cell, composed of two additional NMOS devices which are used to cut off the feedback of the SRAM cell in order to avoid shortcircuit power dissipation. While these solutions effectively reduce the correlation between the power consumption and stored data of the SRAM array, they result in significant delay and power overheads, as well as reduced static noise margins (SNMs). In this paper, we describe a novel security-oriented 7T SRAM cell design, which incorporates a two-phased write operation, and significantly reduces the correlation between the written and stored data in the memory and its power dissipation, thus providing a PA resilient memory.

The proposed 7T cell includes an additional transistor to the original 6T SRAM implementation and a single power gate transistor per memory word, which are used to equalize the Q and QB voltages during the first phase of the write operation. Power analysis (PA) attacks have become a serious threat to security systems by enabling secret data extraction through the analysis of the current consumed by the power supply of the system. Embedded memories, often implemented with six-transistor (6T) static random access memory (SRAM) cells, serve as a key component in many of these systems. However, conventional SRAM cells are prone to side-channel power analysis attacks due to the correlation between their current characteristics and written data. To provide resiliency to these types of attacks, we propose a security-oriented 7T SRAM cell, which incorporates an additional transistor to the original 6T SRAM implementation and a two-phase write operation, which significantly reduces the correlation between the stored data and the power consumption during write operations.

To overcome the information leakage of the 6T SRAM cell during write operations, we propose a modified 7T SRAM cell employing a two-phase write operation consisting of an equalization and write phases, and resulting in a significantly lower correlation between its current dissipation and the stored data in the cell. The schematic representation of the proposed 7T SRAM cell is shown in Fig. 2. A power gate PMOS transistor (PG) is used to disable the voltage supply of an entire memory word (VVDD) to avoid short-circuit power dissipation during the equalization phase of the write operation. Transistor PPC is added to the original 6T SRAM implementation to short Q and QB during the equalization phase. A PC signal is used to disable PG and enable PPC to perform voltage equalization between Q and QB using charge-sharing, hence avoiding additional power consumption from the supply. During the second phase of the write operation, PC is discharged to charge VVDD and cut off PPC, and charged to enable the NMOS access transistors (NA1 and NA2) allowing them to pass the data from BL and BLB to Q and QB, respectively, to complete the write operation.

Fig. 2: 7T SRAM cell

III.PROPOSED METHOD

The rapid growth of portable battery operated devices has made low power IC design a priority in recent years. Embedded SRAM units have become an integral part in modern SoCs. Conventional SRAM cell designs are power hungry and poor performers in this new era of fast mobile computing. With continuous technology scaling, leakage currents dominate the total energy consumption of integrated circuits. Memory banks are primary producers of leakage currents in high performance microprocessors and systems-on-chips (SoCs). As increasing numbers of SRAM cells are crammed onto integrated circuits to meet the aggressive performance requirements, the leakage power consumed by memory arrays increases with each technology generation. Data stability is another important concern associated with SRAM cells. With reduced supply voltage, smaller devices, and exacerbated process

variations, maintaining data stability has become a primary challenge in SRAM design. New memory circuits with lower leakage and higher data stability characteristics are therefore highly desirable.

Memories are an integral part of most of the digital devices and hence reducing power consumption of memories as well as area reduction is very important as of today to improve system performance, efficiency and reliability. Most of the embedded and portable devices use SRAM cells because of their ease of use as well as low standby leakage.

The proposed novel SRAM cell contains two inverters of cross-coupled connection. The proposed 7T SRAM consists of two pull-up transistor and two pull-down transistors and two PMOS pass transistors and an NMOS footer transistor. Since the leakage current of NMOS is larger than that of PMOS with the same feature size. To further reduce the leakage power consumption, instead of using NMOS, the pass transistors of SRAM cells are replaced by PMOSs, and also the footer nmos transistor is used to reduce the leakage path from supply to ground. Since in lower technologies, leakage power is the major concern, to reduce the leakage power.we also used an transistor with sl as its input.

Operation in SRam:

Read operation:

To perform read operation, initially memory should have some value. Therefore let us consider memory has Q=1 and Q'=0. Raise the word line to high, to perform the read operation. bit and bit_b acts as output lines, and these bit lines are initially pre-charged i.e. there will be a node voltage Vdd at bit and bit_b. As Q and bit are high, there will be no discharge in the circuit. As Q' is 0, there will be a voltage difference between the Q' and the node voltage at bit_b, hence bit_b voltage decreases. Therefore there will be discharge in the circuit and current flows. Bit and bit_b are connected to the sense amplifier, this sense amplifier acts as a comparator, so When bit' is low the output will be 1. Hence input Q=1 and we got the output as 1, read operation verified. In the same way consider Q=0 and Q'=1 in the memory. There will be a discharge in the circuit at Q and bit, since there is voltage difference. The transistors must have ratio such that Q lies below the threshold region of P2/D2. This is called read constraint. As bit voltage decreases the output will be 0.when input Q=0, the output we get is 0. Therefore in both the cases read operation is verified.

Write operation:

Consider the memory bits consists of Q=0 and Q'=1. Initially word line is high and hence write operation can be performed. In the write operation bit and bit' are input lines. As we have control on the bit lines, initially make the bit_b connected to ground so that we can have the voltage difference between Q' and bit_b. To write 1 into the SRAM cell, D2 must be stronger than P2,this can be achieved by changing the aspect ratio of the transistors. Hence Q will be 1. Initially Q=0 after the operation Q=1, hence we write successfully into the memory.

Hold Operation:

In retention mode, wordline is turned off which will make two pass gates to become off. Then a feedback loop is formed by the cross coupled inverters hence data will be hold if the power supply is ON.

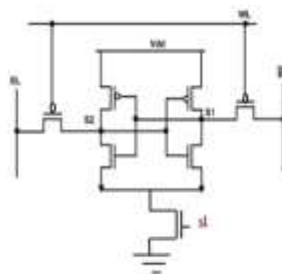

Fig. 4 Proposed SRAM

IV.RESULTS:

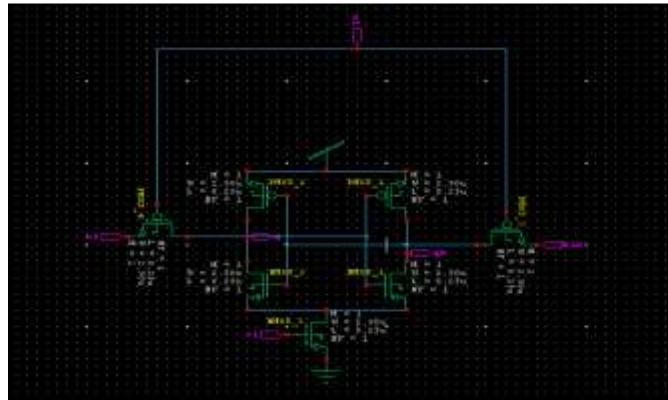

Fig. 5: Schematic of Proposed SRAM

Write-1 operation: In the write operation mode in the SRAM Cell the bit line BL is used to write the data. To perform the write operation BLB and WL line are used. In the operation when we write "1" in the cell the BL is charged to VDD and M5 enable the WL signal and then the "Q" node start charging and turns to M4 leads to flip "QB" node to logic „0". Then 'QB' node helps enabling the M1 for writing logic" 1 ' at 'Q' node.

Write-0 operation: If data need to be written is '0', write bit-line should be at logic low, and M5 turns on, by enabling WL signal. Then the node "Q" starts discharging and turns on M3 which in turn flips 'QB' node to logic '1'. After that 'QB' helps turning M2 on, which facilitates discharging 'Q' node properly, and consequently logic '0' is obtained at 'Q' node.

Read 0 or 1 operation: In Read operation the SRAM data is read from the cell. At the initial stage the data in the bit line is begun pre-charging to VDD. After pre-charging the bit line the read signal is activated. It depends on whether the data in RBL holds or discharged is decided by SRAM cell. After pulling the read line to VDD RBL is discharged, then it going to indicate the SRAM cell store "0" in it. If it hold the charge then it store "1". Then read operation WL is inactive at logic "0".

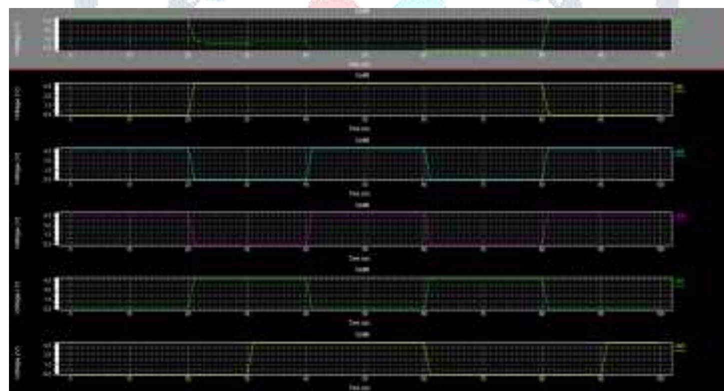

Fig.6:Waveform of Proposed SRAM

Area report:

Fig.7:Area of Proposed SRAM

Delay report:

The static noise margin is decreasing with the decrease in the technology nodes. The side of the square of maximum size embedded in the butterfly curve gives the Static Noise Margin. SRAM is susceptible to lose its characteristics of read stability and write stability on further decrement in technology nodes. Though 7T SRAM can perform better than 6T at low VDD it has limiting factors:

1. The above picture shows the comparison is made till VDD = 0.72v and VSS= 0.36v-: These are the maximum low voltages that this 7T SRAM can perform according To the transistor sizing. If we operate 7T SRAM lower than the stipulated voltage Levels then the write operation cannot be performed, since the write margin Decreases with decreasing VDD.

2. Read operation at low-VDD-: Levels result in storage data destruction in SRAM cells this is due to the leakage current of PMOS transistor P2. This is shown in Figures as the 6T SRAM cell is operated at low VDD.

Fig.8: Delay of Proposed SRAM

Power report:

The power consumption by the particular source is computed by multiplying the average current drawn from the source and voltage provided by the source.A power supply voltage of 0.9 V is used for the simulation in accordance with the ITRS roadmap for 32 nm technology. Since the static power is directly proportional to the threshold voltage in an exponential manner so any increase in the diameter variation causes increase in the static power consumption. The Proposed **7T SRAM** cell **consumes** 22.03% less **power** for write `0' operation, 17.33% less **power** for write `1' operation, 17.52% less **power** for read `0' operation **and** 21.36% less **power** for read `1' operation compared to conventional **6T SRAM** cell.

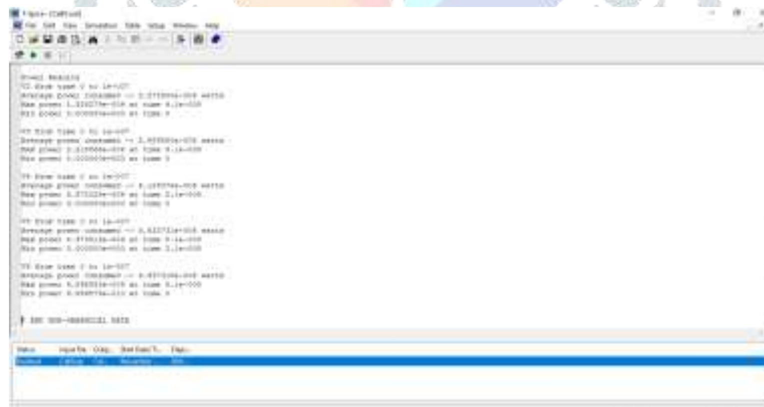

Fig.9: Power of Proposed SRAM

V.Conclusion:

In this paper, a 7T SRAM structure was presented. The proposed SRAM uses a footer nmos switch with input sl to reduce the static circuit power dissipation. The proposed sram cell is designed using 90nm technology in tanner tool. Our simulation results show that the energy dissipation of the proposed circuit is improved over that of existing method.

VI. Future scope:

The future research activities may include integration of the proposed DFF in complex digital systems, combining sequential and combinatorial logic. The future research activities may include integration of the proposed DFF in complex digital systems, combining sequential and combinatorial logic. The future research activities may include integration of the proposed DFF in complex digital systems, combining sequential and combinatorial logic. In the future, we can integrate this proposed SRAM in different applications like EMBEDED SYSTEMS, CPU which are power hungry to reduce the power consumption. Also when integrate this sram cell into an array, the overall power consumption of the array will be decreased which is very useful for all portable applications. The future research activities may include integration of the proposed DFF in complex digital systems, combining sequential and combinatorial logic.

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