A Verilog Implementation and Performance Analysis of Polar Encoder and Decoder for Next Generation Communication Application

Rahul Parmar[1], Dr. Anshuj Jain[2]

M.Tech Scholar, Dept. of ECE., SCOPE College of Engineering, Bhopal, India[1]

Associate Professor & HOD, Dept. of ECE., SCOPE College of Engineering, Bhopal, India[2]

Abstract: Polar codes investigated and achieve improved performance in 5G communication scenario in research laboratories. Especially, the original design of the polar codes achieves capacity when block sizes are asymptotically large with successive cancellation decoder. Polar codes become a new channel coding, which will be common to apply for 5th generation wireless communication systems. There are many aspects that polar codes should investigate further before considering for industry applications. The original design of the polar codes achieves capacity when block sizes are asymptotically large with successive cancellation decoder. So there is a need of high speed, less area and low power encoding scheme for next generation communication. In this paper, design and performance analysis of polar encoder and decoder are presented. Xilinx ISE 14.7 software is used to implement and simulate the polar encoder and decoder. The Simulation results show that the proposed polar code can achieve higher performance.

IndexTerms **– Speed, Area, Power, Polar, 5G, Encoding, Decoding, Channel.**

I. INTRODUCTION

There are numerous perspectives that polar codes ought to investigate further before considering for industry applications. Particularly, the original structure of the polar codes accomplishes limit when square sizes are asymptotically enormous with successive cancellation decoder. Be that as it may, in square sizes that industry applications are working, the performance of the successive cancellation is poor contrasted with the very much characterized and executed coding plans, for example, LDPC and Turbo. Polar performance can be improved with successive cancellation list decoding, be that as it may, their convenience in genuine applications still faulty because of poor execution efficiencies.

Despite the fact that the completely equal polar code based encoder engineering forms the bits in a completely equal manner however endures with gigantic equipment multifaceted nature with expanding code length. As completely equal polar code based engineering will cause rationale multifaceted nature issue, while fractional equal polar code based design is restricted by memory units of high-throughput applications.

The numerical establishments of polar codes lay on the polarization impact [1] of the network G2 = [1 0]. In a (N, K) polar code of length N = 2n, the polarization impact builds up N virtual channels, and through each channel a solitary piece is transmitted. Every one of these bit-channels, or sub channels, has an alternate unwavering quality; message bits are allocated to the K most dependable channels. The polar code is henceforth characterized by the transformation lattice GN = G2⊗n, for example as the n[th] intensity of the polarizing network, and either the solidified set F of size N − K, or its reciprocal information set I = FC of size K, where I and F are subsets of the record set 0, 1, ..., 2n−1 . A codeword d = d0, d1, . . . , dN−1 is determined as

d = uGN (1)

where the info vector u = u0, u1, . . . , uN−1 is produced by appointing ui = 0 in the event that I , and storing information in the rest of the components. Each file I recognizes an alternate bit- channel.

A. LDPC Code

The throughput of layered BP decoder can be calculated as:

$$Throughput_{[Mbps]} = \frac{L \cdot f_{c[MHz]}}{I \cdot N_{Layer} \cdot \left(\left\lceil \frac{z}{P} \right\rceil + T_{pip} - 1 \right)}$$

where,

I denotes the number of iteration;

P denotes the parallelism level;

L denotes the length of code block without CRC;

N_{Layer} denotes the decoding layer, equals the number of rows for base matrix;

z denotes the expending factor;

T_{pip} denotes the processing clocks for CNU and VNU updating plus memory reading and writing at each decoding step;

f_c denotes the operating frequency.And, the throughput of flooding decoder with single-frame can be calculated as:

$$Throughput_{[Mbps]} = \frac{L \cdot f_{c[MHz]}}{I \cdot (N_{Layer} + T_{pip} - 1)}$$

B. Turbo Code

The throughput of turbo MAP decoder can be calculated as:

$$Throughput_{[Mbps]} = \frac{L \cdot f_{c[MHz]}}{2 \cdot I \cdot \left(\left\lceil \frac{L}{P} \right\rceil + \frac{2}{a} \cdot W \right)}$$

where,

I denotes the number of iteration;

P denotes the parallelism level;

L denotes the length of code block without CRC;

W denotes the number of extra trellis for MAP decoder;

a denotes the number of bits processed in one MAP core per clock cycle, i.e. 1 for Radix-2 and 2 for Radix-4.

f_c denotes the operating frequency.

II. BACKGROUND

P. Chen et al., [1] proposed hash-polar codes have comparable casing error rate performance to cyclic redundancy check (CRC)-polar codes and perform better than parity check polar codes. So as to support early end (ET) for 5G coding, we at that point propose divided hash-polar codes, which display the upsides of the ET gain contrasted and both CRC-polar codes and dispersed CRC-polar codes.

S. Shao et al., [2] show that the general usage intricacy of turbo, LDPC and polar decoders relies upon various different factors past their computational unpredictability. More explicitly, we think about the throughput, error correction capacity, adaptability, territory productivity and vitality proficiency of ASIC usage drawn from 110 papers and utilize the outcomes for describing the points of interest and burdens of these three codes just as for dodging traps and for giving structure rules.

H. Mu et al.,[3] show that critical improvement in error performance is accomplished by the proposed polar-coded SCMA in added substance white Gaussian commotion (AWGN) channels, where the performance of the traditional SISO conviction spread (BP) polar decoder supported SCMA, the turbo coded SCMA and the low-density parity-check (LDPC) coded SCMA are utilized as benchmarks.

R. Shrestha et al., [4] decoder conveys a throughput of 298r Mbps which is 16% superior to the best in class execution. It has accomplished better throughput effectiveness of 1.01r contrasted with as of late reported works have combined and post-format reproduced our plan in UMC 180 nm-CMOS procedure and it possesses a zone of 6.1 mm².

P. Chen et al., [5] show that the hash-linked polar codes can accomplish both the lower bogus alert rate and preferable error-correcting performance over traditional CRC-supported polar codes in both the AWGN and high versatility channels. Furthermore, with the joint decoding approach, hash-based CRC-supported polar codes perform better than LTE turbo codes for high-order regulations as far as the casing error rate over the HST channel.

S. Yadav et al., [6] presents the enhancement of throughput and bit-error performance by transmitting extra information bits in each subcarrier block as well as to decrease the complexity of the detector. In this paper, soft trellis decoding algorithm is implemented with channel estimation using Neuro-LS technique. The result analysis shows the better performance of trellis decoder with respect to BER and Neuro-LS channel estimation with respect to BER.

X. Shih et al.,[7] Polar Codes applied for cutting edge MIMO frameworks is a developing exploration subject. In this work, we propose a productive VLSI equipment engineering of the Polar encoder utilizing radix-k preparing motors. Under TSMC 90nm CMOS innovation, the 16384-point radix-2 based Polar encoder configuration is blended with 0.244mm2 under most extreme clock frequency of 2.0GHz. In the comparative way, the VLSI equipment can be stretched out to radix-k based structure. In the chip usage with APR results, the radix-2 based Polar encoder just possesses 0.305mm2 and disseminates 357.8mW with greatest clock frequency of 1.61GHz, conveying all out throughput of 1.61Gbps.

X. Shih, P. Huang et al.,[8] Polar encoder chip (LB-R2-PE) is structured and incorporated with all out region of 0.244mm2 and force dispersal of 366.6mW, working at most extreme frequency of 2.0GHz. In the APR chip execution perspective, the 16384-point LB-R2-PE chip just involves 0.305mm2 and expends 357.8mW with most extreme working frequency of 1.61GHz, conveying all out throughput of 1.61Gbps.

S. M. Abbas et al.,[9] presents LDPC with Polar codes is one well known way to deal with upgrade the performance of BPD, where a short LDPC code is utilized as an external code and Polar code is utilized as an internal code. In this work we propose another approach to develop connected LDPC-Polar code, which not just outperforms ordinary BPD and existing linked LDPC-Polar code yet in addition shows a performance improvement of 0.5 dB at higher SNR system when contrasted and SCD.

A. Arpure et al.,[10] Despite the fact that the completely equal polar code based encoder engineering forms the bits in a completely equal manner yet endures with tremendous equipment unpredictability with expanding code length. As completely equal polar code based design will cause rationale multifaceted nature issue, while incomplete equal polar code based engineering is constrained by memory units of high-throughput applications. In this work effective polar code based encoder engineering is structured and executed on a FPGA utilizing Vertex 5 for the polar encoding plan. Here we break down the encoding procedure of polar code based encoder design and propose another engineering that is reasonable for encoding long polar codes with less equipment intricacy.

III. PROPOSED WORK

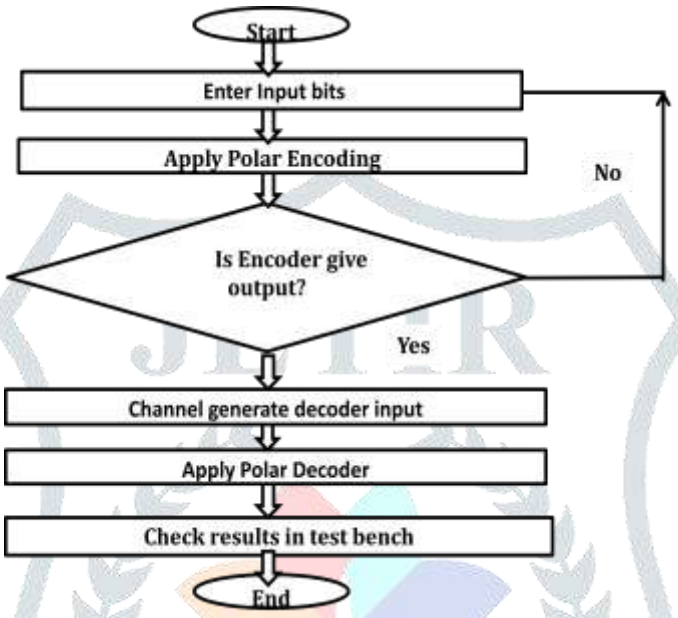

Figure 1: Flow Chart

Algorithm-

- input [15:0]enc_in;
- output [15:0]dec_out;
- wire [31:0]enc_out,channel_in;
- wire[287:0]channel_out,dec_in;
- assign channel_in = enc_out;
- assign dec_in = channel_out;
- encoder_32bit t1(enc_in,enc_out);
- channel t2(channel_in,channel_out);
- decoder_32bit t3(dec_in,dec_out);

Proposed Polar codes are a channel coding innovation and all channels coding innovation works essentially in a very comparative manner. Correspondence joins are defenseless to errors because of random commotion, impedance, gadget weaknesses, and so on that corrupt the original information stream at the less than desirable end. Channel coding essentially utilizes a lot of algorithmic procedure on the original information stream at the transmitter, and another arrangement of procedure on the got information stream at the collector to correct these errors. In channel coding wording, the totally of these activities at the transmitter and beneficiary are individually indicated as encoding and decoding tasks. Channel coding techniques extensively fall under two classes: square codes and convolutional codes. Square codes work on a square of information/bits with fixed estimate and apply the control to this square at the transmitter and collector. Reed-Solomon codes, ordinarily utilized on the hard circles of PCs, are one case of this kind of code. Convolutional codes, then again, work on floods of information with more discretionary quantities of information/bits. These codes apply a sliding window strategy that gives a significant decoding advantage. Basic Viterbi codes are a case of this kind of code.

As you would speculate, significant beneficial exploration has been done throughout the years into the connection of square and convolutional codes to consolidate the advantages of both. For instance, the RSV code, which was the best performing code until turbo codes, was a half and half of the Reed-Solomon code, which is a square code, with a Viterbi convolutional code.

Polar codes encoding ready to encode the polar codes with the assistance of a straightforward organizing strategy. The space unpredictability of the encoder is equivalent to O(N) and the time multifaceted nature is O(Nlog(N)). The generator network G can be characterized by GN = BNF ⊗n where n = log(N), BN is known as the bit-inversion framework and F⊗n is the

Kronecker item where F = [1 0 1] as it is referenced already. Beforehand structure a 8-piece polar encoding. On the off chance that we have polar code with blocklength N, it comprises of an information vector u1 N for example u1 8 = [0 0 1 0 1 0 1] and the vector at the yield is x1 N for example x1 8 = [1 1 0 1 1]. Moving between the information vector and the yield vector u1 N → x1 N is straight over Galois Field (GF(2)).

Polar codes break the wheel to some degree in the field of channel coding with an unorthodox methodology that looks like a portion of the tasks more ordinarily found in the standard correspondence chains between the baseband and radio front finishes.

Perhaps the greatest shock in 5G standardization so far has been the acknowledgment of polar codes as an official channel coding innovation. Such choices are obviously mind boggling ones that are frequently as much about political influence as innovation goodness. In any case, the reality accomplished by this generally early innovation is astounding. It was just a short time back that the prevalent view was that turbo codes could never be obscured.

Polar codes break the wheel to some degree in the field of channel coding. Polar codes work on squares of images/bits and are therefore actually individuals from the square code family. The development of these codes follow an unorthodox methodology contrasted with more customary methodologies like turbo codes. From multiple points of view, the strategies take after a portion of the activities that are generally utilized in standard correspondence chains between the baseband and radio finishes, basically the group of Quick Fourier Transform (FFT) like methods that anyone with an interchanges or sign handling foundation will be much acquainted.

IV. SIMULATION RESULT

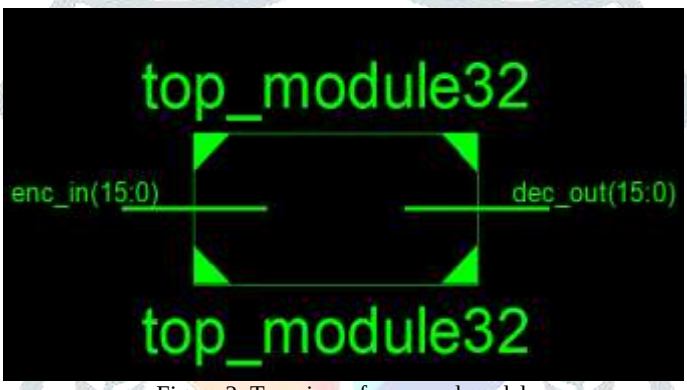

Figure 2: Top view of proposed model

In figure 2, showing top level of proposed polar code model. Here apply 16 bit input and after complete process it gives 16 bit output.

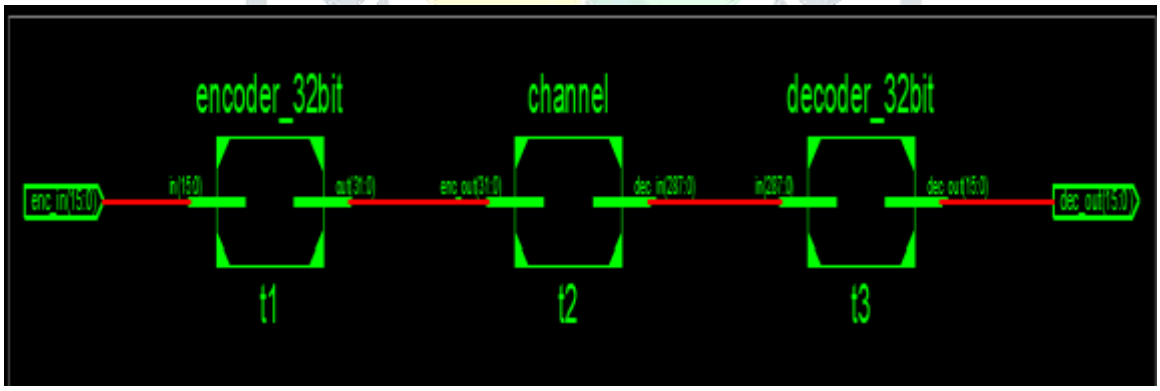

Figure 3: Complete process of proposed model

Figure 3 presenting complete process block diagram in form of RTL view. Here it is clear that all process divide in three steps. The details of all process is explain step via step in below diagrams.

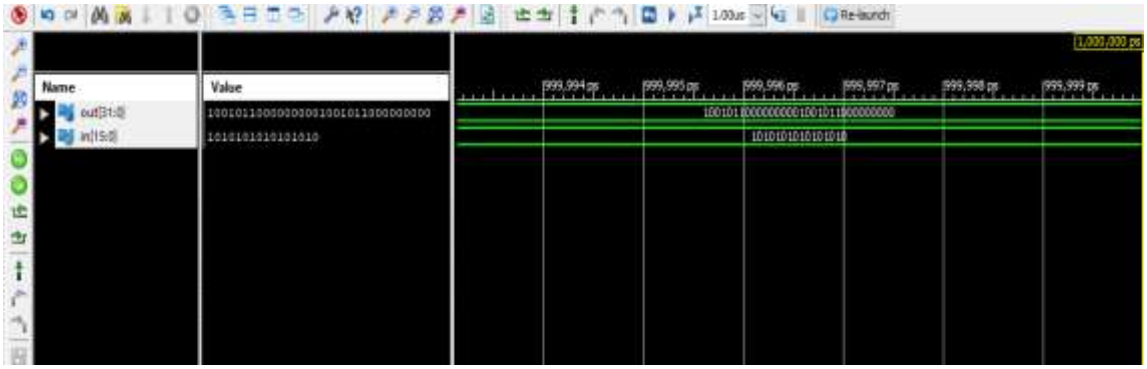

Figure 4: Test bench result at encoder

Figure 4 showing result in test bench, here apply 16 bit input that is 1010101010101010. After encoding it generate 10010110000000001001011000000000.

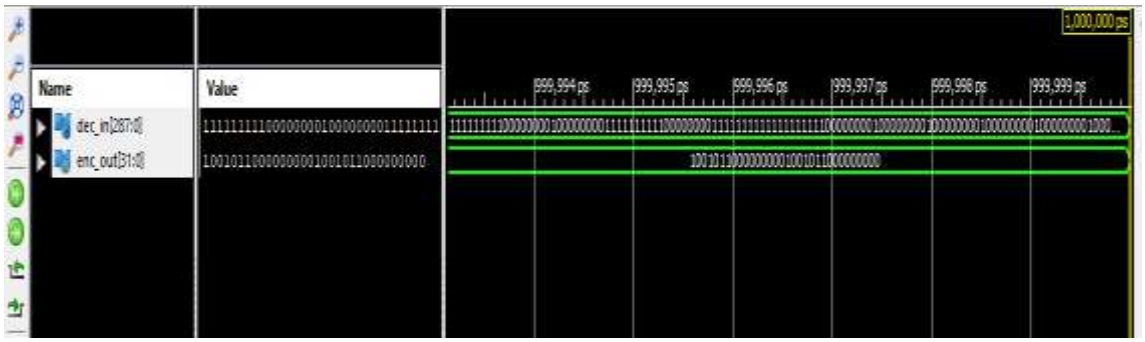

Figure 5: Result at channel

Figure 5 showing channel result in test bench, here apply 32 bit encoder output that is 10010110000000001001011000000000. It generates 288 decoder input bit that is hff80403ff00ffffe0100804020100804020 1ff80403ff00ffffe0100804020100804020 1 in hexadecimal.

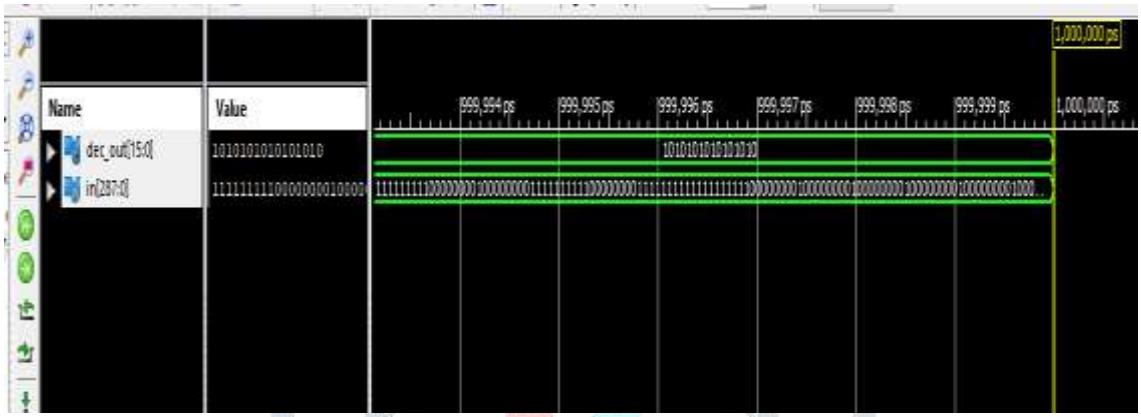

Figure 6: Result at decoder

In figure 6 showing decoder stage of proposed model in test bench, here apply 288 decoder input bit that is hff80403ff00ffffe0100804020100804020 1ff80403ff00ffffe0100804020100804020 1 and it generate 16 bit output 1010101010101010.On the other hand, we recover original data.

Table 1: Simulation Parameter and Comparison with previous work

Sr No.	Parameter	Previous Work	Proposed Work
1	Method	Polar decoder	Polar encoder and polar decoder
2	Area	5.35 mm^2	2.33 mm^2
3	Delay	1534ns	139.612ns
4	Power	1072.9 mW	43mW
5	Time	NA	30.48 secs
6	PDP	164153	6003

Table 1 showing comparison of proposed work with previous work, so it can be seen that proposed work gives better result than existing work.

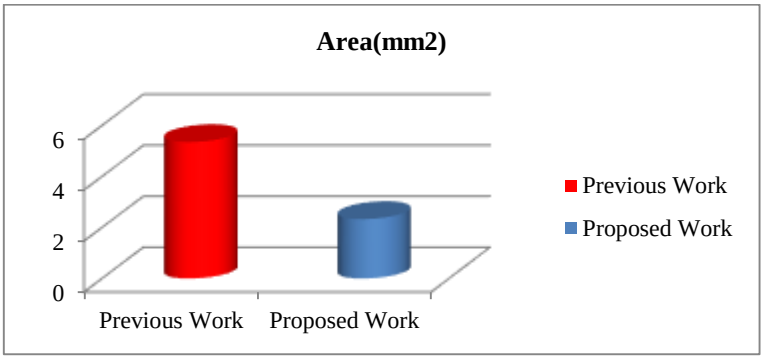

Figure 7: Comparison of Area

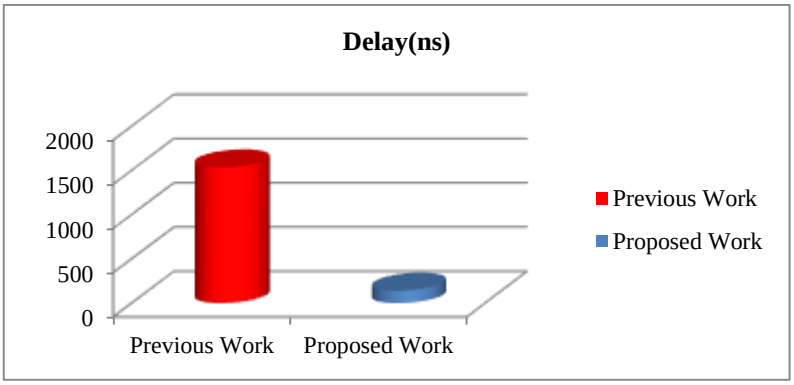

Figure 8: Comparison of delay

From Figure 7 and 8, it is clear that proposed polar encoder and decoder gives significant performance improvement. Although 5G communication and application is still in testing phase and this research provide encoding and decoding scheme under proposed constraints.

V. CONCLUSION

In this work audited the best in class in polar code in encoding and decoding form. It was indicated that the many decoding algorithms were created and executed to address different application necessities. Additionally contrast polar code and CRC code. Numerous specialists suggest that polar code can be utilized ahead of time remote correspondence for people to come.

In this work, we have point by point the polar code encoding process inside the fifth era remote frameworks standard, giving the peruse an easy to use depiction to understand, actualize and mimic 5G-consistent polar code encoding. This encoding chain exhibits the effective efforts of the 3GPP standardization body to meet the different necessities on the code for the eMBB control channel: low depiction intricacy and low encoding multifaceted nature, while covering a wide scope of code lengths and code rates.

REFERENCES

1. P. Chen, B. Bai, Z. Ren, J. Wang and S. Sun, "Hash-Polar Codes With Application to 5G," in *IEEE Access*, vol. 7, pp. 12441-12455, 2019.
2. S. Shao *et al*., "Survey of Turbo, LDPC and Polar Decoder ASIC Implementations," in *IEEE Communications Surveys & Tutorials*.
3. H. Mu, Y. Tang, L. Li, Z. Ma, P. Fan and W. Xu, "Polar coded iterative multiuser detection for sparse code multiple access system," in *China Communications*, vol. 15, no. 11, pp. 51-61, Nov. 2018.
4. R. Shrestha and A. Sahoo, "High-Speed and Hardware-Efficient Successive Cancellation Polar-Decoder," in *IEEE Transactions on Circuits and Systems II: Express Briefs*.
5. P. Chen, M. Xu, B. Bai and J. Wang, "Design and Performance of Polar Codes for 5G Communication under High Mobility Scenarios," *2017 IEEE 85th Vehicular Technology Conference (VTC Spring)*, Sydney, NSW, 2017, pp. 1-5.
6. S. Yadav, A. Nema, and J. Mishra, "Space Time Trellis Code Frequency Index Modulation with Neuro-LS Channel Estimation in OFDM", IJOSCIENCE, vol. 5, no. 9, pp. 21-27, Sep. 2019. https://doi.org/10.24113/ijoscience.v5i9.226
7. Y. N. Li, "Robust Image Hash Function Based on Polar Harmonic Transforms and Feature Selection," *2012 Eighth International Conference on Computational Intelligence and Security*, Guangzhou, 2012, pp. 420-424.
8. X. Shih, P. Huang and Y. Chen, "High-speed low-area-cost VLSI design of polar codes encoder architecture using radix-k processing engines," *2016 IEEE 5th Global Conference on Consumer Electronics*, Kyoto, 2016, pp. 1-2.
9. X. Shih, P. Huang and Y. Chen, "LEGO-based VLSI design and implementation of polar codes encoder architecture with radix-2 processing engines," *2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Jeju, 2016, pp. 577-580.
10. S. M. Abbas, Y. Fan, J. Chen and C. Tsui, "Concatenated LDPC-polar codes decoding through belief propagation," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, 2017, pp. 1-4.
11. A. Arpure and S. Gugulothu, "FPGA implementation of polar code based encoder architecture," *2016 International Conference on Communication and Signal Processing (ICCSP)*, Melmaruvathur, 2016, pp. 0691-0695.
12. B. Chen, T. Ignatenko, F. M. J. Willems, R. Maes, E. van der Sluis and G. Selimis, "A Robust SRAM-PUF Key Generation Scheme Based on Polar Codes," *GLOBECOM 2017 - 2017 IEEE Global Communications Conference*, Singapore, 2017, pp. 1-6.
13. D. Chen, N. Zhang, N. Cheng, K. Zhang, Z. Qin and X. S. Shen, "Physical Layer based Message Authentication with Secure Channel Codes," in *IEEE Transactions on Dependable and Secure Computing*.
14. D. Chen, N. Cheng, N. Zhang, K. Zhang, Z. Qin and X. Shen, "Multi-message Authentication over Noisy Channel with Polar Codes," *2017 IEEE 14th International Conference on Mobile Ad Hoc and Sensor Systems (MASS)*, Orlando, FL, 2017, pp. 46-54.
15. R. Shrestha and A. Sahoo, "High-Speed and Hardware-Efficient Successive Cancellation Polar-Decoder," in *IEEE Transactions on Circuits and Systems II: Express Briefs*.