Power Efficient CMOS DRPTL Adder Topologies

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***Abstract*—With the revolution in integrated circuits, great emphasis was given on performance and miniaturization. Speed, area and power became the main criterion upon which a VLSI system is measured in terms of its efficiency. For high performances of the execution cores in the logic and arithmetic logic unit the efficiency of energy is essential. For highest power density of the processor block is a part of the adder. It creates a thermal hot spots and sharp temperature gradients to operate the system with the circuit which have high performance. The multiple ALUs presence in modern superscalar processors and execution cores of chip further associate with aggravates the problem by impacting circuit reliability. It increases the cooling costs for the purposes of design. Basically the adder circuit is designed to achieve low power and less delay and by logic gate of the circuit improves the performances. For speed process high logic circuit is implemented and also to have less propagation. In hybrid CMOS design style various adder cells and transistor is used, but in proposed circuit Dual Rail Signal System (DRPTL) is implemented with the load condition and the clock signal to manage the power flow in the circuit and the process is performed in an efficient way in terms of its gate count and thereby on power and speed.**

Index Terms*— *Single Rail Signal system, Dual Rail Signal System, Ripple Carry Adder

I. INTRODUCTION

Digital computer arithmetic is an aspect of logic design with the objective of developing appropriate algorithms in order to achieve an efficient utilization of the available hardware. Given that the hardware can only perform a relatively simple and primitive set of Boolean operations, arithmetic operations are based on a hierarchy of operations that are built upon the simple ones. Since ultimately, speed, power and chip area are the most often used measures of the efficiency of an algorithm, there is a strong link between the algorithms and technology used for its implementation.

In VLSI design methodologies power minimization is one of the primary concerns because a long battery life is required for mobiles and portable devices, Power dissipation is increasing due increasing rate of transistors on a single chip. Adder is one of the most critical components of a processor, as it is used in the arithmetic logic unit, in the floating point unit, and for address generation in case of cache or memory access [7]. Increasing demand for mobile electronic devices such as cellular phones PDA's and laptop computers require the use of power efficient VLSI circuits. The total Power dissipation in a CMOS circuit is given as:

Ptotal= Pswitching + Pstatic + Pshortcircuit ----------(1)

Taking into consideration the Static Power dissipation, let us consider a simple CMOS inverter. In ideal cases, when input to the gate terminal is 0, the NMOS is off and PMOS is on and vice versa. So at all times, only one MOS is on and other off. So ideally no leakage current in this operation. But there can be leakage current during this operation, which is a leakage between diffusion region and substrate region of MOS, as per the parasitic diode model. So this leakage current constitutes the static power dissipation and is given by:

*PStatic = VDD * ILeakage ----------(2)*

The Dynamic power dissipation occurs during switching. While switching either from 1 to 0 or from 0 to 1, for a short duration, both NMOS and PMOS are on. At that time a small short circuit current(ISC) flows from VDD to Ground and the dynamic power dissipation occurs.

*PShortCircuit = VDD*ISC ----------(3)*

$$P_{switching} = \sum_{i=0}^{N} \alpha_i C_i V_{DD} V_{swing} f_{clk} - - - - - (4)$$

Where α_i is the switching activity at node.

Propagation delay is how quickly the circuit responds to the change in input and is given by:

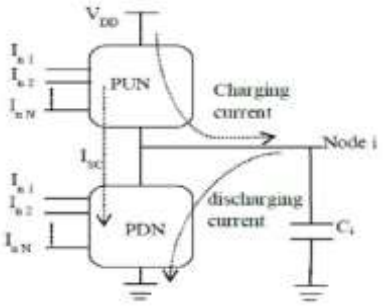

Fig 1.1: Switching And Short-Circuit Current Elements In Static CMOS

$$T_d \alpha \frac{C_L V_{DD}}{K(V_{DD} - V_{TH})^{\alpha}} \text{ - - - - - - - - - - - - - (5)}$$

Where α refer the velocity index saturation.

In well-engineered deep submicron CMOS technologies, the difficult criteria are concentrating on emerging communication process high speed with low power in digital signal processing chip. In the process of arithmetic division, the multipliers and adder are used widely in VLSI system. Since last decades, the growth of the application in electronics is high and it's major in semiconductor industry. However, reduction of power consumption, delay and area are the critical fear in the logic circuits of any application. The explosive growth and the demands are high in convenient electronic product, high speed, battery life's, area and the reliabilities of the circuits. In various logic circuits and algorithm like parity checker, converter of code, compressors and error correcting code or detector are basically used the building blocks of XOR-XNOR circuit.

There are three types of power consumption in VLSI circuits namely short circuit power, static power and dynamic power. The short circuit power dissipation is due to the short circuit current generated when both NMOS and PMOS transistors are simultaneously active for a small duration. The static power dissipation varies with process technology. The dominant dynamic power due to charging and discharging of load capacitance is given by the following equation (1),

Dynamic Power = α (VDD) 2 f CL ----------(6)

Where, α denotes the activities of switching, voltage supply as VDD and frequency of switching the load capacitance. Lower the voltage is, the smaller the power co0nsumption. However, using a lower VDD increases the delay. The alternate way of decreasing the power is by reducing the number of switching transistors. The power consumption of a CMOS digital circuit can be represented as

P= fCVdd²+fIshortVdd+IleakVdd----------(2)

II. RELATED WORK

For high performances of the execution cores in the logic and arithmetic logic unit the efficiency of energy is essential. For highest power density of the processor block is a part of the adder. It creates a thermal hot spots and sharp temperature gradients to operate the system with the circuit which have high performance. The multiple ALUs presence in modern superscalar processors and execution cores of chip further associate with aggravates the problem by impacting circuit reliability. [1] It increases the cooling costs for the purposes of design.

At the same time, it critical the performances of the wide adders under different regions and appear of ALUs inside and microprocessor data path of FPUs. Ripple Carry Adder have cascaded "N" single bit full adder and output carry of previous adder as input to next full adder carry. The value of N increases the adder delay in a linear way. Therefore, the adder has a lowest speed of RCA with large propagation delay but least are only occupies in it. BEC uses less logic gates than the structure of N-bit full adder.

In real time application, adder circuit is a major part in various logic circuits. Normally, the circuit design is design for consumption of low power to enhance the performance and to address the parameter at chip level. The design of the circuit provides an efficient power delay product (PDP), less propagation delay and low power and area. Therefore, for various design style of logic circuit is built with required performances. When compare the conventional static CMOS logic styles Adder like TGA, TFA, etc the hybrid CMOS design provides a better performance. It achieves a good drivability, delay, power, PDP, energy and noise robustness than the existing circuit.

The essential components are used to design the sophisticated hardware circuits and multiplexer is performed based the topology of pass transistor full adder with less area and transistor count. [8] As well as the CMOS adder circuit is designed based on Tanner EDA using T-SPICE and define the design of the gate 3T-XOR with its significant process. The performances of the arithmetic and logic circuit of adder are illustrated the system performances as per the gate function. In digital systems, if adder lies on the critical path, then the delay of the overall system will increase. In circuit implementation the function of sum and carry is carried out by Pass transistor logic and Gate

Diffusion Technique (GDI) respectively. [2] Both functions separate the count of transistor equally.

III. PROPOSED METHOD

The dual rail pass transistor logic improves the dynamic circuit speed with the evaluation of clock signal logic with transistor. The supply of voltage is varied based on the charges phases. If the clock signal is equal to 1 in the evaluation phase, then the circuit will be discharged or pre-charge and if equal to 0 in pre-charge phase, then the circuit is charged and applies to voltage supply level from the transistor. The proposed work is the Complementary Pass Transistor logic as an alternative to reduce static power dissipation and avoids threshold voltage loss.

3.1 PASS TRANSISTOR LOGIC

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages.[9] This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage.

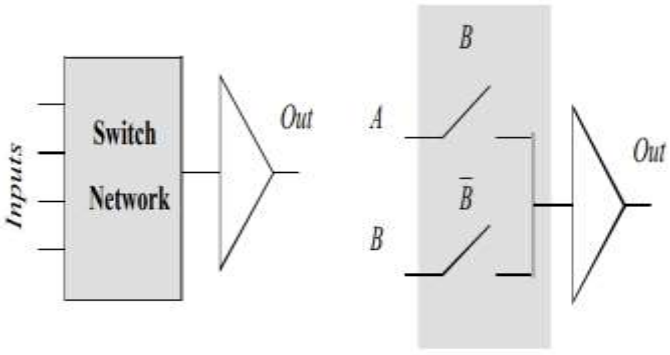

Fig 3.1: Pass Transistor Logic

- N transistors
- No static consumption

Each transistor in series is less saturated at its output than at its input. [10] If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so that output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Simulation of circuits do not decrease. Simulation of circuits may be required to ensure adequate performance.

Primary inputs drive the gate terminals + source-drain terminals. In contrast to static CMOS – primary inputs drive gate terminals.

3.1.1 PASS TRANSISTOR AND GATE

When B is "1", top device turns on and copies the input A to output F. When B is low, bottom device turns on and passes a "0". The presence of the switch driven by B is essential to ensure that the gate is static – a low-impedance path must exist to supply rails. Adv.: Fewer devices to implement some functions. Example: AND2 requires 4 devices (including inverter to invert B) vs. 6 for complementary CMOS (lower total capacitance). NMOS is effective at passing a 0, but poor at pulling a node to Vdd. When the pass transistor a node high, the output only charges up to Vdd-Vtn. This becomes worse due to the body effect. The node will be charged up to Vdd – Vtn (Vs)

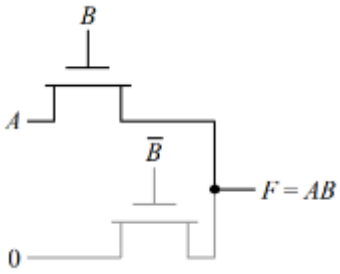

Fig 3.2 AND Gate with pass transistor

3.2 COMPLEMENTARY PASS TRANSISTOR LOGIC

Complementary pass transistor logic. Other authors use the term "complementary pass transistor logic" (CPL) to indicate a style of implementing logic gates where each gate consists of a NMOS-only pass transistor network, followed by a CMOS output inverter.

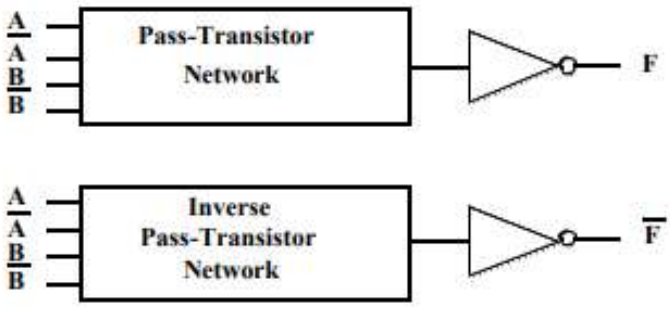

Fig 3.3 Complementary pass logic transistors

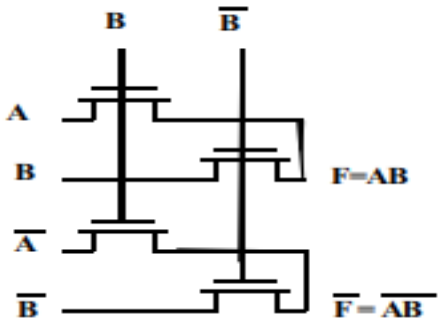

Fig 3.4 AND Gate and NAND Gate With Pass transistors

Since circuit is differential, complimentary inputs and outputs are available. Although generating differential signals require extra circuitry, complex gates such as XORs, MUXs and adders can be realized efficiently.

CPL is a static gate, because outputs are connected to Vdd or GND through a low-resistance path (high noise resilience).

Design is modular – all gates use same topology; only inputs are permuted. This facilitates the design of a library of gates.

Advantages

- Minimum Threshold Voltage Loss.
- Less Power Dissipation.

IV. DRPTL ADDER

In this logic, Pass-Transistor is processed with the design of low power circuit. In pass network transistor is generated according to its function and perform sum and carry function as per the signal of a clock. At the end of generating voltage swing of the logic is performed. This logic provides improvement in speed, eliminating short circuit current in the output of inverter and includes voltage level restoration. The DRPTL logic leads to have an efficient implementation with a clock signal for efficient dynamic access. It provides fast process and dynamic synthesis of logic function in transistor network.

The process of dual rail signal and single rail system is shown in Fig.4.1. The proposed logic improves the dynamic circuit speed with the evaluation of clock signal logic with transistor. The supply of voltage is varied based on the charges phases. If the clock signal is equal to 1 in the evaluation phase, then the circuit will be discharged or pre-charge and if equal to 0 in pre-charge phase, then the circuit is charged and applies to voltage supply level from the transistor. Normally the power density and dissipation are the main objective and rapid growth in portable systems. In VLSI design, the widely used adder component provides better performances in the integrated circuit.

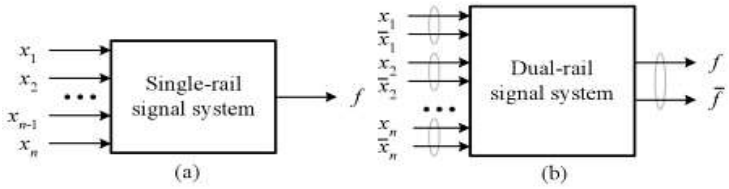

FIG 4.1: (A) SINGLE RAIL SIGNAL SYSTEM, (B) DUAL RAIL SIGNAL SYSTEM

V. SIMULATION RESULTS

5.1 Existing System

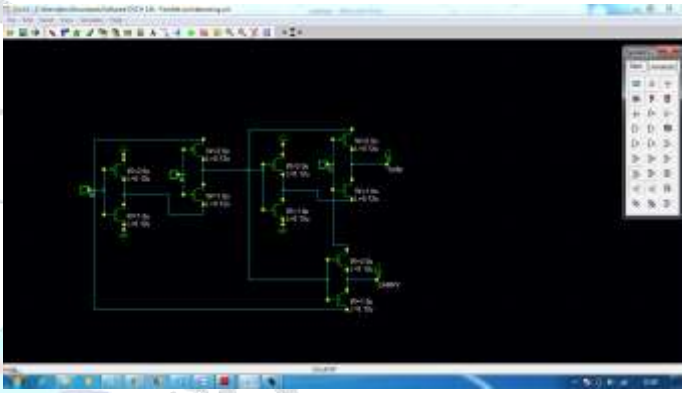

Fig 5.1.1 circuit diagram for existing method

To design a circuit intially open DSCH and Create our required design by using the tools in it.In the above circuit diagram there are totally 5 Pmos and 5 Nmos. A, B, and C are the inputs and Sum and Carry are the outputs. If the given inputs are active low then Sum and Carry are low. Similarly for active high inputs Sum and Carry are high. For remaining inputs it follows the full adder truth table.

Table 1: Truth table for FULL ADDER

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

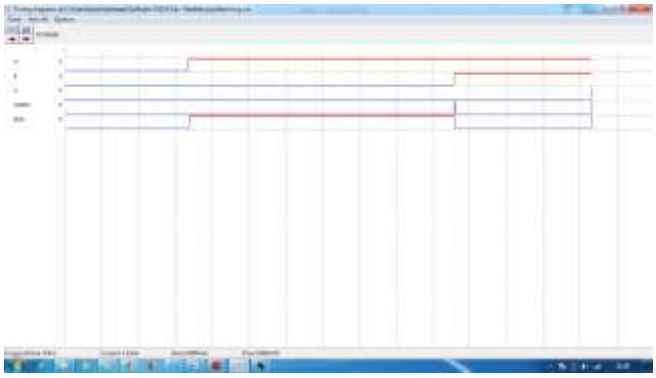

Fig 5.1.2 Timing Diagram For Existing Method

Based on the above truth table the timing diagram follows.

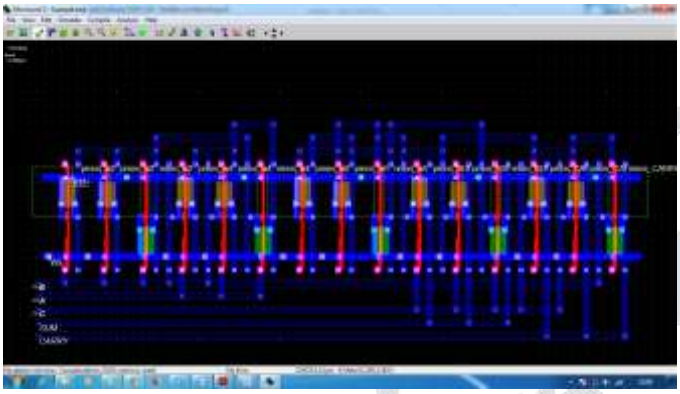

Fig 5.1.3 Layout Diagram

Based on the circuit that is designed in the DSCHand that file is linked to the MICROWIND software so it generates the layout diagram.

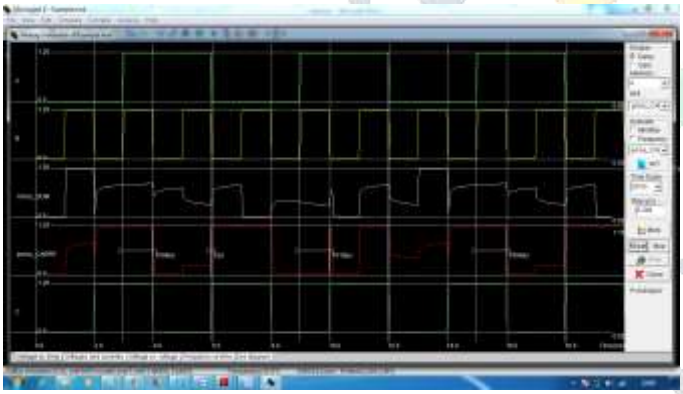

Fig 5.1.4 Analog Simulation

The simulation parameters have been analyzed with the help of the Micro wind tool and DSCH for the schematic verification. After simulating the layout design it shows waveforms of given inputs and also outputs waveforms and the power dissipation of the entire circuit. The power dissipation is 8.394µW.

DRAWBACKS:

- ✓ Poor Dynamic Access.
- ✓ More Delay.
- ✓ Considerable Short Circuit Current.

5.2 Proposed System

The optimized Pass Transistor logic as an alternative to reduce static power dissipation and avoids threshold voltage loss.

The MOS transistor is basically a switch. When used in logic cell design, it can be *on* or *off*. When *on*, a current can flow between drain and source. When off, no current flow between drain and source. The MOS is turned on or off depending on the gate voltage. In CMOS technology, both n-channel (and nMOS) and p-channel MOS (or pMOS) devices exist. The nMOS and pMOS symbols are reported below. The symbols for the ground voltage source (0 or VSS) and the supply (1 or VDD).The n-channel MOS device requires a logic value 1 (or a supply VDD) to be on. In contrary, the p-channel MOS device requires a logic value 0 to be on. When the MSO device is on, the link between the source and drain is equivalent to a resistance. The order of range of this 'on' resistance is 100Ω-5KΩ. The 'off' resistance is considered infinite at first order, as its value is several MΩ.

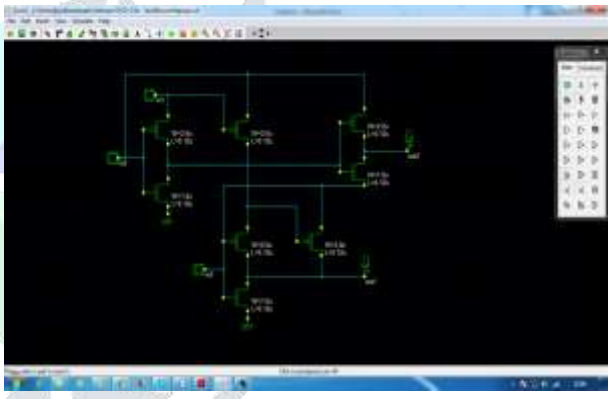

Fig 5.2.2 Circuit Diagram for proposed method

To design a circuit intially open DSCH and Create our required design by using the tools in it.In the above circuit diagram there are totally 5 Pmos and 3 Nmos. A, B, and C are the inputs and Sum and Carry are the outputs. If the given inputs are active low then Sum and Carry are low. Similarly for active high inputs Sum and Carry are high. For remaining inputs it follows the full adder truth table. Here we are reducing the no of Nmos when compared to existing method and this helps to reduce the area and also power dissipation.

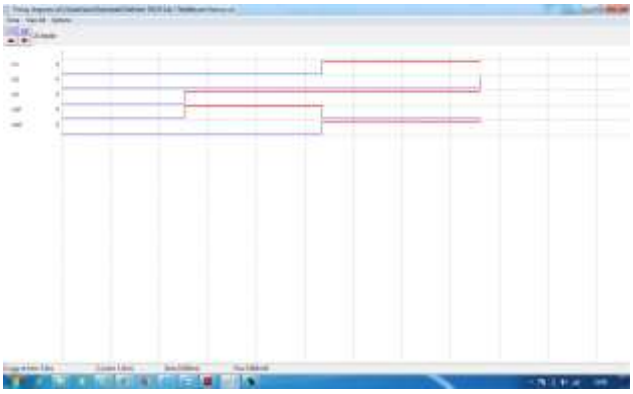

Fig 5.2.3 Timing Diagram for proposed method

Based on the above truth table the timing diagram follows.

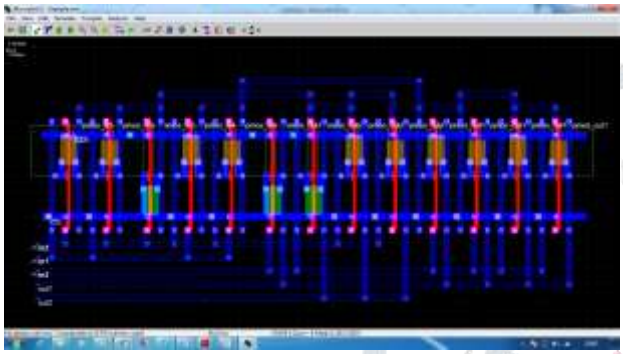

Fig 5.2.4 Layout Diagram

Based on the circuit that is designed in the DSCH and that file is linked to the MICROWIND software so it generates the layout diagram.

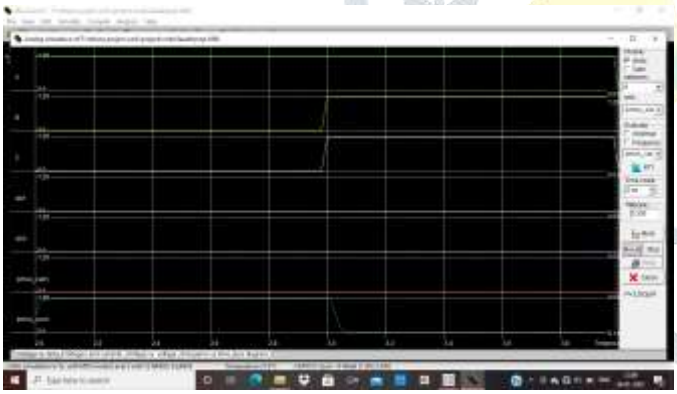

Fig 5.2.5 Analog Simulation

The simulation parameters have been analyzed with the help of the Micro wind tool and DSCH for the schematic verification. After simulating the layout design it shows waveforms of given inputs and also outputs waveforms and the power dissipation of the entire circuit. The power dissipation is P=3.203µW.

ADVANTAGES:

- Minimum Threshold Voltage Loss.
- Less Power Dissipation.

Table 1: COMPARISION BETWEEN THREE METHODS

Parameters	FA_Existing	FA_Proposed
Area Occupied	9.7%	5.0%
Power Dissipation	8.934µW	3.203µW
No. of Transistors Used	10	8
Output	Acceptable	Acceptable

VI.CONCLUSION

In digital design of submicron circuits, an internal logic circuit is proposed with the proposed approach to design and implement the circuit for efficient performances and analysis than the existing circuit. The proposed approach of the hybrid circuit provides faster process, less delay propagation, less power consumption and reduction in transistor count than the others. The DRPTL technology performance was with regard to the delay and power consumption of the submicron adder circuits used in digital circuitry. So the modified circuits satisfied VLSI requirements of an efficient submicron adder circuits.

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