Design and Implementation of High-Speed Vedic Multiplier

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ABSTRACT

This paper introduces a new design method for minor delays and Vedic repetitions effectively based on ancient Vedic Mathematics techniques. It is a N × N multiplication technique used and provides very little delay and an effective location for calculating multiplication. The efficiency of Urdhva Tiryagbhyam Vedic method for multiplication which is different from the process of normal multiplication is used. Urdhava Tiryagbhyam is the most efficient algorithm that gives minimum delay for multiplication for all types of numbers irrespective of their size. Vedic multiplier is coded in VHDL which is simulated and synthesized by using Xilinx ISE 14.7. The proposed design is analyzed according to the delay and memory usage.

Keywords: Vedic Multiplier, Urdhava Tiryagbhyam sutra, high speed, Digital signal processing.

I INTRODUCTION

Multiplication is a crucial component of arithmetic processes. Multiplication-based operations such as Multiply and Accumulates, as well as inner product, are among a number of commonly used computation-intensive arithmetic functions now carried out in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform, filtering, accumulator unit, and microprocessor arithmetic and logic unit. Given that multiplication takes up the majority of the execution time in most DSP algorithms, a high-speed multiplier is required. Currently, the most important component in determining the instruction cycle time of a DSP processor is multiplication time.

As the number of computers and virtual processing programs grows, so does the demand for high-speed processing. In many real-time signal and photo processing algorithms, higher throughput mathematical operations are required to achieve the necessary overall performance.Multiplication is an essential mathematical process in such applications, and the construction of quick multiplier circuits has been a hobby for decades. For many packages, lowering the amount of time they are turned off and the amount of electricity they use is a must.

Different multiplier architectures are presented in this paper. One of the quick and low-power multipliers is based on Vedic mathematics. Minimizing power consumption in digital systems necessitates design optimization at all levels. The technology utilized to create the digital circuits, the circuit style and topology, the architecture for implementing the circuits, and, at the highest level, the algorithms being implemented are all part of this optimization. In any digital circuit design, digital multipliers are the most widely utilized components.

The multiplier unit has a significant impact on the system's speed. This is one of the best places to practice multiplication using Vedic mathematics. They are components that are used to carry out any operation quickly, reliably, and efficiently. There are different types of multipliers depending on how the components are arranged. Depending on the application, a specific multiplier architecture is chosen.

II. VEDIC MULTIPLICATIONS

The usage of Vedic mathematics lies inside the fact that it reduces the standard calculations in conventional mathematics into quite simple one. This is so due to the fact the Vedic formulae are claimed to be primarily based on the natural concepts on which the human mind works. Vedic mathematics is a methodology of arithmetic rules that allow greater efficient speed implementation. Urdhva Triyagbhyam is the general formula applicable to all instances of multiplication.

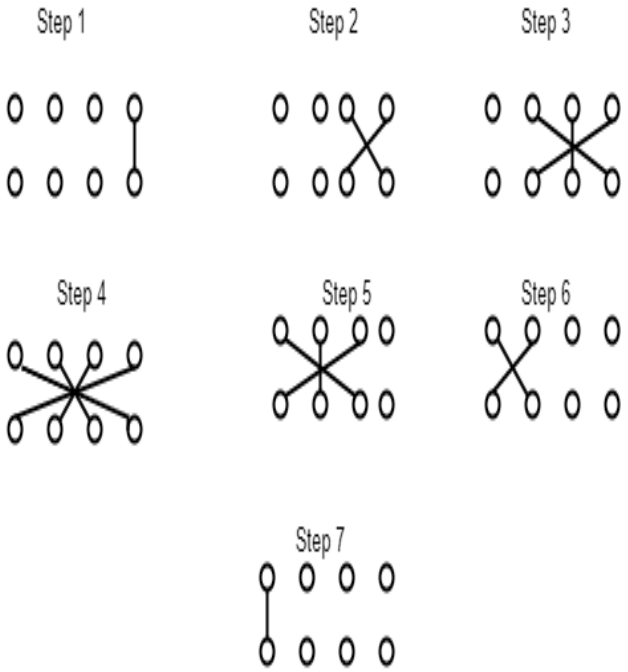

Fig. 1.Line diagram for two 4 bit number multiplications.

The carry from the previous step is doubled and added to the digits on both sides of the line. This generates one of the result's bits as well as a carry. The process continues when this carry is introduced in the next phase. If a step contains more than one line, all of the results are added to the preceding carry. The least significant bit serves as the result bit in each step, while the remaining bits serve as the carry for the following step. The carry is initially set to zero. The sutra is depicted in Figure 1.

Each block is a 2x2 bit Vedic multiplier, as seen above. A1A0 and B1B0 are the first two 2x2 bit multiplier inputs. The last block has a 2x2 bit multiplier with A3 A2 and B3 B2 as inputs. Two 2x2 bit multipliers with inputs A3 A2 & B1B0 and A1A0 & B3 B2 are shown in the middle. So the final result of the multiplication is S7S6S5S4S3S2S1 S0, which is an 8-bit result. The block design of a 4x4 bit Vedic multiplier is provided in Fig. 2 to help comprehend the concept. Four 2x2 bit Vedic multipliers and three 4-bit Ripple-Carry Adders are required to obtain the final product (S7 S6 S5 S4 S3 S2 S1 S0).

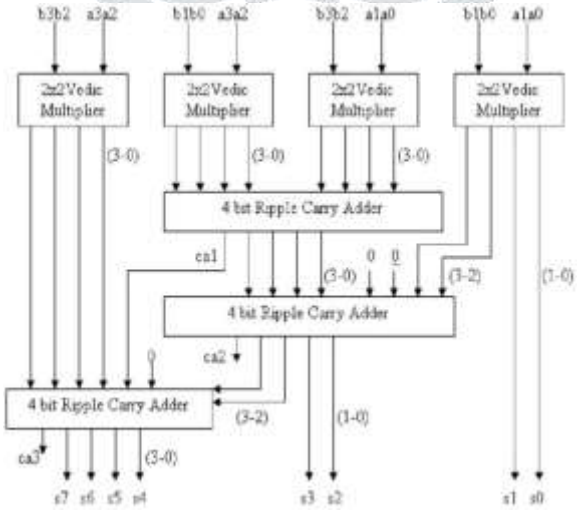

Fig. 2 Block Diagram of 4x4 bit Vedic Multiplier.

III. PRAPOSED DESIGN

Carry save adders were used to do three-bit addition at the same time. At the first stage, 3-bit input (A, B, C) is processed and converted to 2-bit output (S, C). The result carry is not propagated through the addition operation in the first stage.

By port mapping the entire adder VHDL code to a two-stage adder circuit, carry-save adder VHDL code can be created. To reduce delay, the proposed Vedic multiplier can be employed.

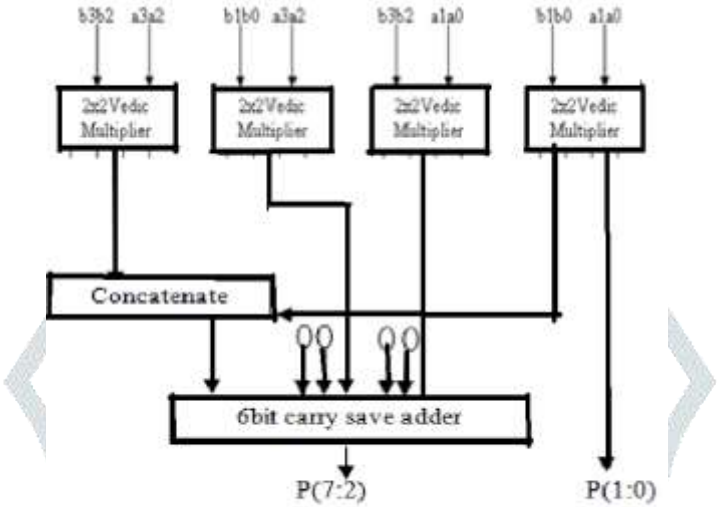

Fig. 3 Block Diagram of Proposed 4x4 bit Vedic Multiplier.

Instead of employing two 4 bit carry-save adders, we used only one 6 bit carry save adder in this architecture. The first partial products are created using a 2x2 Vedic multiplier, with the partial product acquired from the LSB 2x2 multiplier being Q0(3:0),Q0[1:0]=p[1:0], and the remaining bits Q[3:2] being concatenated to bits from the MSB 2x2 multiplier being Q3[3], Q3[2], Q3[1], Q3[0], Q3[0], Q0[3], Q0 Now \spartial products Q1, Q2 are concatenated with "00" in MSB side so as to take it 6 bit. As a result, a single 6-bit carry look-ahead adder is used to add three 6-bit values. As a result, instead of the three 4 bit adders used in Vedic Multiplier, this architecture only requires one 6-bit carry-save adder. Using a carry look-ahead adder and a ripple carry adder for 4x4 bits.

IV. SIMULATION RESULTS

In this work, 4x4 bit proposed design Vedic multiplier using Urdhva Tiryagbhyam Sutra is implemented in VHDL (Very High Speed Integrated Circuit Hardware Descriptive Language). Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in Xilinx 14.7 ISE- Project Navigator and simulator integrated in the Xilinx package respectively. Table 1 displays the simulation results of the proposed Vedic multiplier in terms of time delay (in nanoseconds). The combinational path delay obtained for the proposed 4x4 bit Vedic multiplier is 8.213ns. The performance is evaluated on the Xilinx device family Basys3 Artix-7 FPGA Board (Xilinx XC7A35T-1CPG236C.

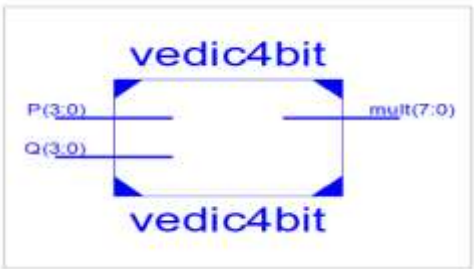

Fig. 4 Block diagram for 4x4 proposed design vedic Multiplier.

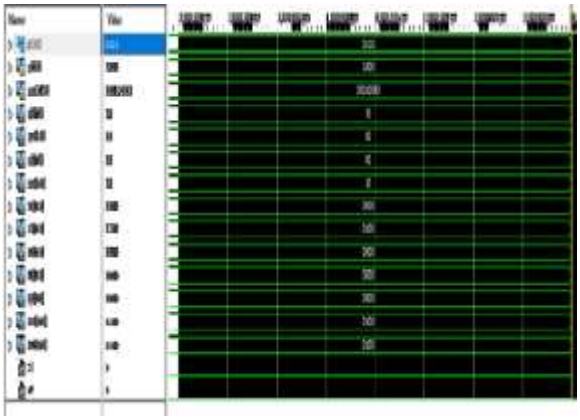

Fig. 5 Simulation results for 4x4 proposed design Vedic Multiplier.

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Table.1 Device Utilization summary			
Logic utilization	Used	Available	Utilization
Number of Slice LUTs	24	3200	<1%
Number of fully used LUT-FF pairs	0	32	0%
Number of IOBs	16	105	15%
Delay	8.213ns	--	--
Power	6.71mW	--	--

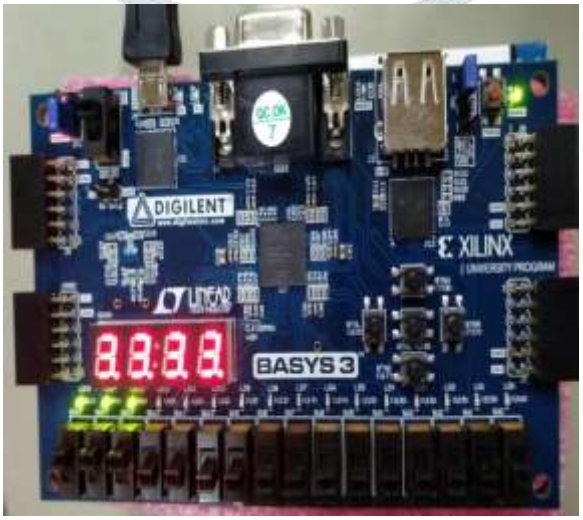

Fig. 6 Implementation of 4x4 Proposed design Vedic multiplier on BASYS 3 FPGA Board.

V. CONCLUSION

The design of the proposed 4x4 bit Vedic multiplier is implemented on Artix-7 Basys-3 FPGA Board. The computational path delay of the Vedic multiplier is found to be 8.213 ns. Hence it can be concluded that the performance of the proposed 4x4 bit Vedic multiplier seems to be highly efficient in terms of speed when compared to Conventional multipliers. Reducing the time delay and power are vital requirements for many applications and Vedic Multiplication technique is very much suitable for this purpose. The idea proposed here may be used for higher bit multiplication.

VI. REFERENCES

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