Reducing Power Dissipation in VLSI Circuits Using Low Power Techniques

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Abstract : This paper describes about different low power techniques that have been implemented using Verilog HDL and some of them using schematics also. Different low power techniques are implemented for different designs and they are simulated and synthesized. The designs are simulated and synthesized using Cadence tools. The net lists and power reports after synthesis have been generated by using the RTL compiler tool of CADENCE. The simulation waveforms with and without using the low power techniques for the designs are compared.

IndexTerms - Low power, Verilog, Simulation, Synthesis, Power.

I. INTRODUCTION

The need for low power electronic circuits is increasing with the proliferation of complex mobile gadgets into our daily life. Several low power techniques are proposed in literature as described below. A. P. Chandrakasan, S. Sheng and R. W. Brodersen [1] described about techniques for Low-Power CMOS Digital Design. Rung-Bin Lin and Chi-Ming Tsai [2] described about Theoretical Analysis of Bus-Invert Coding which consists of calculation of hamming distance in theoretical approach and also the effect of transitions on the bus. Diary RawoofSulaiman [3] described about Using Clock gating Technique for Energy Reduction in Portable Computers which presents a hardware design of the clock gating technique. Walter Aloisi and Rosario Mita [4] described about Gated-Clock Design of Linear-Feedback Shift Registers which consists of method to reduce the power consumption of the popular linear feedback shift register using clock gating technique. Xin Wang, Peter Noel and Tad Kwasniewski [5] described about low power design techniques for a modular multiplier which presents low power design techniques required to develop a high performance multiplier.

II. LOW POWER TECHNIQUES

The Design Styles mentioned in this paper have a significant impact on the overall power consumption of the circuits and they do not affect the functionality of the designs. Some low power techniques have been implemented using schematics also. The different low power techniques are described below.

2.1 Resource Sharing

The RTL coding should be carried out in a manner that there are no unwanted or redundant logic elements. Any logic element will contribute to power consumption as it has a capacitance attached to it and transitioning of data through that logic will lead to power dissipation. Resource sharing is an optimization technique that uses a single functional block (such as an adder or comparator) to implement several operators in the HDL code. The Simulation waveforms with resource sharing are shown in Figure 2.8. In this figure a, b, c, d are 16 bit inputs, sel is the single bit input and z is the 16 bit output. Depending on the sel line z gets the output either a & b or c & d. If a=16'h0011, b=16'h1100, sel =1'b1 then directly z gets 16'h0000 (a & b) and if c=16'0100, d=16'h0111,sel=1'b0 then directly z gets 16'h0100(c & d).

2.2 Register Retiming

Register timing is a concept mostly used in improving timing by reordering the combinational and sequential logic in a given data path. In certain cases, there is a saving of logic and thus can help improve upon power consumption. For example in the Figure 2.3 without retiming first two flip-flops(sequential) are used then sent to multiplexer(combinational) instead of that in Figure 2.4 with retiming first multiplexer is used to select one of the register inputs A or B then sent to the flip-flop so that only one flip-flop is required. Thus by rearranging the register blocks we can reduce the power consumption. The Simulation waveforms with register retiming are shown in Figure 2.9. In this figure, clk, rst, 'a',' b' are 16 bit the inputs, sel is the single bit input, out1 is the intermediate 16 bit output and out is the final 16 bit output. During positive edge of rst output out will be in reset i.e. 0 irrespective of the inputs. Now if rst is made low and the inputs a=16'h0011, b=16'b000A then, a or b selected depending on sel line and given to out1. If sel=1'b0 then out1=16'h0011 otherwise out1=16'b000A.Now out1 is given to flip-flop i.e at positive edge of clk the value present in out1 is given to out. Therefore this design has no timing problems as the final output depends on the clock and also only one flip-flop is used.

2.3 Power optimization using Operation Substitution:

Certain operations require more computational energy than others. In DSP circuits, multiplication and addition are the two most important operations performed. Multiplication consumes more energy per computation than addition. Hence replacing multiplication by addition can not only save area but also achieve improvement in power dissipation so that energy per consumption is reduced but this is achieved at the cost of small increase in delay. The Simulation waveforms with operation substitution are shown in Figure 2.10. In this figure n is parameter, a is 4 bit input clk, rst are the single bit inputs and sum is the 4 bit output. During positive edge of rst output prod will be in reset i.e. 0. On the application of rst low and positive edge of clk the addition result of n times of 'a' will be stored in sum for example a=4'b0101 and n=4'b0011 clk=1'b0->1'b1 rst=1'b0 then sum=4'b1111 after 3 clock cycles.

2.4 Power optimization using Operation Reduction:

Reducing the operations count reduces the total capacitance associated with the system and hence can reduce power dissipation. Consider the implementation of function X^2+AX+B. A straight forward implementation is shown in Figure 2.5 and the implementation shown in Figure 2.6 has one less multiplier reducing the area and power. The critical path for both the implementations are same so the throughput maintained is constant. The Simulation waveforms with operation reduction are

shown in Figure 2.11. In this figure a, b, x are the 4 bit inputs and p, q are the 8 bit intermediate wires and y is the 8 bit output. The whole implementation is $y=x^2 + ax + b=x (a*x) + b$ so that p is assigned a + x, q is assigned p * x and r is assigned b. For example a=4'b7, b=4'h9, x=4'h6 then p=8'h0D (i.e. decimal 13), q=8'h4E (i.e. decimal 48) finally z=p + q=8'h57 which is same as without operation reduction. From the above simulation results the functionality of operation reduction technique has been verified.

2.5 Reducing power dissipation in dynamic memories

In case of dynamic memories the data will be stored by charging or discharging the capacitance through bit line and controlling the operation using word lines. In this technique by reducing the voltage and increasing the capacitance we can save some power. This is verified by simulating one bit dynamic RAM (Random Access Memory) cell as shown in Figure 2.7 and the power dissipated with different voltages and capacitances is shown in Table 2.1. From this table it is observed that the power dissipation in dynamic RAM cell is reduced by reducing the voltage and increasing the capacitance. The circuit has been simulated at W=720nm and keeping L=180nm and the power dissipation and delays are shown in table form below.

Table 2.1: Power report for dynamic memory

Voltage	Capacitance	Power (W)	Rise delay	Fall delay
3.6 volts	15 fF	1.39×10^{-9}	2.8 ns	2.4 ns
1.8 volts	30 fF	1.31×10^{-9}	3 ns	2.6 ns

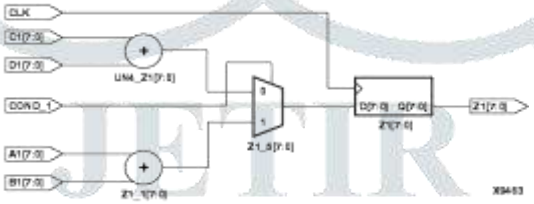

Figure 2.1: Implementation without Resource Sharing

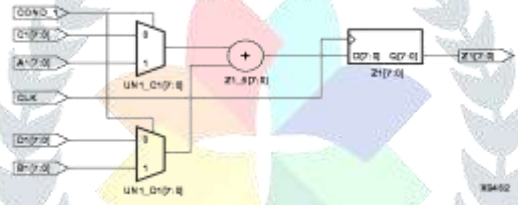

Figure 2.2: Implementation of Resource Sharing

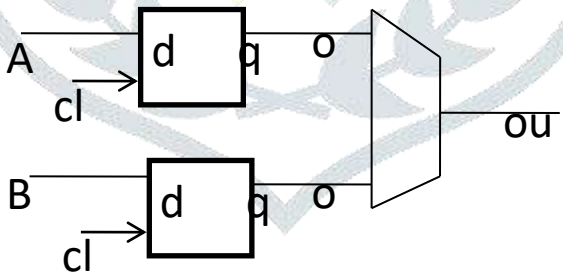

Figure 2.3: Implementation without Register Retiming

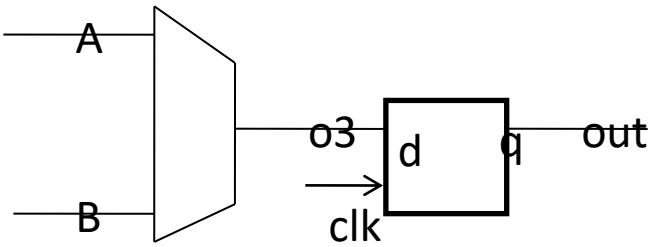

Figure 2.4:Implementation with Register Retiming

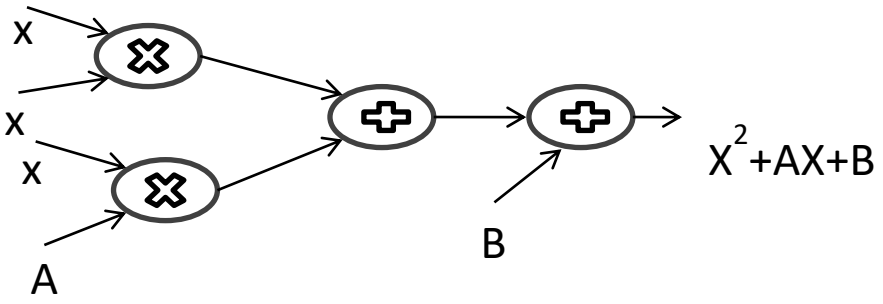

Figure 2.5: Implementation without Operation Reduction

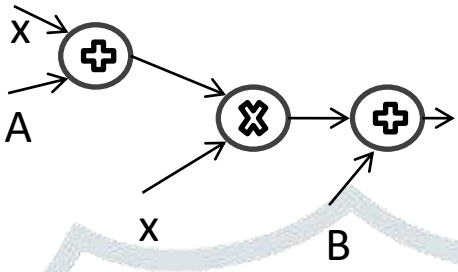

Figure 2.6: Implementation with Operation Reduction

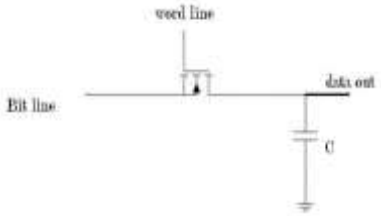

Figure 2.7: Dynamic memory Cell

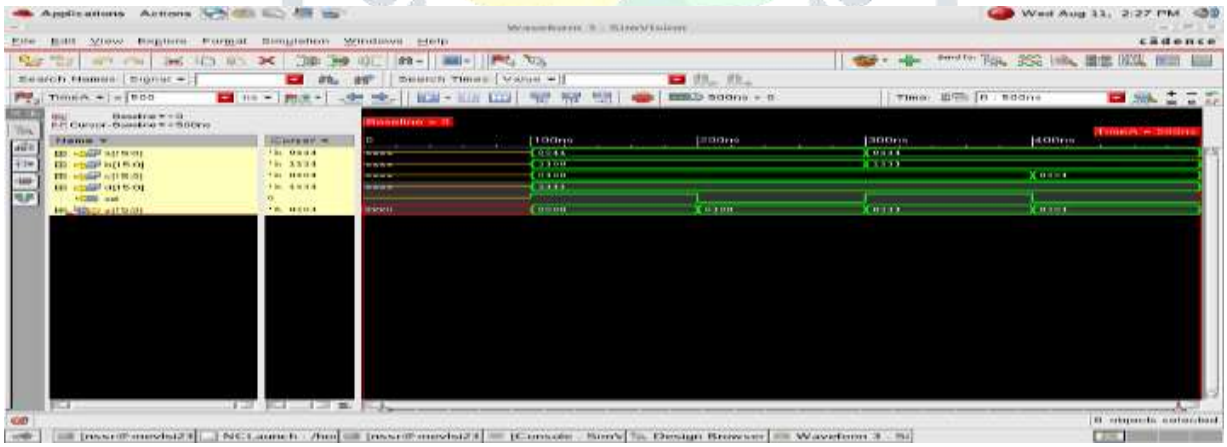

Figure 2.8: Simulation Waveforms with the application of Resource Sharing

Figure 2.9: Simulation waveforms with the application of Register Retiming

Figure 2.10: Simulation waveforms with the application of Operation Substitution

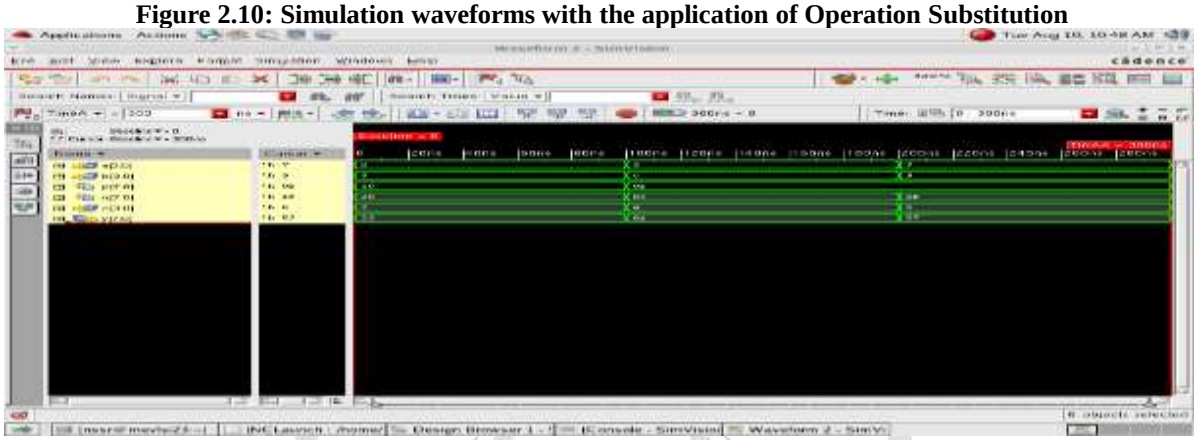

Figure 2.11: Simulation waveforms with the application of Operation Reduction

III. RESULTS AND DISCUSSION

The comparison of power saving using Low power techniques is shown in table 3.1 , which shows that there is power saving when these low power techniques are used.

Table 3.1. Comparison of power saving using Low power techniques

S.No	Low power technique	Power dissipation without low power technique (nw)	Power dissipation with low power technique(nw)	Percentage saving in power dissipation
1	Resource sharing	45776	344433	25 %
2	Register retiming	839154	640651	24 %
3	Operator substitution	271402	181864	33 %
4	Operation reduction	274084	260380	5 %

IV. CONCLUSIONS

The overall power consumption is reduced by sharing the resources. By rearranging the register blocks also, the power consumption in the circuits is reduced. Power dissipation is also minimized by operation reduction and operation substitution. The power dissipation is minimized by operating the circuits at lower voltages and reducing the quiescent current of operation. The power dissipation in dynamic memories is reduced by decreasing the voltage and increasing the capacitance value.

FUTURE SCOPE

In this paper, some of the low power techniques are used. . However, there is scope for applying several other low power techniques like creating power domains, application of DVFS (Dynamic Voltage Frequency Scaling), power shut-off techniques, substrate biasing and further optimize the overall power consumption in the VLSI circuits at lower technologies.

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