Area Efficient Three-Input XOR/XNOR Circuit

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Abstract: As these circuits are fundamental building blocks of many arithmetic circuits, we present a novel three input XOR/XNOR circuit in this article to enhance performance and decrease space. To begin, choose a simple cell with three independent inputs and two complimentary outputs. Then, using different correction and optimization methods, we construct a flawless XOR-XNOR circuit with complete swing operation. We propose and build a 3-input XOR/XNOR gate using 8 transistors in this article, and compare it to current designs. In this article, we can build a suggested design utilizing a 180 nm CMOS technology process and Micro wind simulation findings. The employment of XOR–XNOR circuits in complete adder circuits, compressors, parity checks, and comparators has been the subject of many studies. The suggested designs outperform the current three-input XOR/XNOR circuits in terms of performance. In comparison to prior circuits, we utilized several kinds of optimization and correction methods to decrease the number of transistors.

Index Terms – XOR/XNOR Circuits, Microwind, Digital schematic.

I. INTRODUCTION

Designing low-power, high-speed (LPHS) circuits that occupy tiny chip areas has become a crucial issue with the increasing development of portable electronic devices. Many articles have been published that compete in the creation of improved circuits. These studies are mostly based on innovative design concepts, although they do not use a systematic approach. A well-structured design approach may be seen as a viable solution to the problem. It is not based on trial and error, but rather on a systematic and intentional approach to the design objectives. It also selects circuit components intelligently and does not wait until after simulation to determine circuit characteristics. In the hybrid-CMOS approach, cell design methodology (CDM) has been given to design certain restricted functionalities, such as two-input XOR/XNOR and carry–inverse carry. The majority of the findings encourage us to enhance CDM in two stages: 1) creating more complicated functions, and 2) correcting certain remaining faults.

The shortcomings in earlier versions of CDM include the inclusion of certain manual stages in the design flow and the generation of a huge number of designs from which the most important ones would be chosen after simulations were completed. As a result, a three-input XOR/XNOR has been selected as one of the most complicated and all-purpose three-input fundamental gates in arithmetic circuits in the first stage. If the circuits' efficiency is verified in such a competitive setting, it may demonstrate the methodology's strength. In the second step, CDM is developed as systematic CDM (SCDM) for the first time in constructing three-input XOR/XNORs. It uses a binary decision diagram (BDD) to methodically create elementary basic cells (EBC) and intelligently selects circuit components depending on a particular goal. This occurs when the CDM fails to take into account the aforementioned characteristics. After systematic generation, the SCDM analyses circuit optimization in three steps: 1) smart selection of the basic cell, 2) wise selection of the repair mechanisms, and 3) transistor size. It's worth noting that BDD may be used to generate EBC for various three-input functions. The power-delay product (PDP) is the design goal for us. It serves as a reasonable performance measure for portable electronic system goals. The existence of certain unique characteristics and the possibility to build some efficient circuits that enjoy all of these benefits motivates the usage of this approach.

1) A circuit structure is divided into a primary structure and optimization-correction mechanisms by the SCDM. It takes into account characteristics such as the smallest number of transistors in the critical route, well balanced outputs, being power ground-free, and symmetry in the primary structure. The mechanisms are responsible for completing the circuits' functioning, preventing output voltage deterioration, and improving driving capacity.

2) Having fewer transistors in the critical route improves the likelihood of the circuit having superior characteristics, with experimental findings indicating average savings of 10%–50% and 27%–77% in terms of delay and Energy-Delay Product (EDP), respectively.

3) The well-balanced propagation delay is the source of dynamic consumption optimization. This function is useful in situations where the skew between incoming signals is essential for correct operation, as well as in cascaded systems to minimise the risk of glitches.

4) A primary structure with no power ground reduces power.

5) Because of the symmetrical structure, high modularity, and regular arrangement of designs, more wells of linked transistors may be shared, decreasing the occupied space by approximately 26%–32%.

6) As a result, all output voltage swing deterioration may be entirely eliminated, making the device suitable for low VDD operations and low static power consumption.

The systematic approach leads to automated flow, which may decrease design time and costs, provide consistency in the cell library production process, expand the range of simulation capabilities at the characteristics phase, and reduce the risk of mistakes.

II. PREVIOUS WORKS

The technique for three-input XOR/XNORs is described in this section using the flowchart illustrated in Fig. 1 (a). EBC methodical generation kicks off the design process. In this phase, the most important design objectives are to provide reasonably balanced outputs, have a symmetric and power-ground-free structure, have fewer transistors in the critical path, and share a common sub circuit. In Section II-A, the systematic creation method of EBC is described in depth. In the following stages, the approach allows you to work toward a specific design goal. From a PDP standpoint, two of these stages involve carefully selecting mechanisms and basic cells. An in-depth examination of the options for choosing in terms of representation of three-input XOR/XNOR function. (c) Applying reduction rules. (d) Substitution and disjointing. (e) EBC. In the last step, in order to put the resultant circuits in proper state, a sizing algorithm consistent with the methodology is indispensable. In this line, SEA algorithm that is simple exact algorithm with the capability of determining goal is picked.

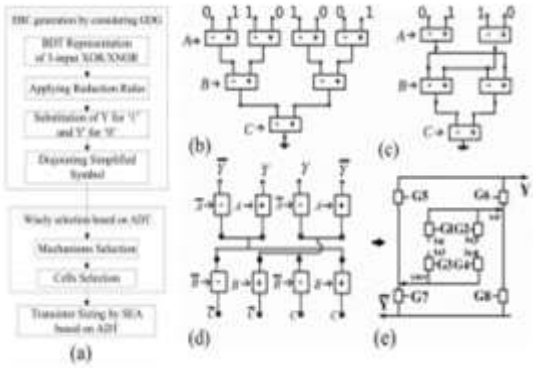


Fig.1 (a) SCDM process for designing efficient three-input XOR/XNORs. (b) BDT

A. Elementary Basic Cell Systematic Generation

In order to generate the EBC of three-input XOR/XNOR circuits, four steps is taken. The process has been shown in Fig. 2(b)–(e). Initially, three-input XOR and its complement are represented by one binary decision tree (BDT) in order to share common sub circuits. The BDT is achieved by some cascaded 2 × 1 MUX blocks, which are denoted by simplified symbol controlled with input variables at each correspondent level. This construction simply implements the min-terms of the three-input XOR/XNOR function, as shown in Fig. 2(b). The step is followed by applying reduction rules to simplify the BDT representation. These include elimination, merging, and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. The trees are acquired by impacting the state matrix on the corresponding control matrix where the multiply and add operators operate as follows:

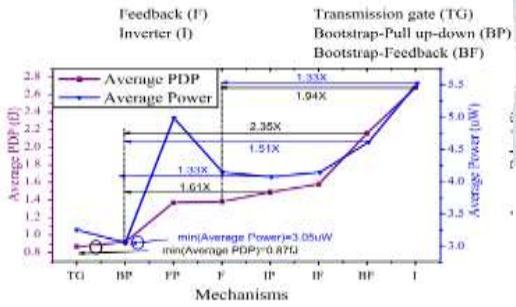


Fig. 2. (a) Average PDP and power order of mechanisms.

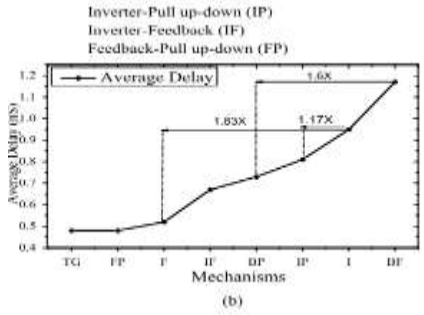


Fig.2. (b) Average delay order of mechanisms.

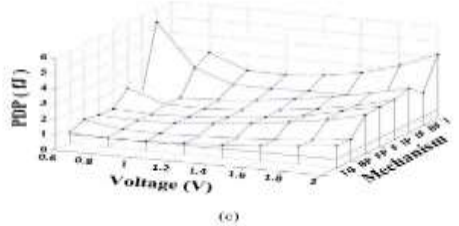


Fig.2.(c) PDP results of mechanisms (0.6–2 V).

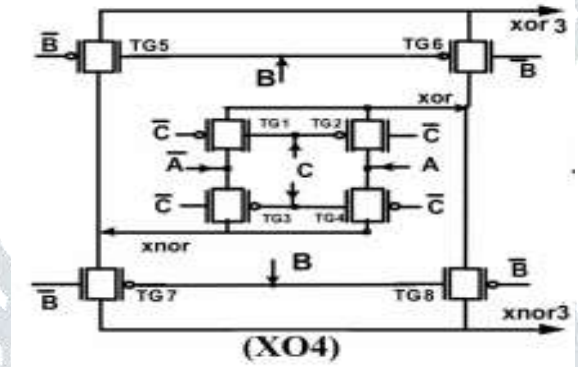
B. Wisely Selection of Mechanisms and Cells

Based on Design Target By replacing the elements with pass transistors or transmission gates and the control inputs with input signals in combination with optimization and correction mechanisms, a huge circuit library is achieved as each circuit can be appropriate for specific applications. The selection is meditated to determine dominant mechanisms and cells, in terms of PDP, power, and delay when the optimization goal is PDP. The results are used to produce

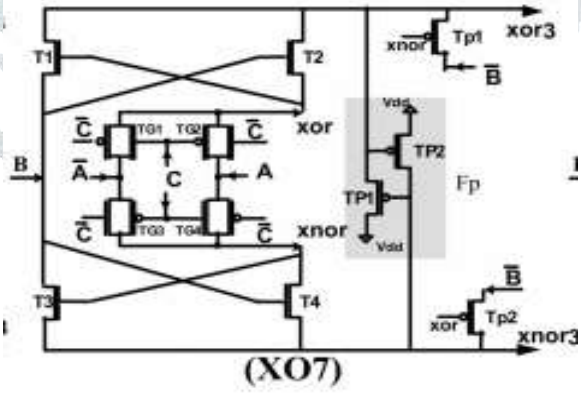
Circuits for high-performance portable electronic applications. Mechanisms include optimization mechanisms to resolve non-full swing [inverter (I) and feedback (F)], correction mechanisms to resolve high impedance [pull up-down network (P) and feedback (F)], or the combinations of them [bootstrap-pull (BP) up-down, feedback pull (FP) up-down, bootstrap-feedback (BF), inverter-feedback (IF), and inverter-pull (IP) up-down]. The cells are divided into three categories: 1) cells with both NMOS and PMOS in EBC structure (C1); 2) only NMOS (C2); and 3) only PMOS (C3). To reduce complexity, we have also considered the central part of EBC and to achieve real results, the circuits have been simulated in the chain test bench [7].

Fig. 2(a) shows the order of mechanisms in terms of average power and PDP in voltage range from 0.6 to 2 V. If the concentration is on delay consumption, the right chart can be useful [Fig. 2(b)]. Fig. 2(c) also shows the PDP details for different mechanisms. The first experiment that studies the performance of the inverter mechanism shows I suffers from more power and PDP in comparison with other mechanisms. The PDP details of I in Fig. 2(c) also demonstrates that there is an inconsistency with the voltage reduction in the mechanism as I has the minimum supply voltage of 0.8 V.

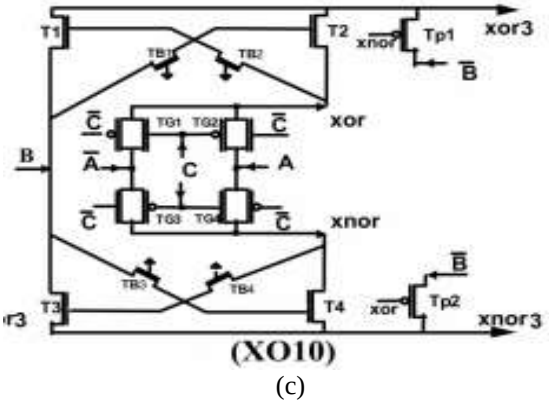
The struggle will be more critical when the F transistors are driven by the nonfull swing outputs or they should resolve solely the high impedance problem, because they should be strong enough to do the duty. The stronger the F transistors, the more the struggle and their consequences are more likely to happen. As a result, in these cases, it is better that high impedance duty is solved by P. As we can observe from Fig. 2, the mechanisms IP, BP, and FP use P for high impedance and exhibit a power saving of 2%–34% and a PDP improvement of 5%–57% rather than both IF and BF.



(a)



(b)



(c)

Fig.3.Three-input XOR/XNOR circuits, (a) XO4, (b) XO7, and(c) XO10

III. PROPOSED METHOD

Extensive simulations have been performed to compare the five presented DET flip-flops against each other and also against six previously reported DET flip-flop designs. Two versions of the novel FN_C flip-flop have been considered: The version presented in Fig. 10 and the version with the symmetric C-element of Fig. 1(b) replacing the weak-feedback output C-element. The latter version is denoted as FN_C (sym.) in the comparison. For a fair comparison, all flip-flops include input, output, and clock buffering.

In proposed method we can design 3-input XOR/XNOR Gate by using 8 transistors so compare to existing method we reduce to half of the transistors. In Fig: 4 we can use two outputs Y and Y1.Y is the output of 3-input XOR Gate and Y1 is output of 3-input XNOR Gate. The circuit diagram of proposed is illustrated in fig: 4.

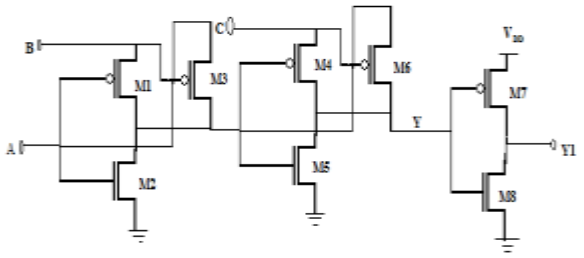


Fig: 4 3-input XOR/XNOR Gate

Operation of proposed method we can explain by using table: 1.The proposed method consists of 8 transistors in this 5 pmos and 3 nmos. Depending upon input sequence transistor operate either ON or OFF. Pmos ON when input is '0' and OFF when input is '1' and nmos ON when input is '1' and OFF when input is '0'. By depends this operation we can explain the proposed method operation. See the table: 2 mainly this explain how operate the circuit depends on input sequence.

A	B	C	M1	M2	M3	M4	M5	M6	M7	M8	Y	Y1
0	0	0	ON	OFF	ON	ON	OFF	ON	ON	OFF	0	1
0	0	1	ON	OFF	ON	ON	OFF	OFF	OFF	ON	1	0
0	1	0	ON	OFF	OFF	OFF	ON	ON	OFF	ON	1	0
0	1	1	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	0	1
1	0	0	OFF	ON	ON	OFF	ON	ON	OFF	ON	1	0
1	0	1	OFF	ON	ON	ON	OFF	OFF	ON	OFF	0	1
1	1	0	OFF	ON	OFF	ON	OFF	ON	ON	OFF	0	1
1	1	1	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	1	0

Table: 2 proposed method Transistor ON/OFF condition depends on input

IV. SIMULATION RESULTS

This section describes performance of the proposed design using Microwind tool on technology. The simulated output of 3 input XOR/XNOR gate as shown in figures.

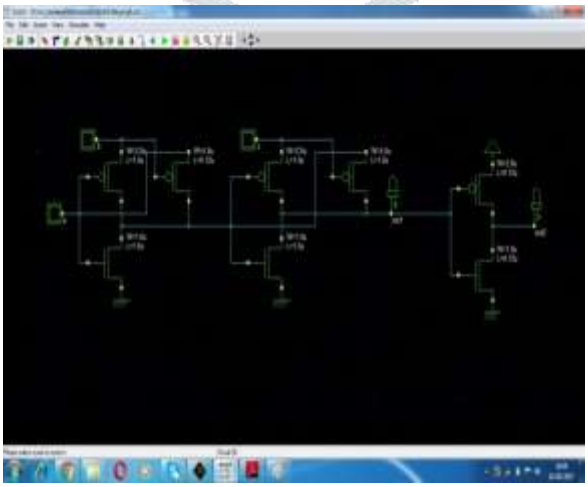


Fig: 5 schematic of proposed 3 input XOR/XNOR gate

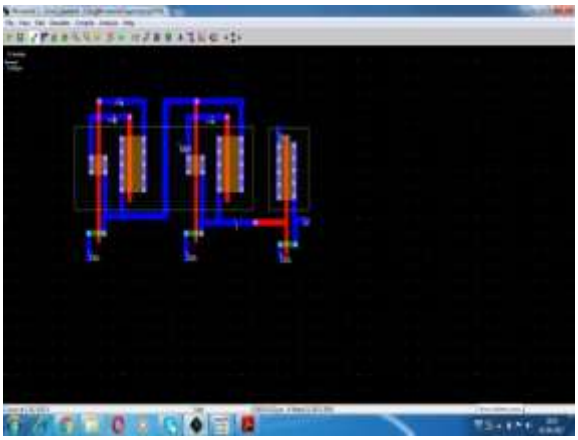


Fig: 7 Layout of 3 input XOR/XNOR gate

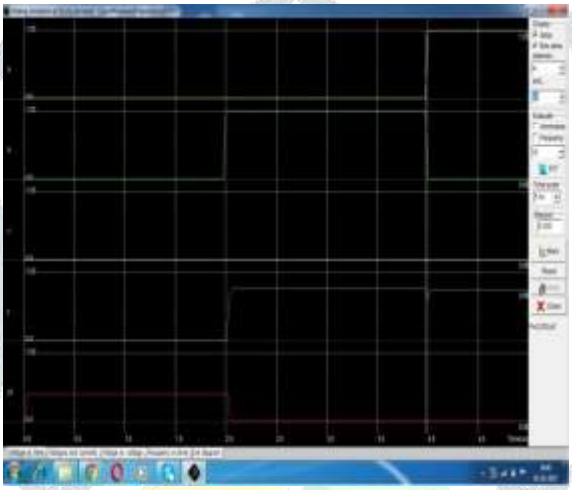


Fig: 7 simulated output of 3 input XOR/XNOR gate

V. CONCLUSION

SCDM is a design technique for three-input XOR/XNOR, which is one of the most sophisticated and competitive three-input basic gates in arithmetic circuits, as well as an all-purpose three-input basic gate. The technique emphasizes following a methodical approach to all of the stages. It also has a lot of design freedom while still following the same process to produce state-of-the-art designs. With the careful selection of circuit components for the PDP goal, this brief has benefited SCDM. Finally, utilizing SCDM, we can present a novel high-performance three-input XOR/XNOR circuit with lower PDP and a smaller footprint. The new circuit has a greater driving capability, a higher transistor density, operates at a lower voltage, and has a lower chance of producing glitches. The critical route of the proposed designs is made up of just two transistors, resulting in a short propagation delay. In MICRO WIND simulation based on CMOS 35-nm technology, these circuits beat their equivalents by 17 percent –53 percent and 27 percent –77 percent, respectively, in PDP and EDP. With the benefits of regularity and symmetry in layout, the suggested circuit's area utilization increases by 26 %–32 %.

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