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A NEW INTERLEAVED ZVS REASONANT CONVERTER USING DICKSON SWITCHED CAPACITOR CONFIGURATION

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***Abstract*— In this paper, A New Automatic Interleaved Dickson Switched-capacitor Converters (AIDSCC) and its ZVS resonant configuration are proposed. Different from the traditional Dickson switched-capacitor converter (SCC), the AIDSCC has symmetrical configuration with functions of interleaved input current, small output voltage ripple and decrease peak capacitor voltage strain. To improve the line regulation capability, one small resonant inductor is inserted and two bulky capacitor banks are changed through two smaller resonant capacitors, forming the Resonant AIDSCC. The transistors are ZVS became on and diodes are ZCS grew to become off through running above the resonance. With frequency modulation inside an affordable range, the voltage-gain variety of the Resonant AIDSCC is elevated substantially, even as sacrificing the most performance due to the higher conduction loss.**

***Index Terms*—Switched-capacitor converter (SCC), Automatic Interleaved Dickson SCC (AIDSCC), resonant switched-capacitor converter (RSC).**

I. INTRODUCTION

Switched-capacitor converters (SCCs) got appealing throughout the most recent couple of decades because of the upsides of high force thickness, little size, light weight and low electromagnetic impedance (EMI) contrasted with the customary inductor-based switch-mode power flexibly (SMPS).

Earlier thyristors were used in converters for wide range of power applications. The main problem with thyristor is commutation. It can be either natural or forced. One such forced commutation circuit involves a LC resonant circuit, for forcing the current to zero during the turn OFF process. This technique is a type of zero current turn OFF process. The use of a resonant circuit for achieving zero current switching or zero voltage switching has emerged as a new technology for power converters. The concept of a resonant switch replacing a conventional power switch is introduced in this section.

A resonant switch is a sub circuit composed of a semiconductor switch S and resonant elements L_r and C_r. Switch S can be implemented by a unidirectional or bidirectional switch which determines the operation mode of the resonant switch.

Two types of resonant switches depending on whether the current through or the voltage across the switch is made zero are implemented:

(1) *Zero-Current (ZC) Resonant Switch:* A switch that operates with zero current switching technique has an inductor in series with it. Switch current resonates only in the positive half cycle if the switch is unidirectional; creating a half wave mode of operation. Current through the switch can flow in both directions if the diode is connected antiparallel to the unidirectional switch. In this case, the resonant switch operates in full wave mode. The switch is turned ON with zero current and the switch current oscillates due to the resonance between L_r and C_r. This switching is used to shape the waveform during conduction and to create a zero-current conduction for the switch to turn OFF.

(2) *Zero-Voltage (ZV) resonant Switch:* This technique operates with a capacitor across the switch. In a unidirectional switch, Voltage across capacitor C_r oscillates both in positive and negative half cycles freely and hence the resonant switch operates in full wave mode. During the negative half cycle, resonant capacitor voltage gets clamped to zero by the diode when it is antiparallel to the switch ensuring

the half wave operating mode. Voltage across the switch tends to zero, causing the switch to be turned ON with ZVS - if negative current is forced to flow through the anti-parallel diode. Switch voltage waveform during OFF time can be shaped by using the resonant circuit. This creates a zero-voltage condition for the switch to turn ON which is the sole purpose of a ZV switch.

To obtain loss-less switching, soft switching techniques are preferred at high switching frequency. The advantages of soft switching are:

- High frequency operation is possible
- Reduction in the converter size
- Less EMI as switching process is not abrupt
- Parasitic capacitance energy can be recovered completely

This paper gives an introduction to Switched Mode Power Supply (SMPS). The requirements of a SMPS and various types of DC-DC converters (isolated and non-isolated) are also discussed. The concept of resonance, quasi-resonance, hard switching and soft switching are deliberated at full length.

Many analog and digital electronic systems require regulated DC power supplies. These power supplies should adhere to certain requirements such as:

- Regulated Output: The output voltage must remain constant within a specified range for variations in input voltage and output load.
- Isolation: The input and the output must be electrically isolated.
- Multiple Outputs: Multi-output (positive and negative outputs) that may differ in voltage and current ratings must be isolated from one another.

Reduction in power supply size, weight and improvements in efficiency are additional requirements. Traditionally, linear power supplies were used. SMPS, as compared to linear power supplies, are smaller and much more efficient due to advancements in semiconductor technology. The cost comparison between linear and SMPS depends on the power rating. High frequency transformer provides electrical isolation in SMPS. In general, switch mode converters can be either Isolated or Non isolated. By isolation, it is implied as galvanic isolation so that there is no DC path from the input of the converter to its output. In order to meet the requirements of various agencies, electronic equipment operating from the AC power line needs at least one stage of isolated conversion. Non-isolated converters are Buck, Boost and Buck-boost converters. Isolated converters are Forward, Flyback, Half Bridge, Full Bridge and Push-pull converters.

II. STEADY STATE ANALYSIS OF AIDSCC

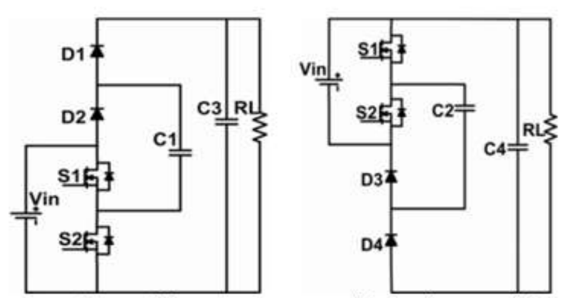
A. Topology

The topology of traditional 2X Dickson SCC is given in Fig. 1(a). In brief, while is grew to become on, the enter supply expenses, and period in between the output capacitor prices the load. When is became on, and are cascaded to charge each and the load The drifting 2X Dickson SCC with a similar activity standard is given in Fig. 1(b), while the info and yield don't have a similar ground. When is turned on, the information source charges, and interim the yield capacitor charges the heap. When is turned on, the and are fell to charge both and the heap.

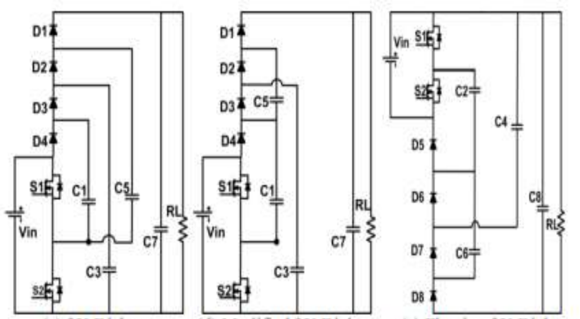
The topology of regular 3X Dickson SCC is given in Fig. 1(c). In a word, when is turned on, the info source charges, and interim the charges.

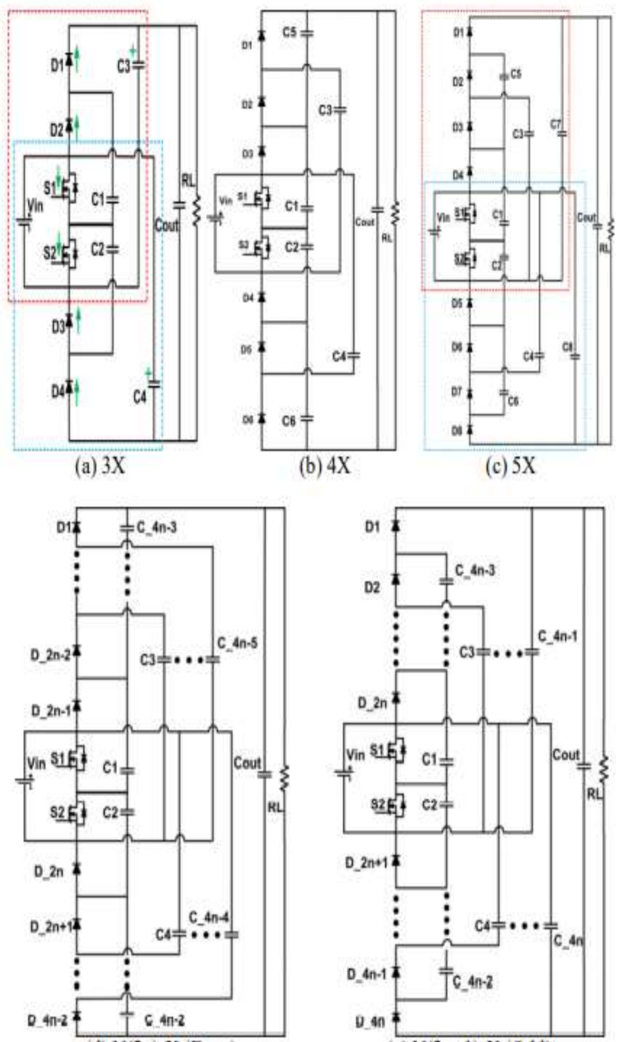
. When is turned on, the and are fell to charge, and interim the and charge the heap in arrangement.By changing the situation of as appeared in Fig. 1(d), the working standard holds, while the voltage weight on will be decreased from to. Comparably, the drifting 3X Dickson SCC with a similar activity rule is given in Fig. 1(e).

The topologies of the proposed AIDSCC are appear in Fig. 2. For instance, the customary 2X Dickson SCC (featured with the red line) and the skimming 2X Dickson SCC (featured with the blue line) are stacked to frame the 3X AIDSCC in Fig. 2(a). The two transistors are multiplexed to accomplish the programmed interleaving. At that point by including a lot of one diode and one capacitor to both top and base sides of the 3X AIDSCC, the 4X AIDSCC is determined in Fig. 2(b). Similarly, the 5X AIDSCC is inferred in Fig. 2(c) by stacking 3X Dickson SCC (featured with the blue line) and the skimming 3X Dickson SCC (featured with the blue line) together. The summedup N-X AIDSCCs with even request and odd request are appeared in Fig. 2(d) (e).



(a) 2X Dickson (b) Floating 2X Dickson


(c) 3X Dickson (d) Modified 3X Dickson (e) Floating 3X Dickson
Fig 1. Topologies of Dickson SCC


(a) 3X (b) 4X (c) 5X
(d) N(2n)-X (Even) (e) N(2n+1)-X (Odd)
Fig. 2. Topologies of AIDSCC

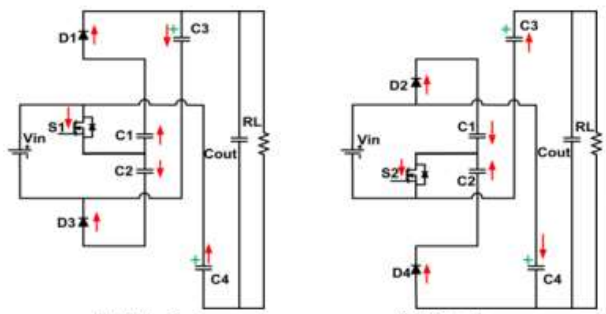
B. Operation Principle

A 3X AIDSCC is exemplified to present the working standard. Expect that the capacitors are sufficiently huge and can be completely energized in each exchanging cycle, so the voltage across them is viewed as a consistent. The parasitic components of all segments are overlooked. Obligation pattern of the two complimentary driving signs for is 0.5.

In state 1, the switch , and are turned on, as appeared in Fig. 3(a). The will charge to the voltage level . Interim, the and are associated in arrangement to charge . Since the voltage level of has been charged to in the past express, the voltage level of is . Interim, the is released by the heap current.

In state 2, the switch , and are turned on, as appeared in Fig. 3(b). The will charge to the voltage level . Interim, the and are associated in arrangement to charge to the voltage level . Interim, the is released by the heap current.

In the two expresses, the yield voltage is equivalent to , so the yield voltage is in consistent state. The exchanging plans of 3X AIDSCC in consistent state are summed up in table 1. The " implies the capacitor is charged, while the " implies the capacitor is released.


(a) State 1 (b) State 2
Fig. 3. Switching States

III. STEADY STATE ANALYSIS OF RESONANT AIDSCC

Like the conventional Dickson SCC, the voltage increase of DSCC is foreordained by the circuit setup with a little space for down modification while their productivity endures a ton. To improve the line guideline extend, the Resonant AIDSCC is proposed by acquainting a full tank with the AIDSCC.
A 3X Resonant AIDSCC is appeared in Fig. 4, where the thunderous tank is featured in a red circle. Contrasted with 3X AIDSCC, just a single little full inductor is included, while two massive capacitor banks are supplanted by two a lot littler thunderous capacitors.

B. Operation Principle

For the 3X Resonant AIDSCC, the obligation pattern of and is fixed at 0.5 and their driving signs are complimentary with a short dead-time. The exchanging recurrence is worked in the scope of , where is the resounding recurrence. The voltage across is signified as . The flows moving through , switches and diodes ~ are spoken to by , and individually. The characterized positive headings are indicated in green bolts in Fig. 4. The working waveforms and exchanging states are appeared in Fig. 5 and Fig. 6.

$[t_0 \sim t_1]$: Before t_0, $i_{Lr}(t)$ is negative. At t_0, transistor S_1 is turned on with ZVS operation. The transistor S_1 and diodes $D_{2,4}$ will conduct the resonant current as in Fig. 6(a).

$[t_1 \sim t_2]$: At t_1, $i_{Lr}(t)$ resonates to zero. The $i_{D2,D4}(t)$

decreases to zero, so diodes $D_{2,4}$ are turned off with ZCS operation. Meantime, $V_{c1}(t)$ reaches the maximum value V_{cr_max}, while $V_{c2}(t)$ reaches the minimum value V_{cr_min}.

Afterwards, $i_{Lr}(t)$ is positive and transistor S_1 and diodes $D_{1,3}$ will conduct the resonant current as in Fig. 6(b).

[t_2~t_3]: At t_2, transistor S_1 is turned off. Since the $i_{Lr}(t)$ is positive, the internal anti-parallel diode of S_2 starts conducting current, shown in Fig. 6(c).

[t_3~t_4]: At t_3, transistor S_2 is turned on with ZVS operation. The loop current starts conducting through the transistor channel. At t_4, $i_{Lr}(t)$ resonates to zero. Diodes $D_{1,3}$ are turned off with ZCS operation. Meantime, $V_{c1}(t)$ reaches the minimum value V_{cr_min}, while $V_{c2}(t)$ reaches the maximum value V_{cr_max}. After t4, the following half exchanging cycle begins and the activity standard is comparable. In light of the above investigation, the transistors are ZVS turned on and diodes are ZCS killed by working over the reverberation.

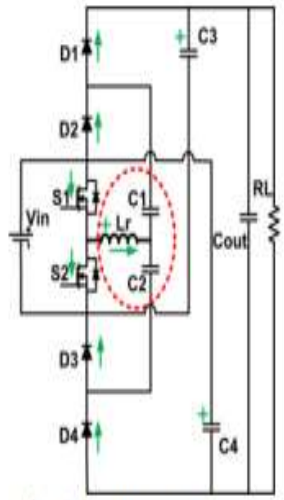


Fig. 4. 3X Resonant AIDSCC

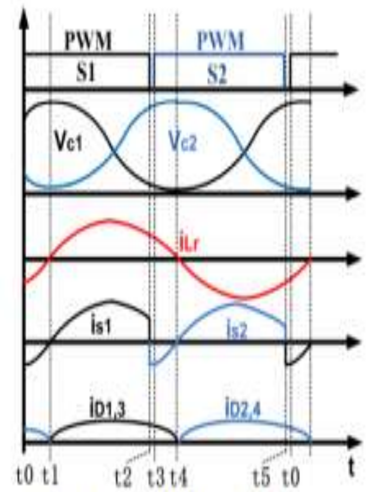
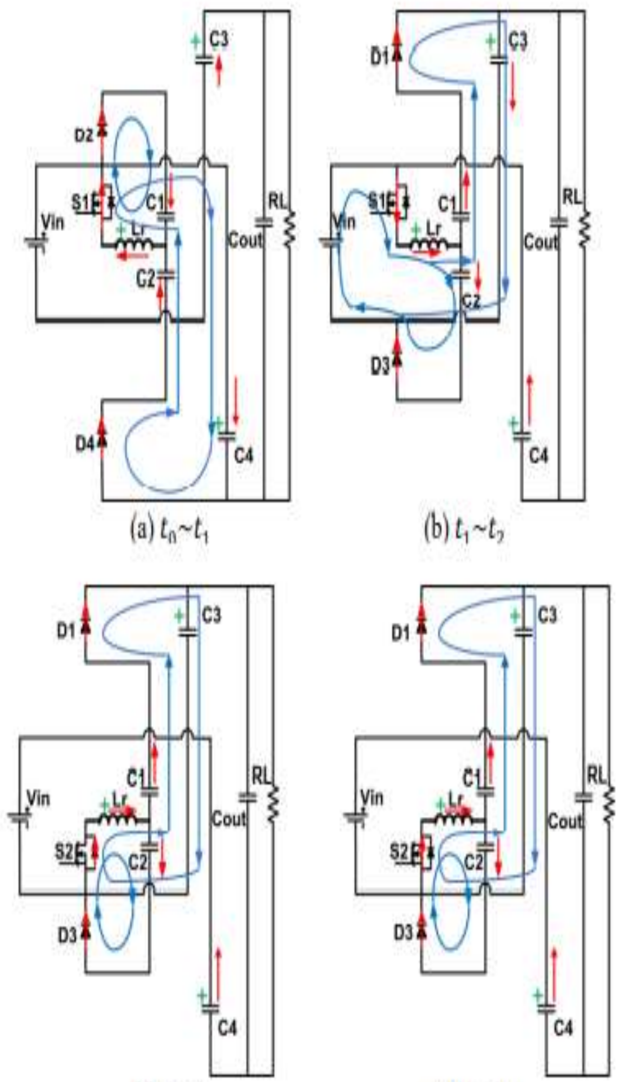


Fig. 5. Operating Waveforms



(a) t_0~t_1 (b) t_1~t_2

(c) t_2~t_3 (d) t_3~t_4

Fig. 6. Switching States of 3X Resonant AIDSCC

IV. HARDWARE MODEL

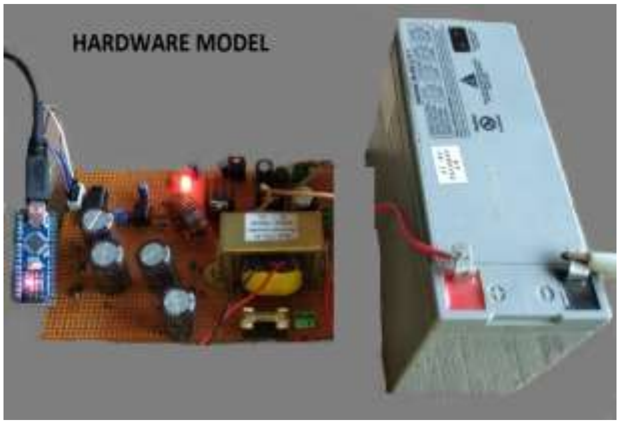
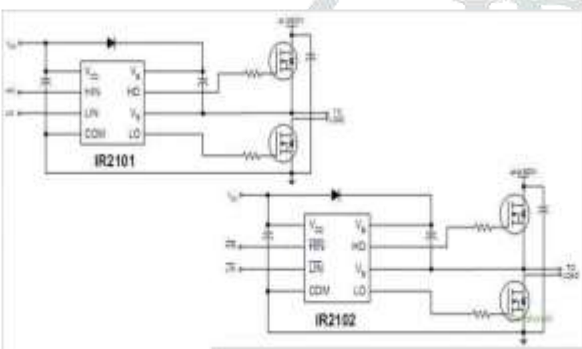


Fig.7 Hardware Prototype

HARDWARE DESCRIPTION

Driver IC configuration is as shown below



Driver circuit consists of two IC's IR2101 and IR2102 Is a 8 pin configuration having Vcc &Vs as supply lines and a common pin along with two pins for high input side and two pins for low output side.

RECHARGEABLE BATTERY (7AH,12V)

During charging, the high-quality energetic cloth is oxidized, producing electrons, and the poor fabric is reduced, ingesting electrons. These electrons constitute the current glide in the external circuit. The electrolyte may serve as a easy buffer for inner ion flow between the electrodes, as in lithium-ion and nickel-cadmium cells, or it is able to be an active player inside the electrochemical response, as in lead–acid cells.

The energy used to price rechargeable batteries typically comes from a battery charger the use of AC mains strength, despite the fact that a few are prepared to apply a vehicle's 12-volt DC electricity outlet. The voltage of the supply have to be better than that of the battery to pressure contemporary to circulate it, but not an excessive amount of higher or the battery may be broken.

Chargers take from a few minutes to numerous hours to price a battery. Slow "dumb" chargers without voltage or temperature-sensing skills will fee at a low charge, commonly taking 14 hours or greater to reach a full rate. Rapid chargers can commonly price cells in two to five hours, relying on the version, with the quickest taking as low as fifteen minutes. Fast chargers need to have more than one methods of detecting when a cell reaches full fee (exchange in terminal voltage, temperature, etc.) to stop charging before harmful overcharging or overheating takes place. The fastest chargers frequently incorporate cooling enthusiasts to maintain the cells from overheating. Battery packs intended for fast charging may encompass a temperature sensor that the charger uses to protect the %; the sensor may have one or greater additional electric contacts.

ARDUINO NANO

The Arduino Nano has a number of centers for communicating with a laptop, another Arduino, or other microcontrollers. The ATmega328 provide UART TTL (5V) serial conversation, that is to be had on digital pins zero (RX) and 1 (TX). An FTDI FT232RL on the board channels this serial verbal exchange over USB and the FTDI drivers (included with the Arduino software program) offer a virtual com port to software on the computer. The Arduino software program includes a serial display which allows simple textual information to be despatched to and from the Arduino board. The RX and TX LEDs on the board will flash whilst records is being transmitted thru the FTDI chip and USB connection to the pc (but now not for serial verbal exchange on pins zero and 1). A SoftwareSerial library lets in for serial conversation on any of the Nano's digital pins. The ATmega328 additionally support I2C (TWI) and SPI conversation. The Arduino software program consists of a Wire library to simplify use of the I2C bus.

BUFFER IC (CD4050 BE)

The CD4050 hex buffers are monolithic complementary MOS (CMOS) integrated circuits built with N- and P-channel enhancement mode transistors. These devices function good judgment level conversion the use of only one deliver voltage (VDD). The enter signal high level (VIH) can exceed the VDD supply voltage while those devices are used for common sense degree conversions. These gadgets are meant for use as hex buffers, CMOS to DTL/ TTL converters, or as CMOS current drivers, and at VDD = 5.0V, they can force at once two DTL/TTL masses over the total running temperature variety.

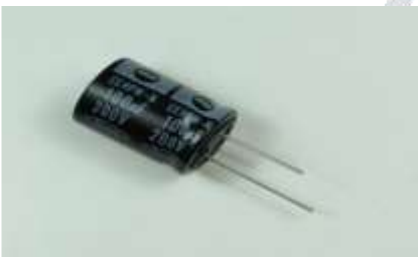
Features:

Wide supply voltage range: 3.0V to 15V.
Direct drive to 2 TTL hundreds at 5.0V over full temperature variety.
High source and sink cutting-edge capability.
Special input safety allows input voltages more than VDD.

Applications:

1. CMOS hex inverter/buffer.
2. CMOS to DTL/TTL hex converter.
3. CMOS current "sink" or "source" motive force.
4. CMOS HIGH-to-LOW logic stage converter.

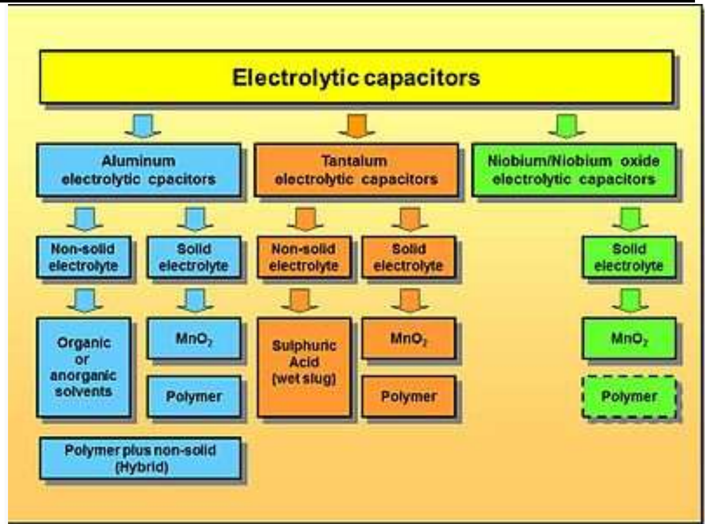
CAPACITORS



An electrolytic capacitor is a polarized capacitor whose anode or fine plate is fabricated from a metallic that forms an insulating oxide layer thru anodization. This oxide layer acts because the dielectric of the capacitor. A strong, liquid, or gel electrolyte covers the floor of this oxide layer, serving because the cathode or negative plate of the capacitor. Due to their very thin dielectric oxide layer and enlarged anode floor, electrolytic capacitors have a far higher capacitance-voltage (CV) product according to unit quantity than ceramic capacitors or movie capacitors, and so may have huge capacitance values. There are 3 households of electrolytic capacitor: aluminum electrolytic capacitors, tantalum electrolytic capacitors, and niobium electrolytic capacitors.

ELECTROLITIC CAPACITOR FAMILY TREE

As to the basic creation ideas of electrolytic capacitors, there are 3 different sorts: aluminum, tantalum, and niobium capacitors. Each of these three capacitor families uses non-solid and strong manganese dioxide or stable polymer electrolytes, so a top notch unfold of various combinations of anode fabric and stable or non-stable electrolytes is available.



The first industrially realized electrolytic capacitors consisted of a metallic container used as the cathode. It become filled with a borax electrolyte dissolved in water, in which a folded aluminum anode plate became inserted. Applying a DC voltage from out of doors, an oxide layer became fashioned on the surface of the anode. The benefit of these capacitors become that they had been notably smaller and inexpensive than all other capacitors right now relative to the realized capacitance fee. This creation with unique types of anode creation but with a case as cathode and container for the electrolyte became used as much as the Nineteen Thirties and become referred to as a "moist" electrolytic capacitor, within the experience of its having a excessive water content material.

The first greater commonplace software of moist aluminum electrolytic capacitors was in large smartphone exchanges, to lessen relay hash (noise) on the forty eight volt DC electricity deliver. The development of AC-operated domestic radio receivers in the late Nineteen Twenties created a demand for huge-capacitance (for the time) and excessive-voltage capacitors for the valve amplifier method, generally at least four microfarads and rated at around 500 volts DC. Waxed paper and oiled silk film capacitors have been available, but gadgets with that order of capacitance and voltage score have been cumbersome and prohibitively luxurious.

The electrical traits of electrolytic capacitors depend upon the shape of the anode and the electrolyte used. This influences the capacitance price of electrolytic capacitors, which relies upon on measuring frequency and temperature. Electrolytic capacitors with non-stable electrolytes show a broader aberration over frequency and temperature tiers than do capacitors with solid electrolytes.

The simple unit of an electrolytic capacitor's capacitance is the microfarad (μF). The capacitance price exact inside the information sheets of the producers is called the rated capacitance CR or nominal capacitance CN and is the price for which the capacitor has been designed.

The standardized measuring situation for e-caps is an AC measuring technique with 0.Five V at a frequency of 100/one hundred twenty Hz and a temperature of 20 °C. For tantalum capacitors a DC bias voltage of one.1 to 1.Five V for sorts with a rated voltage ≤2.5 V, or 2.1 to two.Five V for types with a rated voltage of >2.5 V, may be carried out at some stage in the size to avoid opposite voltage.

The capacitance fee measured at the frequency of one kHz is set 10% much less than the 100/one hundred twenty Hz cost. Therefore, the capacitance values of electrolytic capacitors are not directly comparable and differ from the ones of movie capacitors or ceramic capacitors, whose capacitance is measured at 1 kHz or better.

Measured with an AC measuring method with one hundred/120 Hz the capacitance value is the nearest price to the electrical fee saved inside the e-caps. The saved rate is measured with a special discharge approach and is called the DC capacitance. The DC capacitance is set 10% higher than the one hundred/a hundred and twenty Hz AC capacitance. The DC capacitance is of interest for discharge packages like photoflash.

The percentage of allowed deviation of the measured capacitance from the rated cost is known as the capacitance tolerance. Electrolytic capacitors are to be had in different tolerance series, whose values are special in the E series laid out in IEC 60063. For abbreviated marking in tight areas, a letter code for each tolerance is specified in IEC 60062.

V. SOFTWARE DESIGN AND EXPERIMENTAL RESULTS

A. Software Design without motor

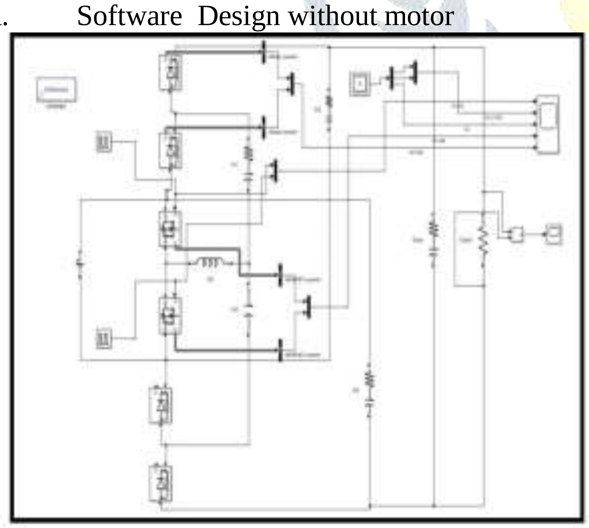


Fig.8 Simulation circuit

A unregulated 3X AIDSCC is designed using MATLAB software that is 2017b version is applied to obtain software output. 3X AIDSCC circuit with output power 140W and input voltage 50V is designed. The VS of $S_{1,2}$, $D_{1,2,3,4}$ and $C_{1,2}$ is given 50V.And also the VS of $C_{3,4}$ is of 100V which is working as capacitor banks. The value of capacitors $C_{1,2,3,4}$ is large enough at $40\mu F$. Ideal conversion ratio of the circuit is 3, so ideal output voltage is about 150V hence the minimum load is $R_L = 160\Omega$ .The circuit consists of two MOSFET IR2101 and turned ON one at a time .The Mosfet is given pulse from drive circuit and capacitor is charged through diodes connected to Mosfet .Capacitor is used for coupling voltage a input of 50V DC is given and ouput of 100V is obtained.

B. Experimental Results

The trial waveforms of 3X AIDSCC are appeared in Figure, where the exchanging recurrence is $f_s = 30kHz$ the heap is estimated to be $R_L = 323.9\Omega$. From Fig 8, the information current wave is 5% when the heap current is 0.45A with the assistance of the programmed interleaved arrangement and an information capacitor channel (100uF). In Fig.8, the information voltage is fixed at 50V and the yield voltage is 146.5V, so the voltage gain is 2.93. The voltage is 98.3V, which is lower than the normal worth 100V. The loss of the voltage gain and is because of the voltage drop on the transistors and diodes.

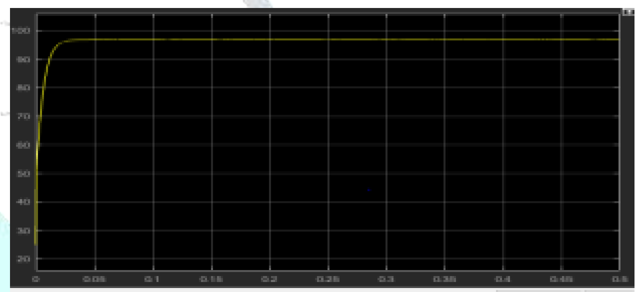


Fig 9 waveform of output voltage across load

The characteristic waveforms for the above simulated circuit is shown .The waveforms includes switching current and voltage diode current, inductor and capacitor current .

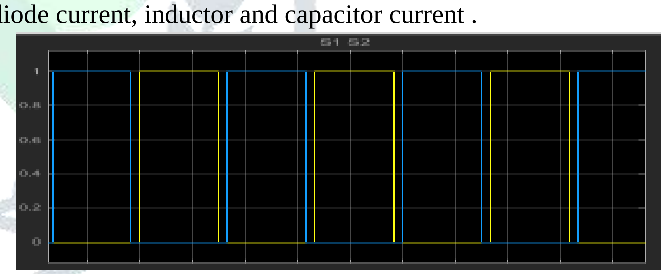


Fig 10 waveform of Gate voltage of S1 and S2

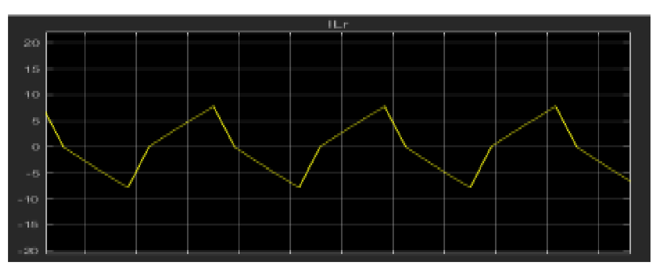


Fig 11 waveform of resonant inductor current

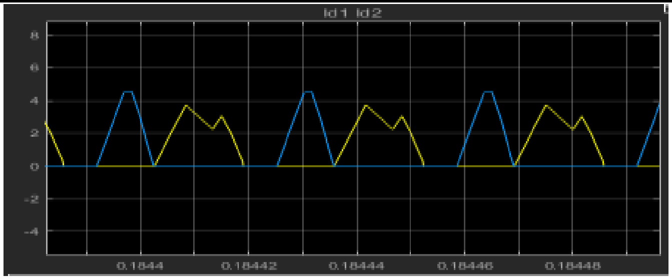


Fig 12 waveform of diode current at d1 and d2

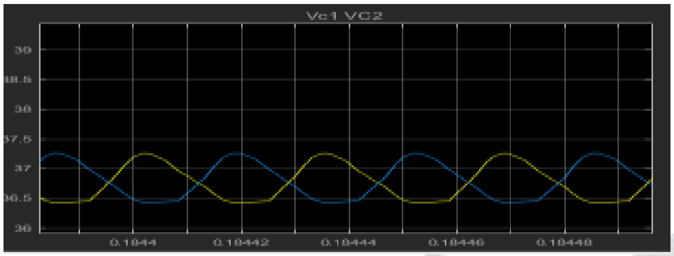


Fig 13 waveform of capacitor voltage at C1 and C2

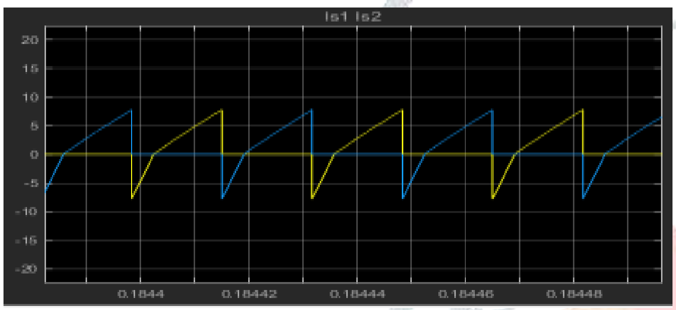


Fig 14 Input ripple current at S1 and S2

C. Software design with permanent magnet motor

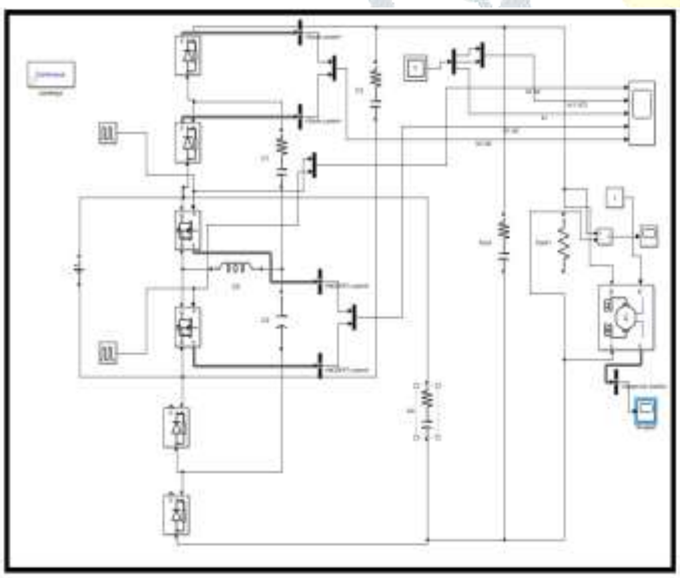


Fig.15 design of permanent magnet motor

The above circuit shows permanent magnet motor connected to RL load . And parameters used in circuit is similar to AIDSCC the speed of motor is 25 rad/sec. Speed is measured in radians per second which is obtained at load. The output characteristics of circuit is as shown below. The circuit uses two MOSFET where one switch is operated at a time the input of 50V is applied and output is obtained as motor speed.

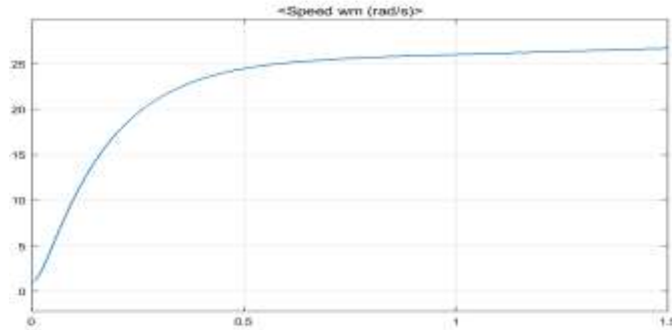


Fig 16 waveform of speed of permanent magnet motor

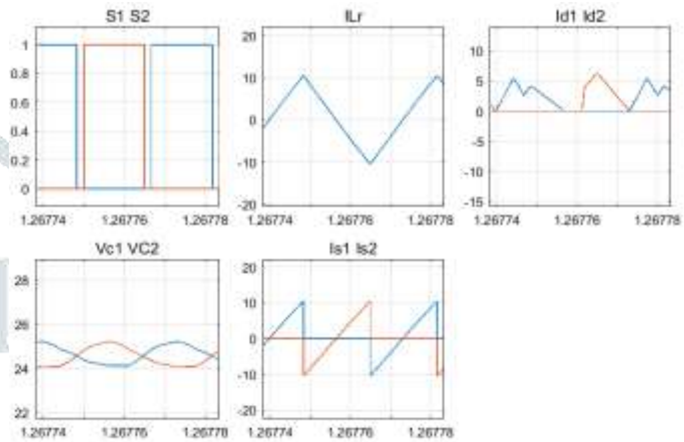


Fig 17 characteristics waveform of permanent magnet motor

VI .CONCLUSION

In this paper, a group of AIDSCC is proposed by reflecting the customary Dickson SCC and evacuating the excess transistors. The trial consequences of a 3X AIDSCC show that its information current wave is well beneath 10% because of the programmed interleaved design. What's more, the pinnacle capacitor voltage stress is lower than the conventional Dickson SCC if N>3. The pinnacle productivity is 98% at 66W. In any case, the variety scope of the voltage gain is lower than 10% regardless of whether the converter works at 1kHz. To improve the line guideline ability of AIDSCC, a little inductor is included and two 40uF capacitors are supplanted by two 0.1uF thunderous capacitors, framing the group of Resonant AIDSCC. The transistors are turned on with ZVS activity the diodes are killed with ZCS activity if the exchanging recurrence is over the full.

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