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VLSI Architecture of Polar Encoding and Decoding for Next Generation 5G-IOT Applications

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Abstract : 5G is designed for high reliability and low latency massive data interaction scenarios. Compared with 4G mobile communication, it puts forward higher requirements for channel decoding. The VLSI encoding and decoding techniques are currently use in many of the digital signal processing applications. Many of the research is going on the enhancement of the encoding and decoding techniques, which can meet the requirement of the 5G. The artificial intelligence based applications work under the 5G constraints. Polar code is one of the emerging encoding and decoding approach, which can be used in the FPGA, based AI-IOT applications. This paper proposed the VLSI architecture of polar encoder-decoder. The simulation is performed on the Xilinx ISE 14.7 software with verilog coding.

IndexTerms **- VLSI, FPGA, IOT, 5G, AI, Xilinx ISE, Polar Code.**

I. INTRODUCTION

Polar codes are a class of codes versatile enough to achieve the Shannon bound in a large array of source and channel coding problems. For that reason it is important to have efficient implementation architectures for polar codes in hardware. Polar codes have attracted increasing attention recently due to its low encoding and decoding complexity. Hardware optimization can further improve their implementations to enable real-time applications on resource-constrained devices. There are many complexities inherent in adopting 5G networks, and one way the industry is addressing those complexities is by integrating artificial intelligence into networks. When Ericsson surveyed decision-makers from 132 worldwide cellular companies, over 50% said they expected to integrate AI into their 5G networks by the end of 2022. The primary focus of AI integration is reducing capital expenditures, optimizing network performance, and building new revenue streams. 55% of decision-makers stated that AI is already being used to improve customer service and enhance customer experience by improving network quality and offering personalized services. 70% believe that using AI in network planning is the best method for recouping the investments made on switching networks to 5G. 64% of survey respondents will focus their AI efforts on network performance management. Other areas where cellular decision-makers intend to focus AI investments include managing SLAs, product life cycles, networks, and revenue.

There are challenges associated with integrating AI into 5G networks, of course. Effective mechanisms for collecting, structuring, and analyzing the enormous volumes of data amassed by AI must be developed. For that reason, early AI adopters who find solutions to these challenges will emerge as the clear frontrunners as 5G networks become connected.

While 5G is up to 20 times faster than 4G, it offers more than just faster speeds. Due to its low latency, 5G speeds will allow developers to create applications that take full advantage of improved response times, including near real-time video transmission for sporting events or security purposes. Additionally, 5G connectivity will allow more access to real-time data from various solutions. 5G leverages Internet of Things (IoT) sensors that last for years, requiring far less power for operation. This could allow remote detection of farming irrigation levels and equipment condition changes in factories. Doctors could securely access patient data more easily. All these opportunities will require the use of AI to make them functional.

II. METHODOLOGY

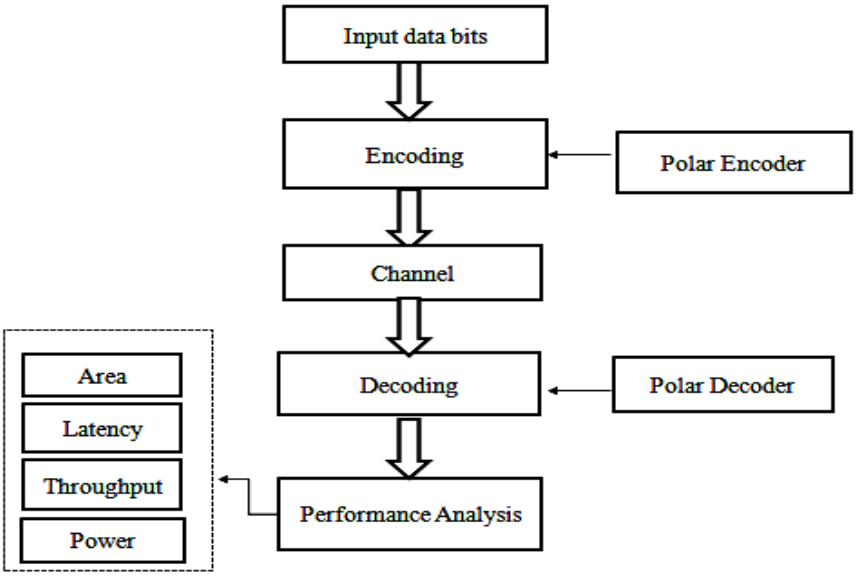

Figure 1: Flow Chart

Polar code as a high-performance error correction code technology, its huge application potential has also cause a strong concern among 5G standardization of communications research and development institutions and academic word. In the case of channel combining and channel separation, channel polarization occurs. The focus of channel coding research may be stated quite simply: develop high performance channel codes that mitigate the effect of the errors in a communication link (bit-error-rate is the common performance measure used here). However, the real challenge here is doing this in a manner of sufficiently low complexity that allows practical implementation into the silicon technology of the day. The complexity of a code determines everything, e.g. how much power it consumes, how much memory it needs, how much computation power it requires, and how much latency it incurs, all of which at the end of the day determine whether a code is good for any particular use case.

Step-1: Assign input bits into polar encoder and it give encoder output.

Step-2: Encoder output applies in channel and it generates decoder input.

Step-3: This input applies in decoder and it generates decoder output, this is same as assigned input.

Step-4: Now check all results in test bench and calculate all parameters.

The concept of channels polarization transform N independent channels into polarized channels by channels combining and splitting, a set of more reliable and a set of less reliable channels can be observed .Than, the K most reliable channels are now used to transmit information bits, while the other N-K bit-channels are frozen, which are set to zero .For a given code rate R=K/N,the K information bits are mapped into the K non-frozen position of uN, all other position are frozen. The encoding process (polar transformation) can be simply described by a generator matrix G=Fn. And FN denotes the nth power of F=[10/11].

III. SIMULATION AND RESULTS

The proposed polar code is implemented and simulated by using the Xilinx ISE 14.7 software, The Isim simulator is used to check the results validity in test bench.

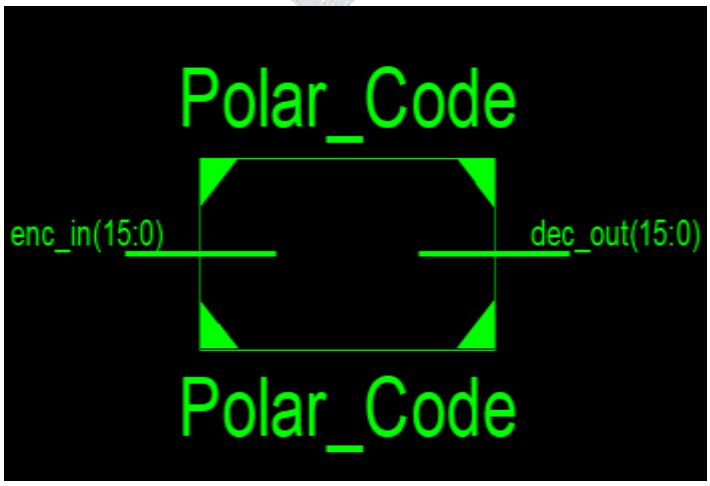

Figure 2: Top view of polar code

Figure 2 is showing the top view of the proposed code, which includes the polar encoder, decoder and channel.

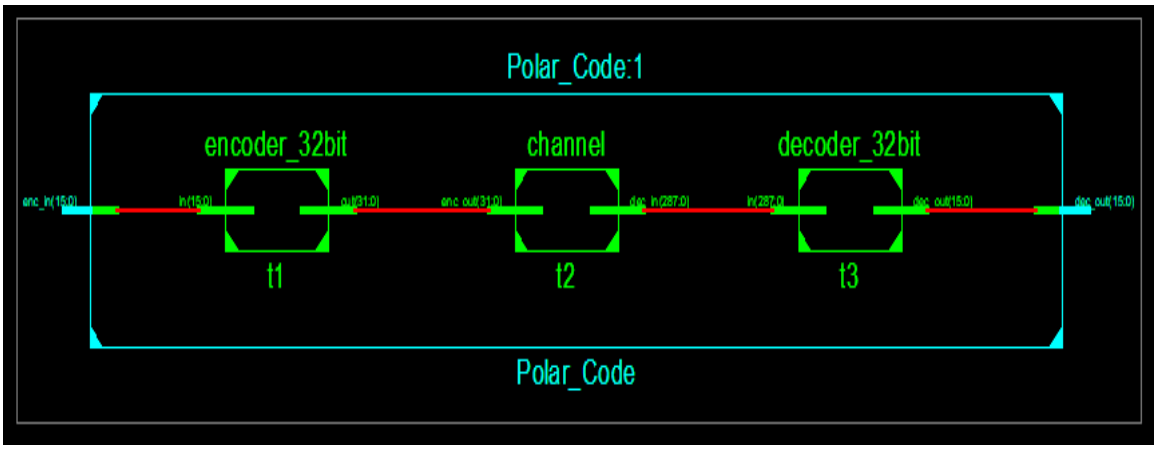

Figure 3: Polar code steps

Polar Encoder- In this step, provides the 16 bit input data bits and it converts into the 32 data bits.

Polar Channel- the 32 bit polar encoder output gives in the channel and here it converts into the 288 bits.

Polar Decoder- In this step the channel output gives in the polar decoder and it converts into the 16 data bits.

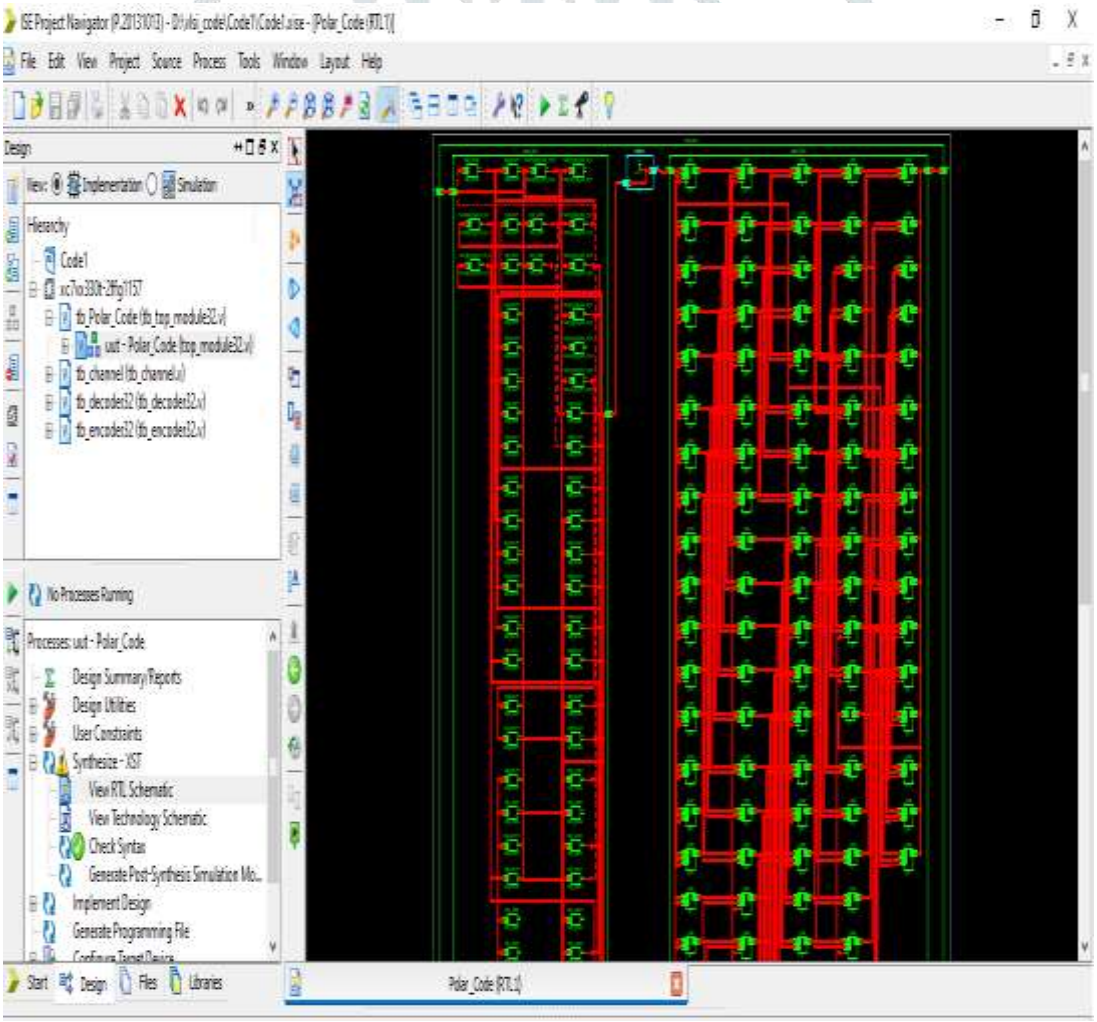

Figure 4: RTL view of proposed model

Figure 4 showing register transfer level diagram which contain all blocks and wires.

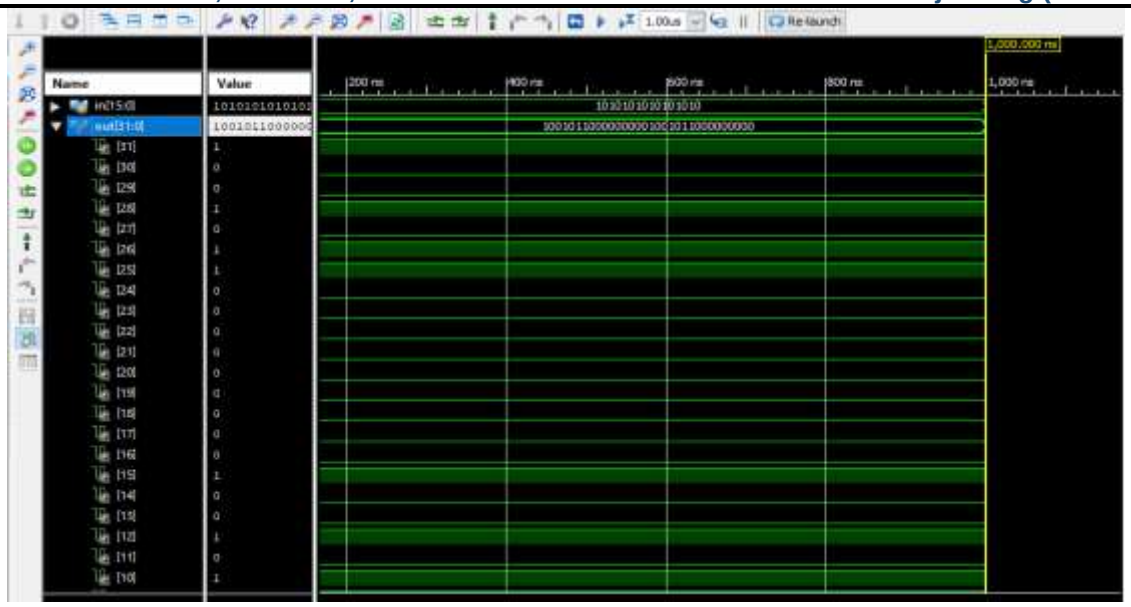

Figure 5: Test bench encoder output waveform

Figure 5 is showing the test bench results. Here the 16 bit input data bits is 1100110011001100 and the data bit is retrieve in the output of the decoder side that is same as input side of the encoder.

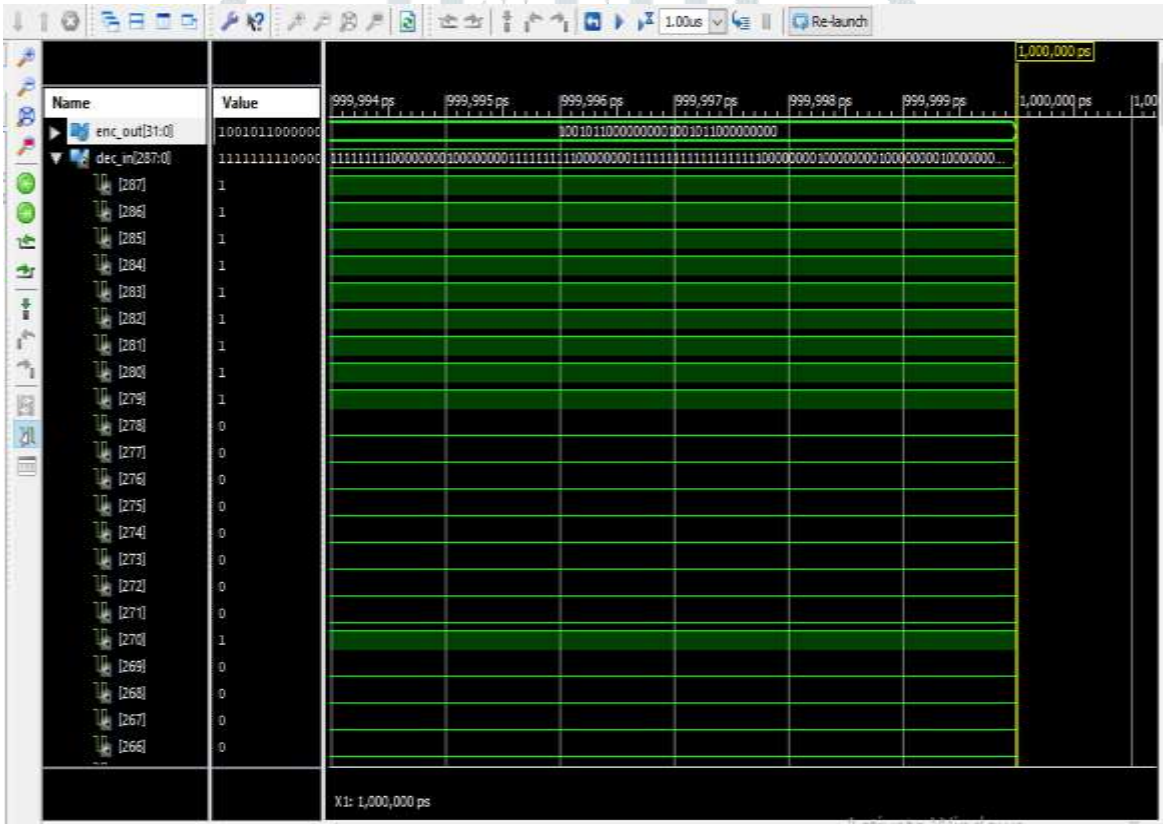

Figure 6: Test bench channel output waveform

Figure 6 showing channel result in test bench, here apply 32 bit encoder output that is 10010110000000001001011000000000. It generates 288 decoder input bit that is hff80403ff00ffffe01008040201008040201ff80403ff00ffffe01008040201008040201 in hexa decimal.

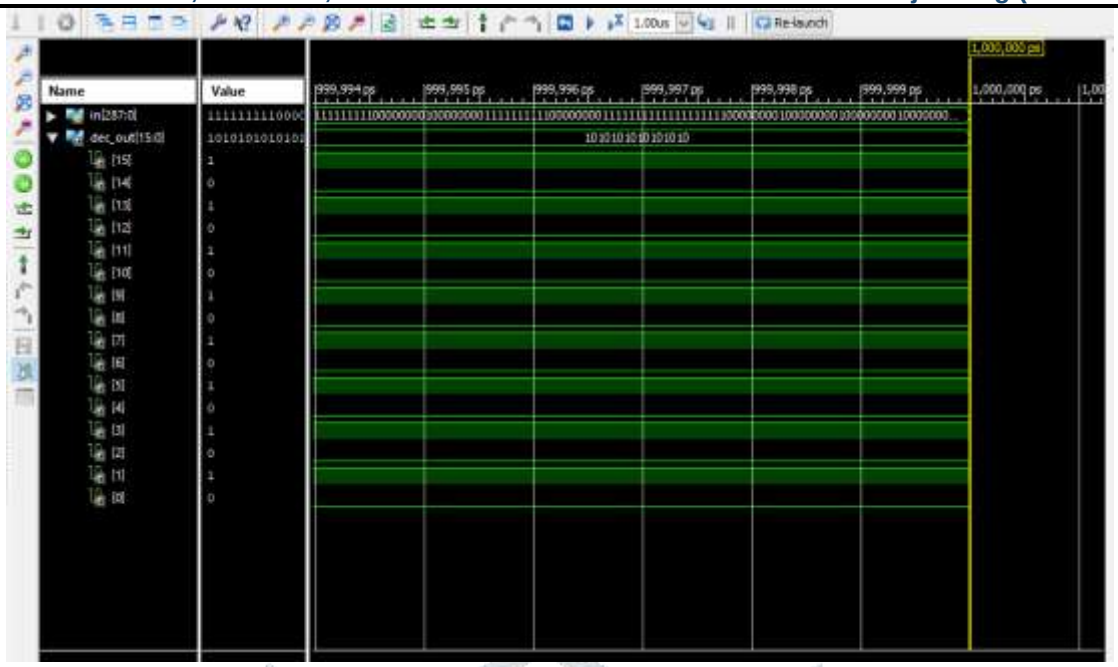

Figure 7: Test bench decoder output waveform

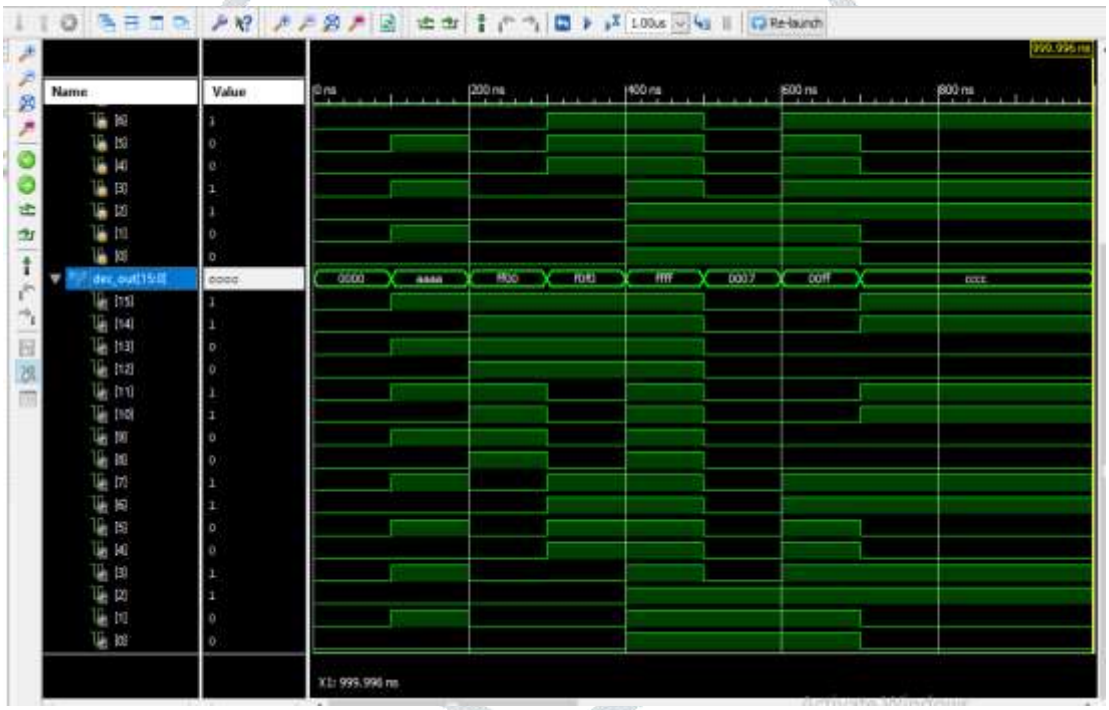

Figure 8: Test bench Result in hexadecimal complete waveform

Figure 8 is showing the various results value in the Xilinx test bench. The input of encoder and output of decoder is the 'cccc' in the form of hexadecimal.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	2107	204000	1%
Number of fully used LUT-FF pairs	0	2107	0%
Number of bonded IOBs	32	600	5%

Figure 9: Device utilization of proposed model

Table 1: Comparison of simulation results

Sr No.	Parameter	Previous Work [1]	Proposed Work
1	Method	Polar Decoder	Polar Encoder & Decoder
2	Area	2.189 mm^2	2 mm^2
3	Delay	99.94 ns	80.67 ns
4	Power	193.5 mW	125 mW
5	Throughput	11.9 Gbps	12.4 Gbps

IV. CONCLUSION

Polar codes have attracted increasing attention recently due to its low encoding and decoding complexity. This paper proposed the FPGA implementation of polar encoder-decoder for 5G artificial intelligence applications. The total number of component or area is 2 mm^2, while previous it is 2.189 mm^2. The delay or latency is achieved 80.67ns while previous it is 99.94 ns the overall throughput is 12.4 Gbps while previous it is 11.9 Gbps. Therefore the simulation results show that the proposed polar code gives the significant better results than previous work.

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