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Low cost Probability Density Function Estimator Architecture for Image Histogram

[1]Koteswar Rao Bonagiri,[1]Giri Babu Kande,[2] P.Chandrasekhar Reddy[3]

[1]Research Scholar, [2]Professor & Dean,[3]Professor
[1]Dept. of ECE,
[1]JNTU Hyderabad, Hyderabad, India

Abstract : Estimation of Probability Density Functions (PDFs) in view of accessible information is critical issue emerging in various fields such as broadcast communications, machine learning, information mining, design pattern recognition and Personal Computer (PC) vision. In this paper, Low- Cost PDF (LC-PDF) method is introduced for "Histogram Estimation". The Carry Select Adder (CSLA) employs in the Bin architecture for additional process. The Look-Up Table (LUT) using in priority encoder for storage purpose, which increases the system performance. The LC-PDF design is verified in Modelism by using Verilog code. The FPGA implementation is done by using Xilinx tool for two different type of devices such as Virtex-6 and Virtex-6 LP. The FPGA analysis, LUT, slices, and flip-flops. And the ASIC implementation is done by using 180nm and 45nm technology, which analysis area, power, delay, Area Power Product (APP), Area Delay Product (ADP) are improved in the LC-PDF method compared to conventional method.

IndexTerms **- Carry select adder, histogram equalization, look-up table, area power product, and area delay product.**

I. INTRODUCTION

The PDF is a basic concept in the statistic processes. A statistical measure of data can be categorized into two types such as 1. An understanding features and shape of data over the density function. 2. An estimation of one function over the joint density function. The PDFs estimation is building of predict density function from observed data points, which is based on obtainable data that is an important issue arising in different fields like telecommunications, data mining, machine learning, computer version, pattern recognition and so on [1]. The PDFs estimation of a random variable can be estimated by employing different techniques like Parametric, Non- parametric or Semi- parametric techniques. The parametric techniques are utilized to fit the data to an identified model and reduce the value of parameters. This parameter employed to statistics from the model's equations. But this technique experimental result is very poor accuracy. The Semi- parametric techniques are used for all kinds of density functions, which gives the high accurate outcomes within low data [2]. The Non- parametric techniques are classified into two methods such as Histogram and Kernel methods. The density function can be estimated by using a histogram of the sample data that requires several numbers of samples for a smooth curve. This PDF method can provide a smoother curve from few data samples [3], [4], [5]. Commonly, most of the Stochastic Control Design (SCD) techniques focused on a control output of mean and variance of Stochastic System. There are 2-types of PDF control strategies have been used for stochastic systems. The first type of Stochastic Systems has created turning to the PDF control function that is general and practical in the Joint PDF (JPDF) shape control.

The second type of stochastic systems strategies is related to the JPDFs are immeasurable. The JPDFs of the outcomes were formulated recursively by using system function. But its accuracy of the closed-loop control is more difficult to be assured for the stochastic system below the modeling errors [6] [7]. The PDFs are offered for the asymmetric non-Gaussian distribution of the drain current. This distribution, the drain current at the non-Gaussian high – sigma tail can be predicted by median and variance removed from statistical information of a small group of samples, this method is not suitable for a large arrangement of samples [8],[9]. Parametric Maximum Likelihood (PML) estimators are employed for the PDFs because it is an efficient computing process in various static fields such as fast convergence rate, asymptotic normality and so on. But these estimators are not given appropriate results in the statistics processes [10]. To conquer this problem, the LC-PDF method is implemented for histogram estimation. In the LC-PDF method, the image is read in Matlab tool. Here, the image converts into pixel format, and the pixel converts into text format. Furthermore, the MATLAB output gives into Verilog. The LC- PDF structure design is implemented in Modelsim by using Verilog code. Finally, the Verilog output is givenin Matlab. The histogram output is taken from the Matlab tool. In ASIC implementation, area, power, and delay, APP, ADP are mitigated in the LC-PDF method. In FPGA implementation, LUT, slices, and flip-flops are improved in the LC- PDF method compared to the existing method.

This paper is composed as follows. In section-II, described some previous related work. In Section-III, shows LC - PDF design architecture. In Section-IV, mentioned experimental setup and results and discussion. The conclusion is made in Section -V.

II. RELATED WORK

HubinRuanet al, [11] implemented FPGA based design to accelerate the evaluation of the Gaussian Copula- PDF (GC-PDF). Generally, the computation of the GC-PDFs was mapped into a fully pipelined FPGA data flow mechanism by employing three optimization stages such as transforming the computation pattern, extending computation to multiple pipelines, neglecting constant computation from hardware logic. In this method, increased the system speed but that cost of the system is more expensive.

Suhaib A. Fahmy [12] proposed the heterogeneous resources based on new FPGAs are enable to the real-time evaluation of PDFs of sampled information or data at speeds of over 200 M samples/ second. In this work, a flexible architecture was employed to extract statistical data in the real-time as saving a moderate amount of area, which allows it to be incorporated into conventional FPGA applications.

Komatyet.al [13] have introduced a signal filtering, the noise removal is most important part of instrumentation and measurement in signal domains. Where is to preserve the significant structures of the signals as well as removing noise. Hence, a noise signal is adaptively broken down into oscillatory elements are called as Intrinsic Mode Function (IMF), which is used as an estimation of the PDF of every extracted mode. This method was cannot fully remove noise from the original signal.

KarthikNagarajanet al, [14] illustrated design and analysis of a multi-core PDF estimation algorithm on FPGAs. In this work, analysis and implement a PDF estimation algorithm by employing kernel based FPGA. The calculated PDF values were read and verified in the MATLAB and error statistics in the solution was computed. A maximum error percentage was 3.8%. This method is detected low amount of error.

This all related works contains mainly two more problems in the PDF - histogram method such as more area, and power consumption. To solve these issues, the LC- PDF method is implemented to increase the ASIC and FPGA implementation results.

III. LC-PDF METHODOLOGY

In this paper, the LC-PDF is implemented by using Matlab and Modelsim tool. The input image has been read in the Matlab. The input image converts into pixel format in the Matlab, and the pixel converts into text format which gives into the input of the Modelsim tool (Verilog Code). In the fig.1 shows the LC- PDF architecture design, which consists of mainly using five important structure designs are employed in the LC- PDF architecture such as First-in-First-out (FIFO), Access pattern memory, Bin structure, Comparator, and Priority Encoder (PE). The LC- PDF architecture is following below functions,

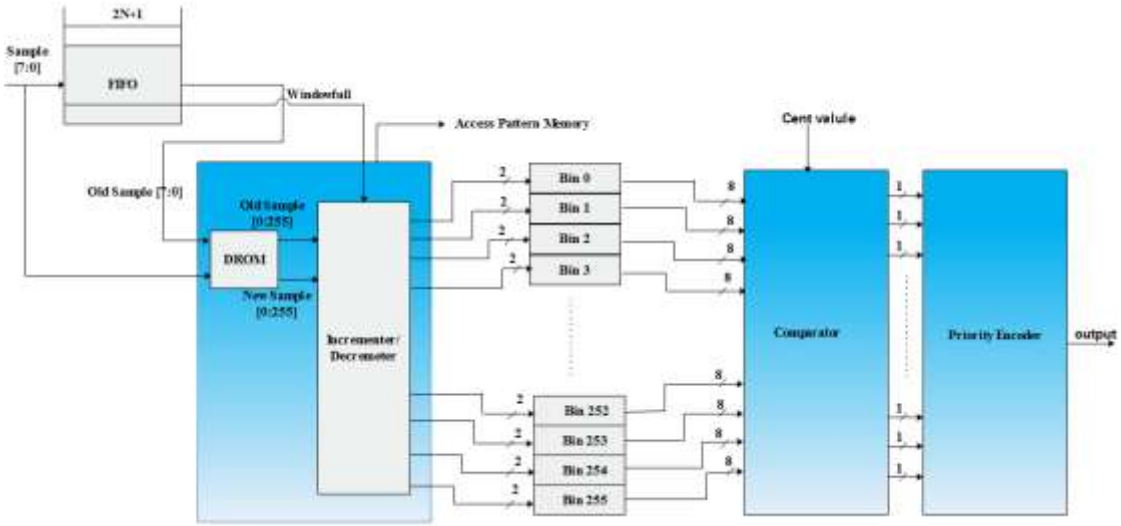

Figure.1. Block diagram of the LC-PDF architecture

This allows extracting different PDF statistics in a highly efficient method. Maintaining the entire histogram within the architecture has the advantage of allowing the designer to extract several statistics of interest, as needed for a specific application.

3.1FIFO Structure

The Matlab output of text format is given into the FIFO structure. The FIFO buffer of the length equal to the window is instantiated, this buffer keeps track of the samples in the window. Initially, a FIFO buffer is employed to store the samples for the window. The input samples enter the system and fed into the FIFO. Hence, the output position can be set by the FIFO_length signal, the permitting the window size to be different at the runtime. The FIFO is constructed, which can be set to any useful power of 2. When a new sample is received FIFO and window is full, at the time the oldest samples are removed from the FIFO. The histogram needs all bins corresponding to the access pattern used for the old sample to be decremented. When, the bins corresponding to the new input sample should be increased. This can all be implemented in one cycle, by simply leaving any bins are contained in both sets unchanged, since increment/decrement at the same time. The bins are only enabled by the access pattern of the new sample are incremented, whereas bins enabled only by the access pattern of the removed sample are decremented. The output of the FIFO denotes the old sample developing from the sample window. Furthermore, the new samples are collected, which used to address the access pattern memory. The output of this memory expresses of every bin counters to increase, decrease or maintain the existing value and to update the histogram standards. The count output of all the bins (Bin count [0: N-1]) is passed to the next stage, where statistics can be extracted. Hence, the PDF permits for more interesting statistics to be extracted in the real-time system.

3.2Access Pattern Memory

The access pattern memory contains Dual-port Read Only Memory (DROM), and Incrementer/Decrementer operation shown in figure 2. The access patterns have been stored in the ROM that correct bins are enabled employed for any given input sample. Next, these can be processed to determine which bins are incremented/decremented, it is shown in the figure .3.

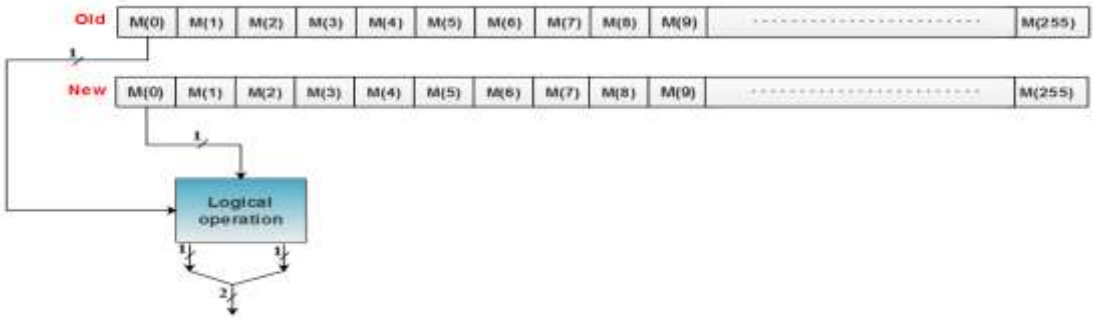

Figure.2. Block diagram of the Incrementer/Decrementer operation.

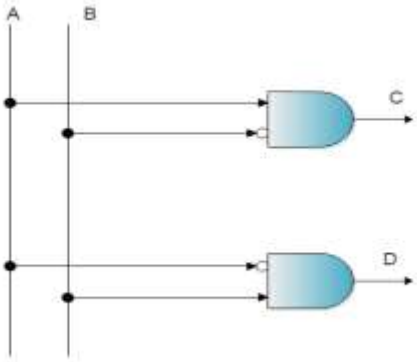

Figure.3.Logical Operation of the in Incrementer/Decrementer process

In DROM module, the 8-bit new sample and 8-bit old sample data are stored in DROM, the main advantage of this method the old and new samples are stored in single DROM. Because of not required two or more ROM. Each and every memory (M) like M [0], M [1], up-to M [255] can be stored in 256-bits. This DROM output of 0 to 255-bits new and old samples are given into Incrementer/Decrementer.

In the figure.3 shows the block diagram of the Incrementer/Decrementer process. Here, old sample 0 to 255 bits and new sample 0 to 255 bits arestored in separate memory space. In the Incrementer/Decrementer operation, 1-bit old sample and 1- bit new sample are given into input the logical circuit, which is shown in the figure.3. For example, the A (1-bit) old sample and B (1-bit) new sample for logical operation is done by using AND logic circuit, which provides two-bit output like C and D. This output is given to the input of the Bin structure, which is described follows by below section.

3.3Bin Structure

This simple logic format must be illustrated used for each and every bin, which is shown in the figure. 4. Two-bit selection has been given to the MUX, initially the one is stored in the register, which gives increment and decrement operation. In this section, the CSLA used for the addition operation. If the selection line is 00 the MUX output is 1, selection line is 01 the MUX output is 2, and selection line is 10 the MUX output is 0, which stored in the register. Finally, the bin structure provides 8-bit output. The 8-bit bin counter output is given to the input of the comparator.

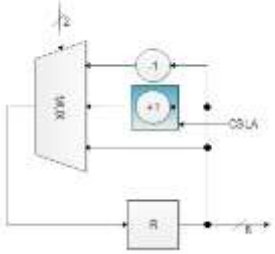

Figure.4. Block diagram of the bin architecture

3.3.1CSLA Design

The CSLA designs using in the Bin structure for bit addition process, which is shown in figure.5. The CSLA can achieve fast arithmetic operation in various data processing technique. The main aim of employing this adder is to reduce the area, power dissipation, and delay. The CSLA is operating in many computational structures to cut the carry propagation delay. The elementary knowledge of this work is to use BEC (binary to excess-1 converter) instead of RCA (Ripple Carry Adder) with Cin=1. By using fewer numbers of logic gates, BEC logic is derived instead of using n-bit FA (Full adder).

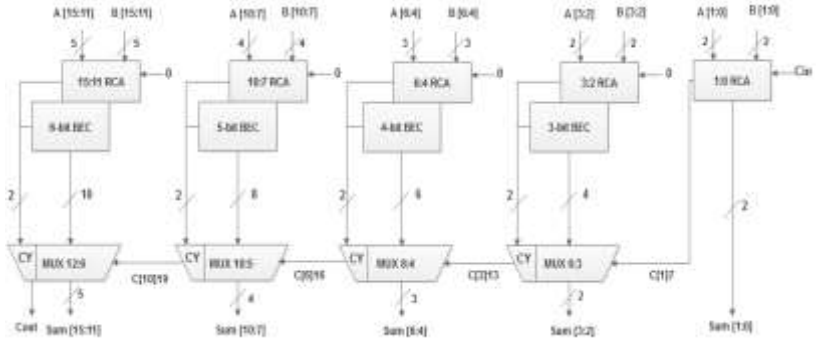

Figure.5. Block diagram of low-area CSLA

The basic idea of this paper is to utilize BEC instead of RCA with in the normal CSLA to achieve low-area and power consumption. The advantage of this BEC logic comes from the lesser number of logic-gates compared to then-bit FA structure. The group2 has one 2-bit RCA, which has 1 FA and 1 HA for instead of another 2-bit RCA with, 3-bit BEC is employed which adds one to the output from 2-bit RCA. The input arrival time is lesser than the multiplexer selection input arrival time. Based on the selection line input Cin, this adder gives either BEC output or multiplexer output. The multiplexer delay and mux selection arrival time derived from the different kind of groups.

The considerable variations in memory usage can be put down to the optimization of the fixed value comparator. When comparing values to a fixed number, and depending on the value of the fixed number, not all bits required to be taken into account. In the comparator, the 8-bit bin structure output compared to the median index. For example, Cent value is 8 bit binary value (med index = 8'd2). cmp_out_0= bout0 <med index into cmp_out_255= bout255 <med index.

3.4Priority Encoder

In the fig.6 shows the block diagram of 16-PE, Which consists of five LUT designs, five OR logic gates, and one MUX. Each LUT store the memory value of given input bits. Each and every LUT produces two outputs. That two-bit gives into four OR gate logic operation, which provides single bit output. The four single bit Most Significant Bit (MSB) and Least Significant Bit (LSB) outputs have been given into last LUT, its associated with MUX. Selection line-2 bit and four 2-bit LUT has been given to MUX. Finally, the MUX has been providing 4-bit output LSB. In this paper, 256- bit PE has been designed for the LC-PDF architecture, which provides 8-bit output.

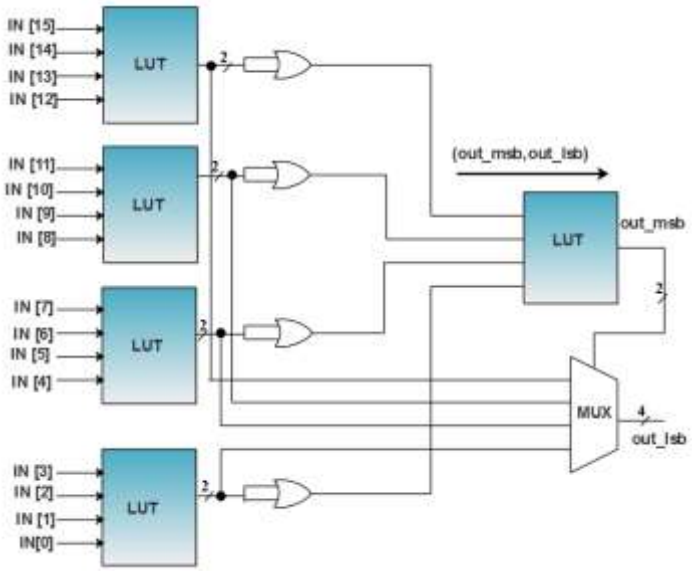

Figure.6. Block diagram of the 16 bit PE

The input image can estimate by employing the PDF estimator, which can be evaluated the input image into given particular interval period. Finally, that Verilog output is given into Matlab for histogram estimator verification. In FPGA implementation, Xilinx tool is required to compute slices, flip flops, frequency, and LUT. Furthermore, to minimize the area, power, and delay by using cadence tool an encounter with 180nm and 45nm library technology.

IV. Results and Discussion

The LC - PDF design timing diagram was verified in Modelsim by using Verilog code. The RTL schematic was taken from Simplify pro tool. FPGA performance was analyzed for different devices of Virtex-6, and Virtex-6 LP by usingXilinx 14.4 ISE tool. ASIC implementation of LC - PDF algorithm was verified by using Cadence tools in 180nm and 45nm library technology.

4.1ASIC Synthesis

This ASIC synthesis is implemented in cadence encounter tool for different technology such as 180nm and 45nm. From this tool, the performance will be calculated such as area, power, and delay.

Table.1.Comparisonof ASIC performances of the existing and LC-PDF method for 180nm and 45nm technology

Technology	Method	Area (μm^2)	Power (nW)	Delay (ps)	APP (μm^2 * nW)	ADP (μm^2 * ps)
180nm	Existing [7]	3913222	1149642041	2839	4498804526966102	11109637258
	LC-PDF	702456	852013617	2786	598502077343352	1957042416
45nm	Existing [7]	512523	135360152	1148	69375191183496	588376404
	LC-PDF	81251	101864837	1120	8276619871087	91001120

In the tab.2 shows a comparison of ASIC performance of the existing and LC-PDF method for 180nm and 45nm technology. In existing method, the normal digital adder is used to perform the PDF operation, which occupies more area. In the LC-PDF method, the CSLA is used in Bin structure, which required less space to operate addition operation. Due to the area, power, delay, APP, and ADP are mitigated in LC-PDF architecture than conventional PDF architecture. These ASIC results have been taken from cadence software for the different libraries such as 180nm and 45nm technology.

From the table.1, it is cleared that LC - PDF method consumes less area, less power, less area power product and less area-delay product than conventional methods.

Table.2. Reduced percentage of area, power, delay, APP, and ADP for LC-PDF method

Technology	Reduced % of Area	Reduced % of the power	Reduced % of Delay	Reduced % of APP	Reduced % of ADP
180nm	82.04	25.88	1.86	86.69	82.38
45nm	84.14	24.64	2.43	88.06	84.53

The reduction percentage of area, power, APP, and ADP for different PE like 1 PE and 2 PE is given in table.2. This architecture result has been taken in both 180nm and 45nm technology. In 180nm technology, 82.04% of area, 25.88% of power, 1.86% of delay, 86.69 % of APP, and 82.38 % of ADP is mitigated in LC-PDF as well as 45nm technology, 84.14 % of area, 24.64% of power, 2.43 % of delay, 88.06% of APP, and 84.53 % of ADP is reduced in LC - PDF method than conventional method.

4.2FPGA Synthesis

This FPGA synthesis is implemented in Xilinx tool for different devices such as Virtex-4, Virtex-5, and Virtex-6. From this tool, the performance will be calculated such as LUT, flip-flop, Slices, and Frequency.

Table.3 shows the comparison FPGA implementation for existing and LC-PDF method, which is used to analyzing the performance parameters such as LUTs, the number of flip-flops, for slices for different FPGA devices such as Virtex 6 different families, and vertex6 LP. From this table, it clears that the LUT, flip-flop, slices are reduced and operating frequency is increased in LUT-CSLA-PDF method than the existing method. Due to the reduction of those parameters, the area has been minimized in LC-PDF architecture. These FPGA results have been taken from Xilinx software

From the table.3, it clears that all the FPGA performance is improved in LC - PDF design compared to conventional methods. The output waveform of the LC- PDF method shown in the figure 5. That output is taken from the Modelsim. From this waveform, it's clears that the LC - PDF architecture is working perfectly. Furthermore, LC-PDF output has been showing the 8-bit of PE output, which represents red color. In the fig.14 shows histogram output, which is taken from the Matlab tool.

Table.3. Comparison FPGA performance for the existing and LC-PDF method.

Target FPGA	methodology	LUT	Flip-flop	Slice
Virtex-6 xc6vcx75t	Existing [7]	2774/46560	1552/93120	756/11640
	LC-PDF	2232/46560	1552/93120	638/11640
Virtex-6 xc6vcx130t	Existing [7]	2774/80000	1552/160000	804/20000
	LC-PDF	2232/80000	1552/160000	649/20000
Virtex-6LP xc6vcx75t	Existing [7]	2774/46560	1552/93120	803/11640
	LC-PDF	2227/46560	1552/93120	655/11640

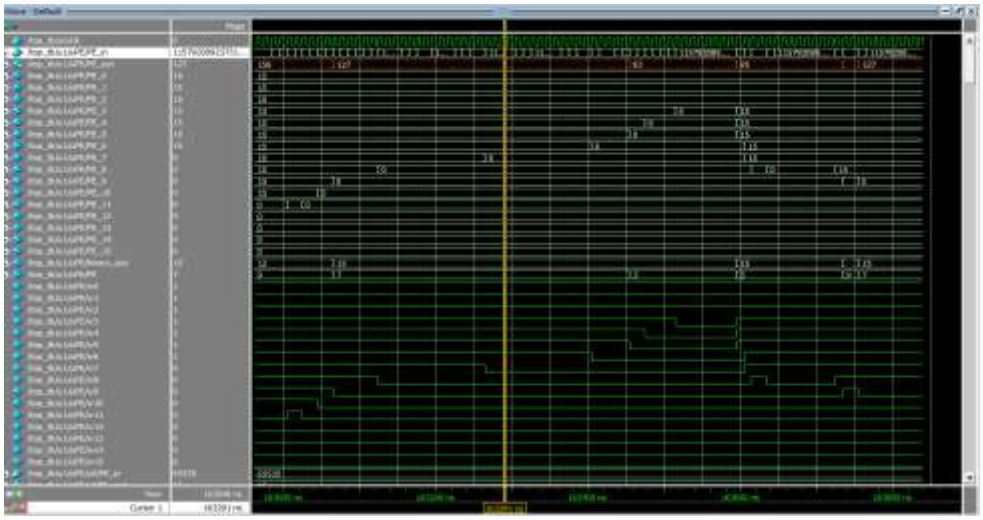

Figure.7. The output waveform of LC-PDF

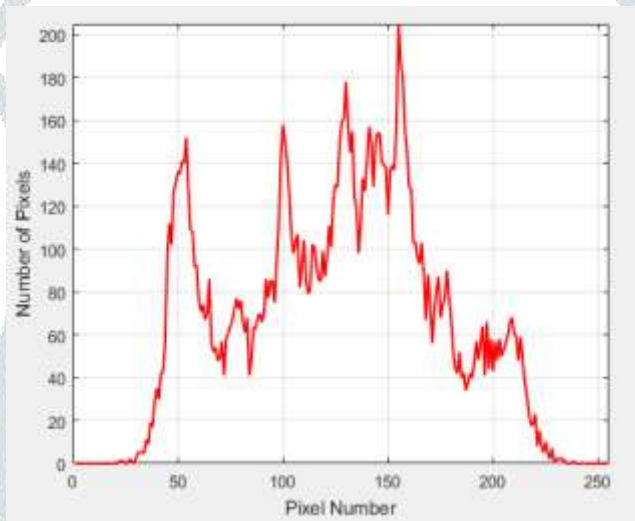

Figure.8.Histogram waveform

The RTL top module of the LC - PDF is shown in figure.9, which is taken from Synplify pro software using Verilog code. This LC-PDF architecture has been a separate code for each block such as FIFO, DROM, bin structure, CSLA, comparator, and a priority encoder. In the fig.10 shows the Virtex-6 output for the LC-PDF method. It is taken form Xilinx tool for verification purpose. As well as the ASIC performance area, power and delay analysis for LC - PDF in the 180nm shown in the fig.11 for verification purpose.

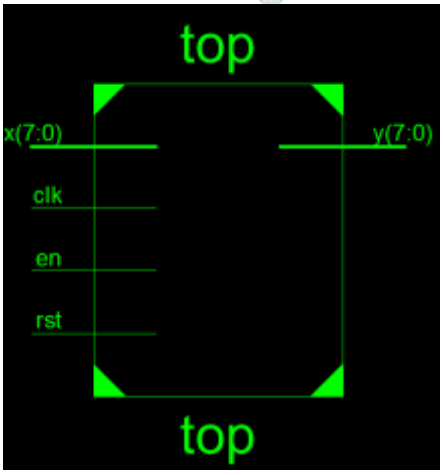

Figure 9. RTL top module

Figure.10.Virtex 6 for an LC-PDF method

Figure.11.Area, power and delay analysis for LC - PDF in 180nm

The RTL schematic of LC - PDF design is shown in fig.9, which is taken from cadence tool. For ASIC implementation, the same code is used for the FPGA implementation. Cadence RTL compiler is used to convert RTL Verilog into Gate level Verilog. Verilog codes are read by using a Tcl file and corresponding libraries also set into the Tcl file. After synthesizing, Area, Power and Delay, the result is displayed in cadence tool. The overall cadence output of LC - PDF method is shown in the fig.11. From cadence tool, get this results for 180nm technology, which is shown as a screenshot for verification purpose. From this screenshot, it clears that total area, total delay, total power, APP and ADP is reduced in LC - PDF method compared to the existing methods.

V. CONCLUSION

In this paper, the LC-PDF architecture has been done in the Modelsim by employing Verilog code. The LC-PDF method has been implemented by using CSLA design. In this work, the CSLA design used instead of the normal adder for addition operation of the bin architecture. Furthermore, the LUT module was employed in the priority encoder for storage purpose, so the storage area is less compared to the existing PDF architecture. In FPGA implementation, LUT, slice and flip-flop are reduced in the LC-PDF architecture design. In 180nm technology, 82.04% of area, 25.88% of power, 1.86% of delay, 86.69 % of APP, and 82.38 % of ADP is mitigated in LC-PDF as well as 45nm technology, 84.14 % of area, 24.64% of power, 2.43 % of delay, 88.06% of APP, and 84.53 % of ADP are mitigated in the LC - PDF method than conventional method.

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