JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

FPGA based Barrel shifter Design and Implementation using Verilog HDL

Anam Srinivasa Reddy [#1], Mohammed Abdul Raqeeb [#2], Meenaiah Batta [#3]

Department of Electronics and Communication Engineering, Vignan Institute of Technology and Science, Deshmukhi.

Abstract: A shifter of barrels may be advanced circuit that can transfer a data word by a certain number of bits in a single clock cycle. This might be possible to execute no of multiplexers, in such execution one mux's output is associated with following separately, in such a manner that is predicated on the move. Along with number juggling and rationale operations barrel shifter is utilized to move a craved no of bits in a wanted course. An 8-bit and 16-bit barrel shifter is presented in this research actualized utilizing Verilog.

Keywords: **Multipliers, Logical shift right, logical shift rotate, Field programmable gate array.**

I. INTRODUCTION

A Barrel Shifter is a rationale part that performs shift or turn tasks. Barrel shifters are material for computerized signal processors. This part configuration is for regular size (4,8, 16.) barrel shifters that perform shift right intelligent, shift left sensible, turn left and pivot right activities relying upon the launch boundaries. The left and right activity is executed through reversal of the info and result vectors. The quantity of multiplexing stages is comparative with the width of the information vector.

Block Diagram

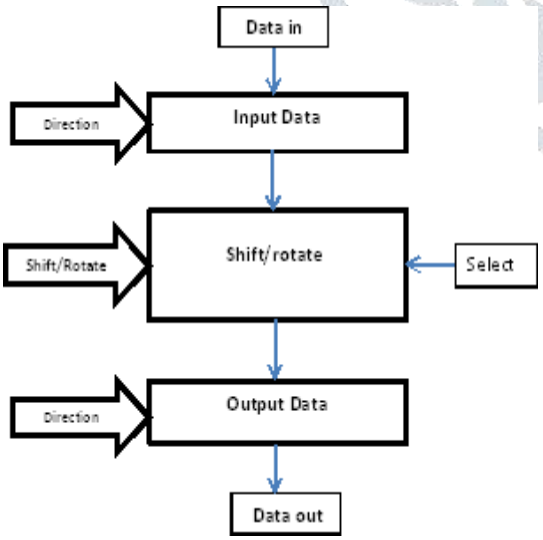


Fig 1- Block Diagram of Barrel Shifter

Moving and turning information is needed in a few applications including number-crunching tasks, variable length coding, are bit ordering. Subsequently, barrel shifters, which are equipped for moving or pivoting information in a solitary cycle. Select lines are utilized to indicate how much shift as it were. A barrel shifter can be planned by utilizing mux trees.

Architecture

1. *Logical shifter right:*

A consistent right shifter utilizing a front referenced methodology is displayed in the figure 1. The first line relates to a shift of one, while the last column compares to a shift of four, As required, zeros take care of the great request locale. Thus, interconnects highway zero into the high request multiplexers. The qualities x_amt[x] addresses the piece in place x of the shift sum, and as such addresses the worth 2^x.

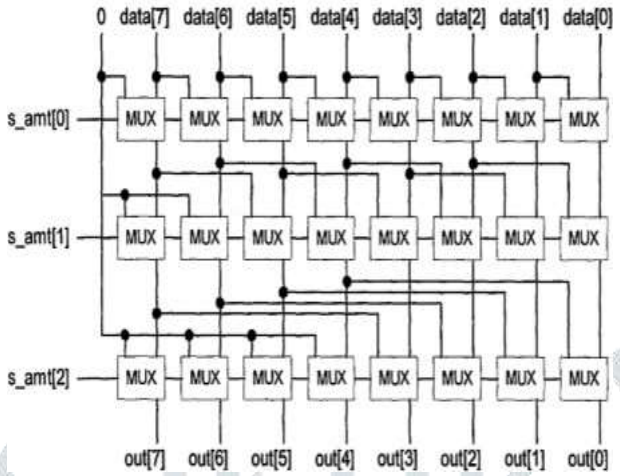


Fig 2- Logical Right Shifter

1.1 Operation of right shifter:

The shift right consistent activity is similar as a turn right however without the lower request bits (LSB) being moved to a high request (MSB) position. All things being equal, the LSB pieces are taken out. The excess pieces are moved to one side to make up for the shortcoming made by the deficiency of the low request bits (LSB). The void made in the MSB district by this shift is loaded up with zeros.

Fig 3- Right Shifter Operation

As displayed in model beneath, the LSB bit is eliminated from the outcome and the leftover pieces are shifter over. The request pieces are set to nothing.

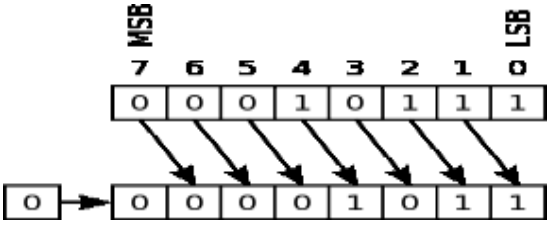


Fig 4- Example of right shifter

2. *Right Rotator:*

A right rotator is basically the same as a coherent right shifter. The contrasts between the two lies in the way in which interconnect lines are put, specifically, since every one of the information pieces are directed to the result, there could be at this point not a requirement for interconnect lines conveying the zero sign. All things considered; interconnect lines should be embedded to empower directing of the low request bits from each line to high request district so that pivot can happen. The more extended interconnect lines of the rotator, notwithstanding, can increment both region and deferral

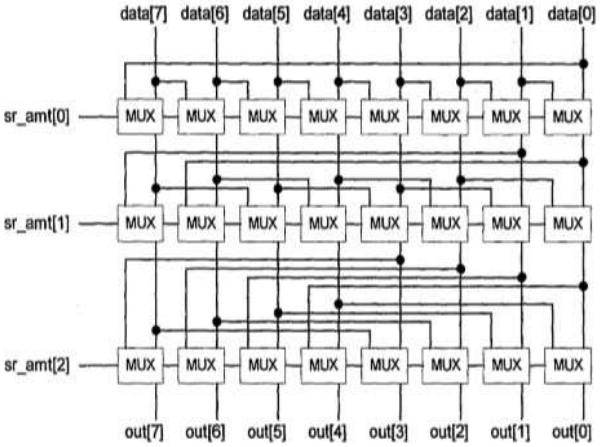


Fig 5: Right Rotator

2.1 Operation of right rotator:

Pivot is a cyclic shift either to the left or right. This implies that as pieces are moved out of the information vector on one side, they are moved into the information vector on the opposite side. During this interaction, all pieces from the information are steered to the result. Their situation in the result, be that as it may, isn't really equivalent to it was in the info.

Fig 6- Right Rotator Operation

An example of rotate right can be seen in the figure 6 where a 8-bit word of data has a one bit rotated right.

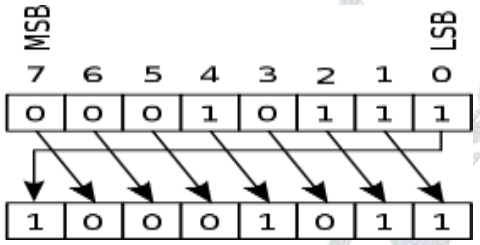


Fig 7- Example for right rotator

II. RESULTS

The below figures show the RTL schematics of 8 & 16-bit barrel shifter .

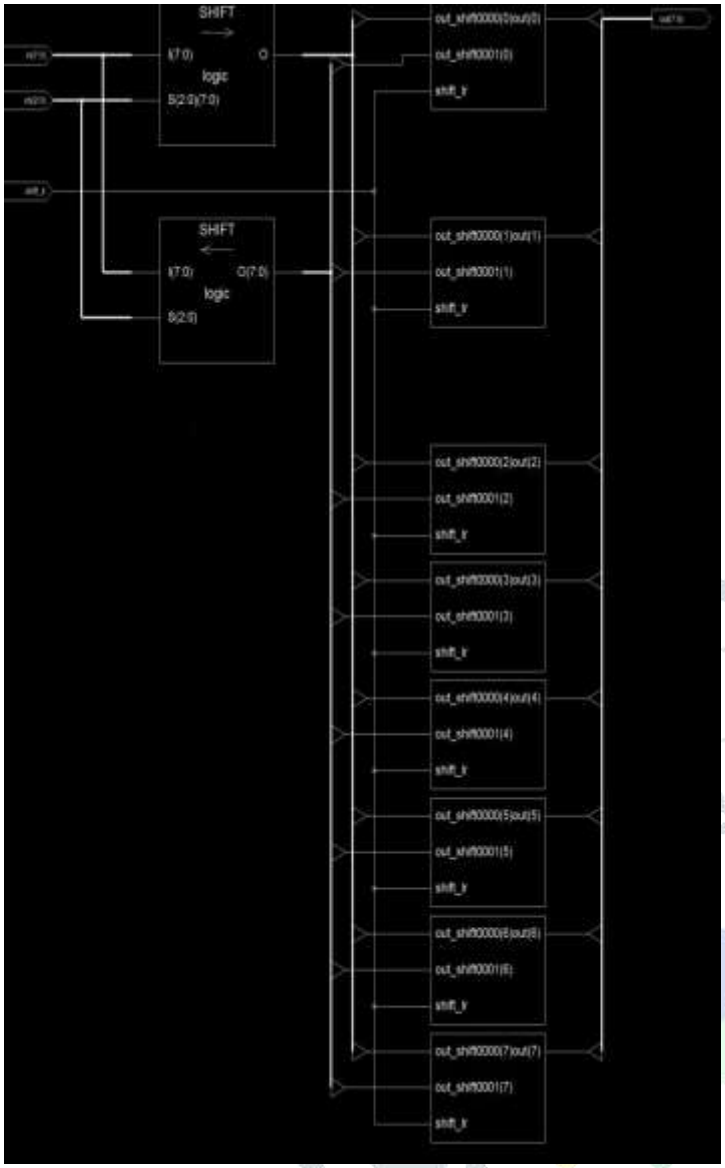


Fig 8- RTL View of eight-bit barrel shifter

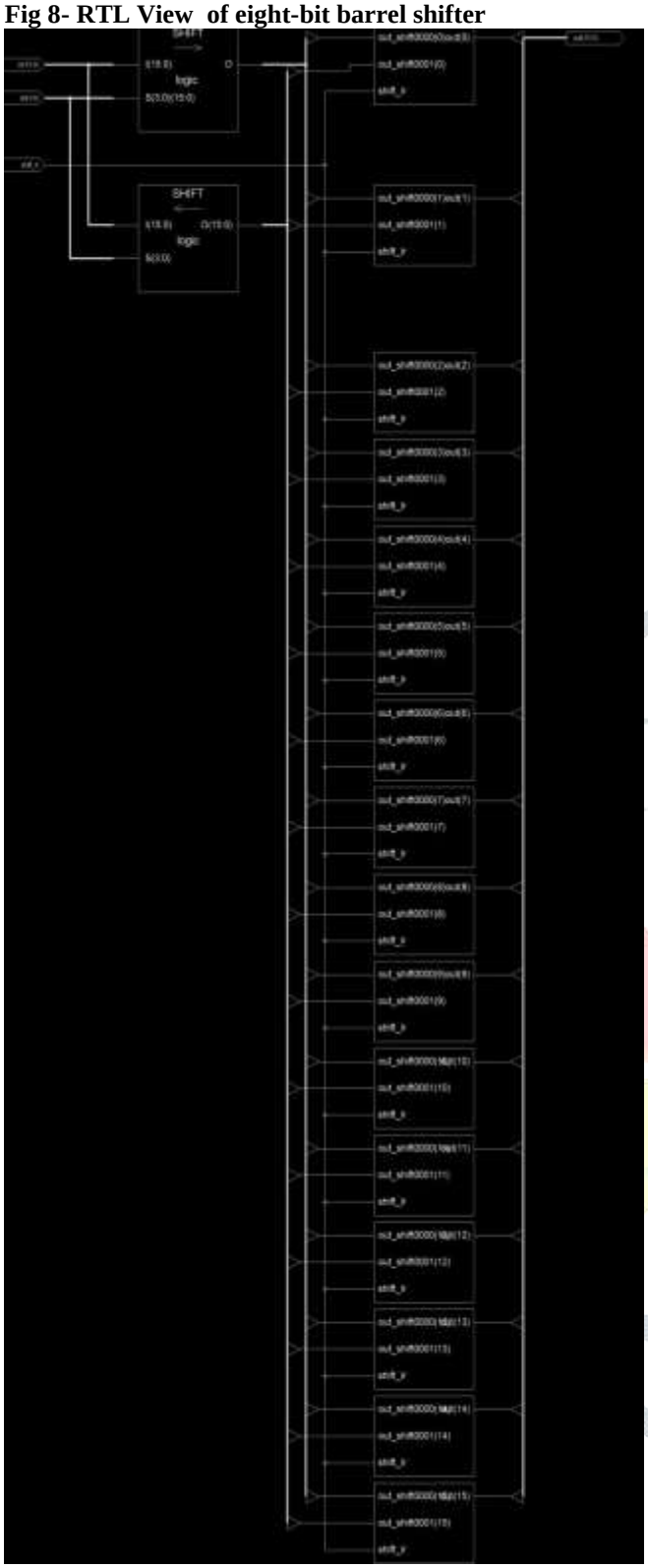
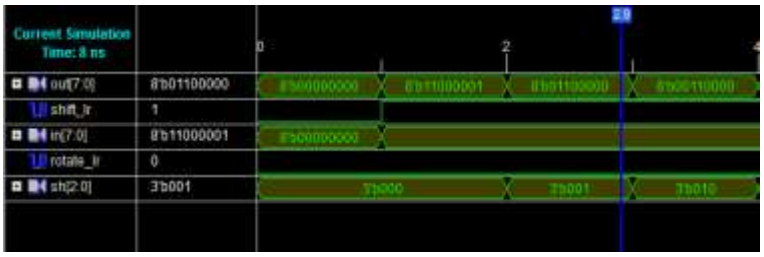
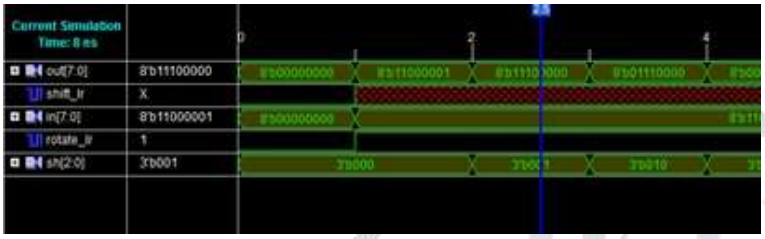


Fig 9- RTL View of Sixteen-bit barrel shifter

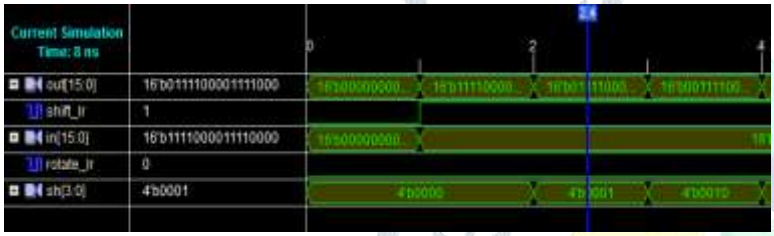
The shown below are the 8 bit and 16-bit barrel shifter results for different operations such as right shift and right rotate.



Output **waveform of** eight-**bit Barrel Shifter (shift right)**



Output waveform of eight-bit Barrel Shifter (rotate right)



Output waveform of Sixteen-bit Barrel Shifter (shift right)

Output waveform of Sixteen-bit Barrel Shifter (rotate right)

Device Utilization Report			
Logic	**Used**	**Available**	**Utilization**
No. of slices	**18**	**860**	**1%**
No. of LUTs	**33**	**1540**	**1%**
No. of IOBs	**16**	**46**	**22%**

Table 1- Usage summary of eight-bit barrel shifter

Device Utilization Report			
Logic	**Used**	**Available**	**Utilization**
No. of slices	**55**	**910**	**4%**
No. of LUTs	**101**	**1590**	**4%**
No. of IOBs	**22**	**56**	**46%**

Table 2- Usage summary of sixteen-bit barrel shifter

III. CONCLUSION

We have proposed and planned a Verilog usage of FPGA based barrel shifter which deliver obvious comes about and illustrated that our approach yields and tall speed barrel shifter.

REFERENCES

[1]M.Seckora, Barrel Shifter or Multiply/Divide IC Structure," U.S. Patent 5,465,222, November 1995.
[2] J. Muwafi, G. Fettweis, and H. Neff, "Circuit for Rotating, Left Shifting, or Right Shifting Bits," U.S. Patent 5.978,822, December 1995.
[3]A.Yamaguchi, \Bidirectional Shifter," U.S. Patent 5,262,971, November 1993.
[4] G. F. Burns, \Method for Generating Barrel Shifter Result Flags Directly from Input Data," U.S. Patent 6,009,451, December 1999.