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Optimization Analysis of Multi-rate Approach based LMS Adaptive Filter using Distributive Arithmetic Technique

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Abstract: **More and more people around the world suffer from digital signal processing research field. The increase hardware complexity and increase area are the main reasons for this field. The multi-rate approach used for narrow band filter is designed and implemented in Xilinx Vertex-E XCV50E device family. The multi-rate approach is design using the decimator and interpolator structure in VHDL. Each structure is simulated using Xilinx Vertex-E XCV50E device family and compared the existing structure. The resulting structure is hardware efficient and consumes less slices compared to existing structure.**

Index Terms **– Filter Coefficient, Finite Impulse Response, Pass-band Frequency, Narrow Band Filter**

I. INTRODUCTION

Adaptive filter is extensively used in noise and echo cancellation, system identification, channel estimation and equalization [1]. It comprises of a linear finite-impulse-response (FIR) filter whose transfer function is adjusted by changing the filter weights according to an optimization algorithm. Usually, least-mean-square (LMS) algorithm is preferred to update the filter weights due to its simplicity and ease of implementation. The combined FIR filter and the weight update unit consists of several multiply-and-accumulate (MAC) units depending upon the filter order. The computational efficiency of MAC based LMS adaptive filter is lower due to the large size of multipliers in MAC units. In most practical applications, the computational efficiency of any system can be improved by reducing the hardware complexity. One of the fundamental approach is sequential processing which reduces implementation complexity by using single computational unit over several number of clock cycles. But, it involves more latency, for example, if the filter order is N, then it would require at most N clock cycles.

Conventional converters are often difficult to implement in fine line very large scale integration (VLSI) technology. By keeping these things in mind the people are going for over sampling converters, these converters make extensive use of digital signal processing. The main advantages of the sigma delta A/D converters are mentioned below.

- Higher reliability.
- Increased functionality.
- Reduced chip cost.

Those characteristics are commonly required in the digital signal processing environment of today. Consequently, the development of digital signal processing technology in general has been an important force in the development of high precision A/D converters which can be integrated on the same die as the digital signal processor itself. Conventional high-resolution A/D converters, such as successive approximation and flash type inverters, operating at the Nyquist rate (sampling frequency approximately equal to twice the maximum frequency in the input signal); often do not make use of exceptionally high speeds achieved with a scaled VLSI technology. These Nyquist samplers require a complicated analog low pass filter (often called an anti-aliasing filter) to limit the maximum frequency input to the A/D, and sample-and hold circuitry. The high resolution can be achieved by the decimation process. Moreover, since precise component matching or laser trimming is not needed for the high-resolution sigma delta A/D converters, they are very attractive for the implementation of complex monolithic Systems that must incorporate both digital and analog functions [4].

The remainder of the paper is organized as follows: multi-rate approach algorithm is presented in Section II. The proposed structures of narrow band filter are presented in Section III. Hardware and time complexity of the proposed structures are discussed and compared with the existing structures in Section IV. Conclusion is presented in Section V.

II. MULTI-RATE APPROACH

The process of converting a signal from a given rate to a different rate is called sampling rate conversion. The systems which employ multiple sampling rates in the processing of digital signal are called multi-rate signal processing [5].
Decimation is the processes of lowering the word rate of a digitally encoded signal, which is sampled at high frequencies much above the nyquist rate. It is usually carried out to increase the resolution of an oversampled signal and to remove the out-of-band noise. In a sigma-delta ADC, oversampling the analog input signal by the modulator alone does not lower the quantization noise; the ADC should employ an averaging filter, which works as a decimator to remove the noise and to achieve higher resolutions. A basic block diagrammatic representation of the decimator is shown in Figure 1.The decimator is a combination of a low pass filter and a down sampler. In Figure 1 the transfer function, H(z) is representative of performing both the operations. The output word rate of the decimator is down sampled by the factor M, where M is the oversampling ratio [6]. The function of low pass filtering and down sampling can be carried out using an averaging circuit. The transfer function of the averaging circuit is given by equation (1.1). It establishes a relation between the input and output functions (1.1)

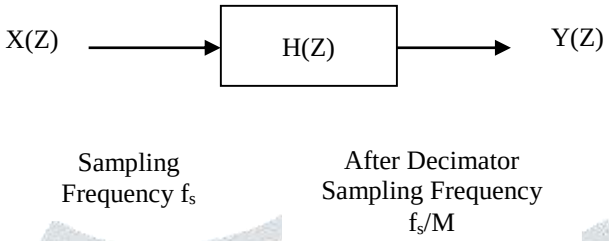

Figure 1: Block Diagram of Decimator

$$H(Z) = \frac{X(Z)}{Y(Z)} = \frac{1}{M}\sum_{x=0}^{M-1} Z^{-x} \quad (1)$$

"Up sampling" is the process of inserting zero-valued samples between original samples to increase the sampling rate. (This is called "zero-stuffing".) Up sampling adds to the original signal undesired spectral images which are centered on multiples [7] of the original sampling rate.
"Interpolation", in the DSP sense, is the process of up-sampling followed by filtering. (The filtering removes the undesired spectral images.) As a linear process, the DSP sense of interpolation is somewhat different from the "math" sense of interpolation, but the result is conceptually similar: to create "in-between" samples from the original samples.
The result is as if you had just originally sampled your signal at the higher rate. Increasing the sampling frequency use interpolator

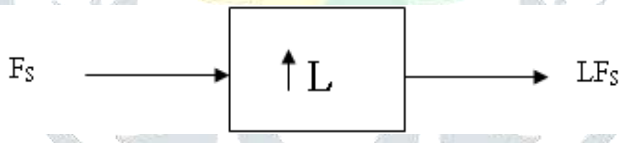

Figure 2: Interpolation with factor L

Since interpolation relies on zero-stuffing you can only interpolate by *integer* factors; you cannot interpolate by fractional factors. (However, you *can* combine interpolation and decimation to achieve an overall rational factor, for example, 4/5
Up-sampling adds undesired spectral images to the signal at multiples of the original sampling rate, so unless you remove those by filtering, the up-sampled signal [7] is not the same as the original: it's distorted.
Some applications may be able to tolerate that; for example, if the images get removed later by an analog filter, but in most applications you will have to remove the undesired images via digital filtering. Therefore, interpolation is far more common [8] that up-sampling alone.

III. PROPOSED METHODOLOGY

In this work the design of a decimation filter is presented for integrating with an existing designed modulator to form a complete sigma-delta ADC. we use multi-stage decimation filter which means the single decimation filter is replaced by cascaded filters. In this chapter, we are going to talk about the filter architecture used in this work, including their structures, strengths and drawbacks. the first step in designing a decimation filter is to decide which types of filters will be used and where decimation will occur. This chapter explores the issues involved in choosing filter architecture for a hearing aid application. The relative power of several architectures is compared, resulting in the three-stage architecture that is chosen to implement this filter.
A common need in electronics and DSP is to isolate a narrow band of frequencies from a wider bandwidth signal.
Narrowband filters instead capture only a very small part of the spectrum. They are said to have a narrow band-pass. The band-pass is simply how much of the spectrum the filter allows to pass. This is usually measured in nanometers. Narrow band filter consists of decimator, narrow band and interpolator.

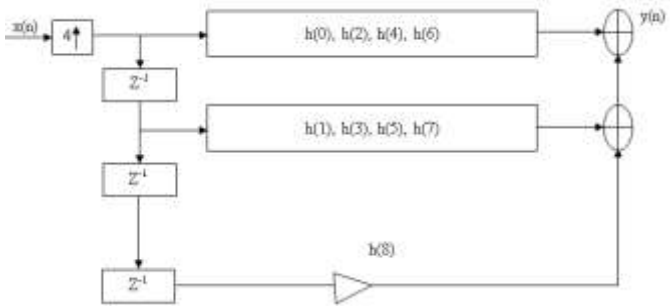

Figure 3: Interpolator structure with filter order N3=9 and L=4

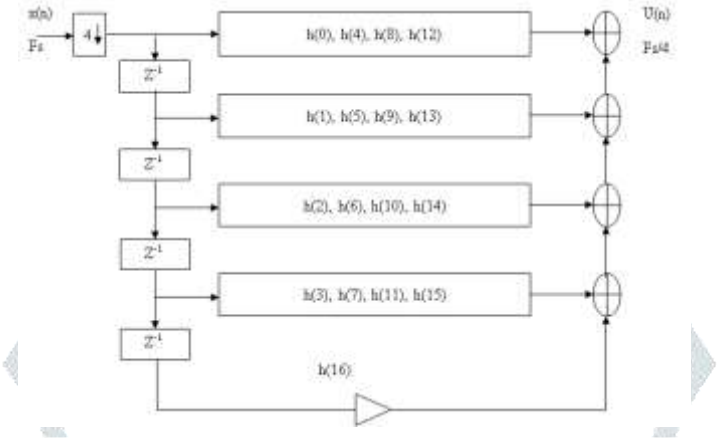

Figure 4: Decimator structure with filter order N1=17 and M=4

Table 1: Theoretical Analysis of Direct Method and Multi-rate Approach for Different Filter Coefficient and Sampling Frequency

Author	Sampling		Filter Coefficient	Multiplier	Adder	Register	Cycle Period
Direct Method	1		08	08	07	07	$08T_S$
	1		09	09	08	08	$09\ T_S$
	1		17	17	16	16	$17\ T_S$
	1		38	38	37	37	$38\ T_S$
	F_S=150Hz		150	150	149	149	$150\ T_S$
Multi-rate Approach	Decimator	2	09	09	08	08	$09\ T_S$
		4	17	17	16	16	$17\ T_S$
	NBF	2	75	75	74	74	$75\ T_S$
		4	38	38	37	37	$38\ T_S$
	Interpolator	2	05	05	04	04	$05\ T_S$
		4	09	09	08	08	$09\ T_S$

IV. **SIMULATION RESULTS**

The proposed architecture has very low hardware complexity compared to direct approach based structures, because direct method requires more multiplier compare to proposed architecture. In the proposed architecture, calculate the decimator and interpolator structure for design a narrow band filter.

Table 1 shows the theoretical analysis of direct method & multi-rate approach for different filter coefficient and sampling frequency. Table 2 shows cell usage for the Comparison of Performance of the Proposed Implementation and the Existing Implementation of Narrow Band Filter.

Table 2: Comparison of Performance of the Proposed Implementation and the Existing Implementation of Narrow Band Filter

Order	Proposed Structure		Yajun Zhou et al.	
	Area (Slice)	MHF (MHz)	Area (Slice)	MHF (MHz)
8	180	258.665	208	252.14
9	203	258.665	235	252.14
17	390	258.665	430	252.14
38	868	258.665	935	252.14

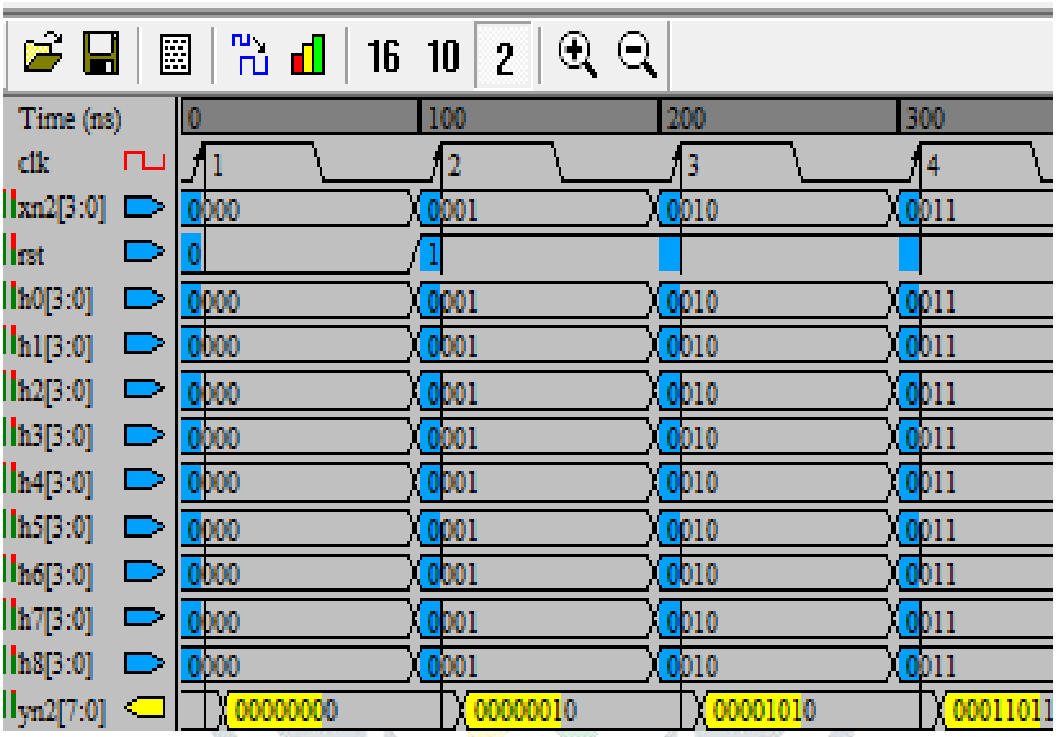

Figure 5: Output Test Bench Waveform of Narrow Band Filter (Filter Coefficient N=9)

The design as were discussed in figure 3 and figure 4 were implemented using VHDL and then were tested on model sim to determine the number of slice and maximum high frequency. In figure 5, figure 6 and figure 7 have shown the output waveform of narrow band filter and chat between filter order and slices. In figure 7, compare the result between numbers of slice and filter order. Increase the filter order also increase the number of slice shown if figure 7.

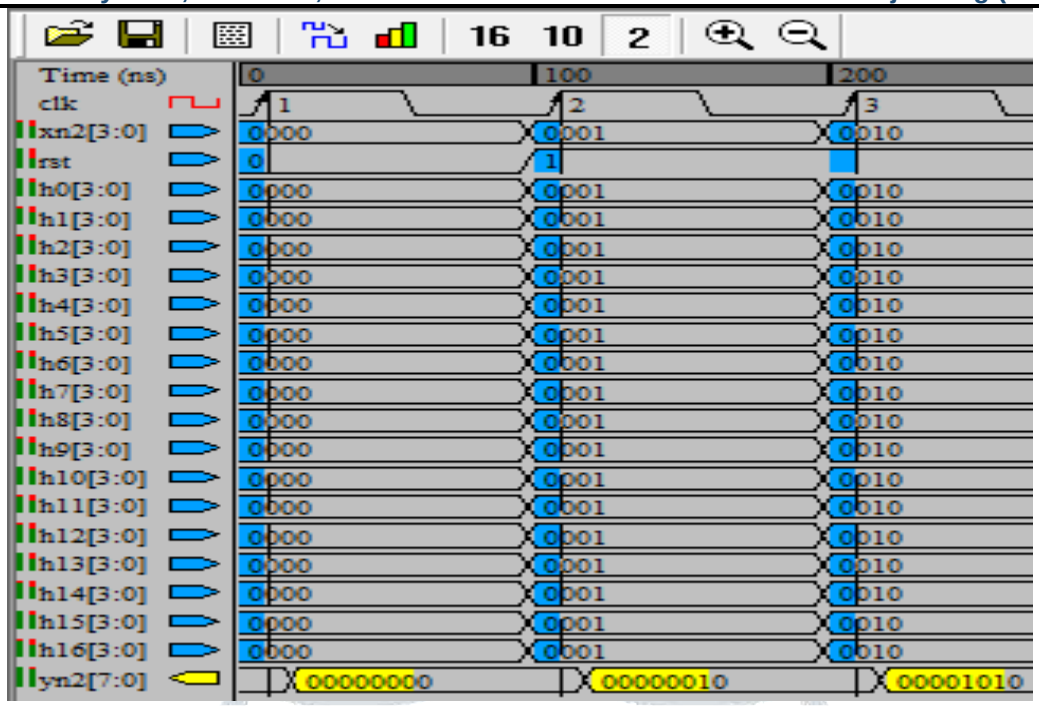

Figure 6: Output Test Bench Waveform of Narrow Band Filter (Filter Coefficient N=17)

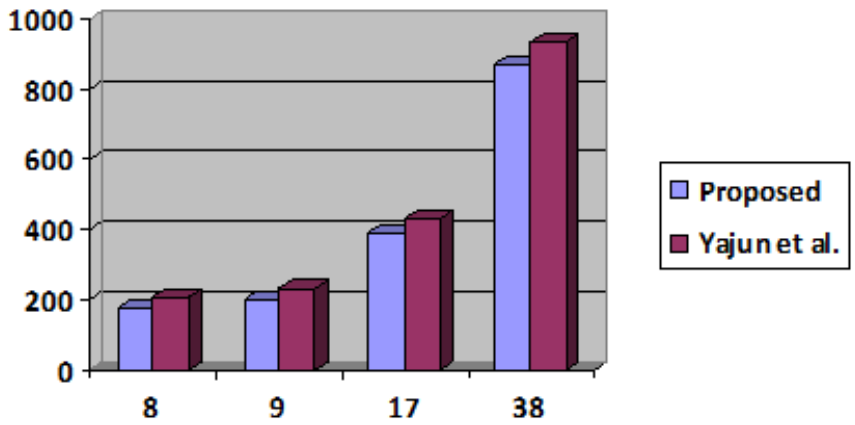

Figure 7: Show the Graph between Filter Coefficient and Area (Slice)

X axis:- Filter Coefficient

Y axis:- Number of Slice

V. CONCLUSION

In this paper, a new area and power efficient design for DA based LMS adaptive filter has been presented. The proposed approach is based on storing OBC combinations of input samples and filter weights in two separate LUTs. In the proposed implementation, the recent sample has been stored in LUT due to that decomposition of LUT is not possible, unlike the case of [6]. Thus, the savings in area and power are significant due to less hardware complexity and non-concurrent LUT update scheme over [6]. To implement the narrowband filter, we therefore chosen down sampling factor 4 and designed the decimator, interpolator and narrowband filter. The total number of filter coefficients required to realize the decimator, interpolator and the narrowband filter 64 which is almost 58% less than the direct method.

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