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Design and Analysis of RFID Memory Cell based on Static-RAM

Swati Asati, Prof. Shivraj Singh

[1]Research Scholar, Dept. of ECE., Technocrats Institute of Technology, Bhopal, India
[2]Assistant Professor, Dept. of ECE., Technocrats Institute of Technology, Bhopal, India
swatiasati18@gmail.com , 86.shivraj@gmail.com

Abstract : Radio Frequency identification is an automatic identification method that uses wireless non-contact radio frequency waves in which data is digitally encoded in RFID tags or smart labels which can be read by reader through radio waves. The design of memory elements of SRAM for RFID plays a major role in electronic applications. This research presents design and analysis of RFID memory cell based on static-RAM. Tanner software is used for designing and simulation. 12T and 13T RFID-SRAM is proposed in this research. Simulation results show the significant improvement in the performance parameters.

IndexTerms **– RFID, SRAM, Memory, Cell, Tanner, 12T.**

I. INTRODUCTION

Memories are widely utilized in aviation applications as the medium to store information in which single event upsets induced by radiation particles are becoming one of the hugest issues. Since they can conduce to the information debasement in a memory chip and the circuit itself isn't for all time harmed, SEUs are likewise described as the delicate errors. Along these lines, SEUs can cause a breaking down of an electronic system. In some basic memory applications (e.g., satellite equipment and cardioverter defibrillators), SEUs can be unfavorable and crucial. However, radiation solidifying procedures for recollections are one of the bottlenecks in giving adaptation to non-critical failure.

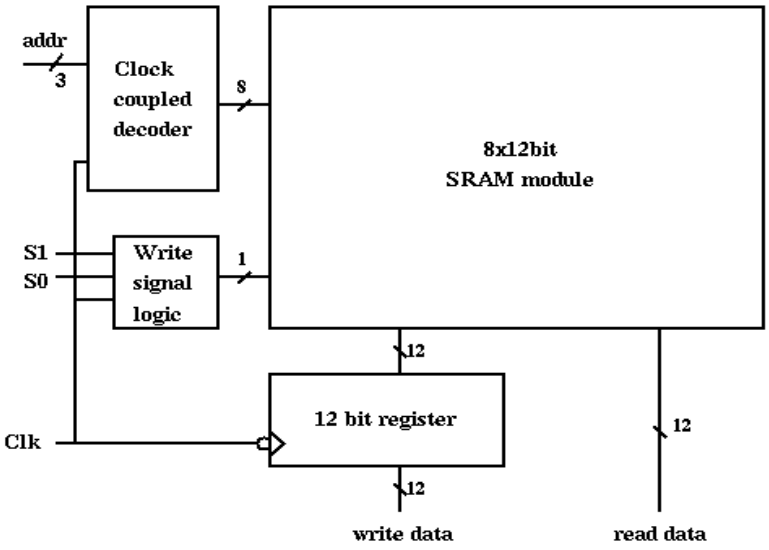

Figure 1: Block Diagram for the SRAM module

For a long time, some radiation hardening by design(RHBD) strategies have been utilized to endure delicate errors in recollections utilizing standard business CMOS foundry processes, without any adjustments to the current procedure or violation of configuration rules. Customarily, these techniques can be predominantly isolated into the accompanying three sub item techniques.

Format level procedures utilize mostly design changes, such as H-entryway, T-door, annular-entryway, and shallow trench isolation for the radiation tolerance. Although it is commonly obvious that these format level techniques do give incomplete assurance ability, they are hard to actualize in nanometer innovations due to increasingly urgent plan rules.

II. BACKGROUND

D. Pathak et al., [1] The proposed design incorporates an off-chip differential double band radio wire with differnetial double band matching organization followed by a CMOS cross coupled rectifier for RF-DC change which replaces a battery in a few RFID applications. The proposed differential double band matching organization for the rectifier gives a pinnacle proficiency of 60% at - 12 dBm at 0.9 GHz and 64% at - 16 dBm at 1.8 GHz. The proposed engineering accomplishes better productivity for lower input power goes from - 20 dBm to 8 dBm which executed utilizing UMC 0.18 µ m CMOS Innovation.

M. H. Ouda et al., [2] The proposed engineering mitigates the converse spillage issue in regular, cross-coupled rectifiers without corrupting awareness. A model is intended for UHF RFID applications, and is executed utilizing 0.18 µm CMOS innovation. On-chip estimations exhibit an awareness of - 18 dBm for 1 V result more than a 100 kω load and a pinnacle RF-to-DC power transformation effectiveness of 65%. A traditional, completely cross-coupled rectifier is manufactured close by for examination and the proposed rectifier shows more than 2× expansion in unique reach and a 25% helping in yield voltage than the regular rectifier.

M. Kumari et al., [3] This work proposes another circuit plan for Extremely High Recurrence (VHF) radio telemetry, to scale down dynamic RFID labels for following little bugs and honey bees. It presents a CMOS bug label execution for creating 150 MHz burst-mode flagging plan by utilizing computerized approach which was not revealed previously.

M. Kumari et al., [4] The new telemeter circuit utilizes a 150-MHz voltage-controlled ring-oscillator (VCRO) taking care of into a course of recurrence dividers whose results are joined (without requiring control rationale) to produce incredibly low obligation cycle burst-mode transmission sign to save power. Also, it is the main headway of the VHF telemeter that joins computerized code for bug label distinguishing proof, contrasted and the current situation with the-workmanship simple techniques which utilize little recurrence shifts from a reference f o (~150 MHz) to f o +Af MHz for individual label ID.

B. Wang et al., [5] This work presents a super high-recurrence (UHF) inactive sense tag for electrical matrix and substation warm checking, with accentuation on the label framework advancement and the plan of a low power inserted temperature sensor. The planned tag accomplishes a responsiveness of - 12.3 dBm under dynamic temperature checking activity, which is the best in class among existing UHF detached temperature sense label items.

III. METHODOLOGY

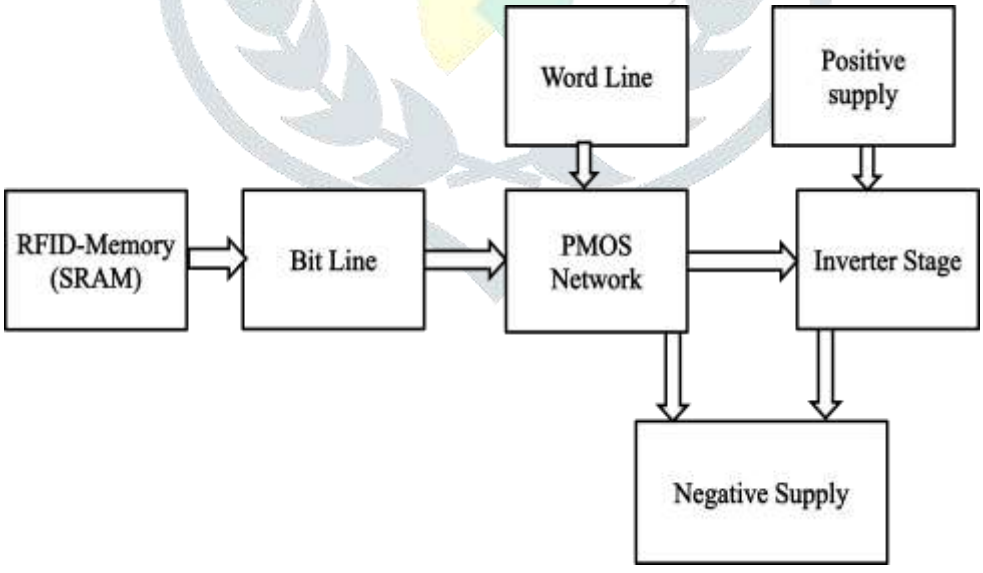

Figure 2: Flow block diagram

The RFID-SRAM architecture is mainly used to the single cell storage process in any type of memory architecture. And the architecture requires less power consumption for the storage of 1-bit. The SRAM architecture is consumes less energy due to the internal memory placement. And to design the SRAM cache architecture also. The RFID-SRAM CMOS design is to apply the STT-MRAM CACHE memory architecture and to reduce the overall power consumption level and improve the performance.

Their ON/OFF state is controlled by a word-line WL. It ought to be noticed that when a radiation molecule strikes pMOS transistor, just a positive transient heartbeat (0→1or 1 → 1 transient heartbeat) can be produced; on the contrary, only a negative transient heartbeat (1 → 0 or 0→0 transient heartbeat) can be induced when a radiation molecule strikes nMOS transistor. Accordingly, so as

to stay away from a negative transient pulse induced by a radiation molecule in Q and QN nodes, pMOS transistors (i.e., transistors P6 and P5) are utilized as access transistors.

IV. SIMULATION RESULTS

The implementation of the proposed design is done over Tanner EDA 13.0. Various simulation toolbox or window is available. Tanner library have different files to complete and execute various designs.

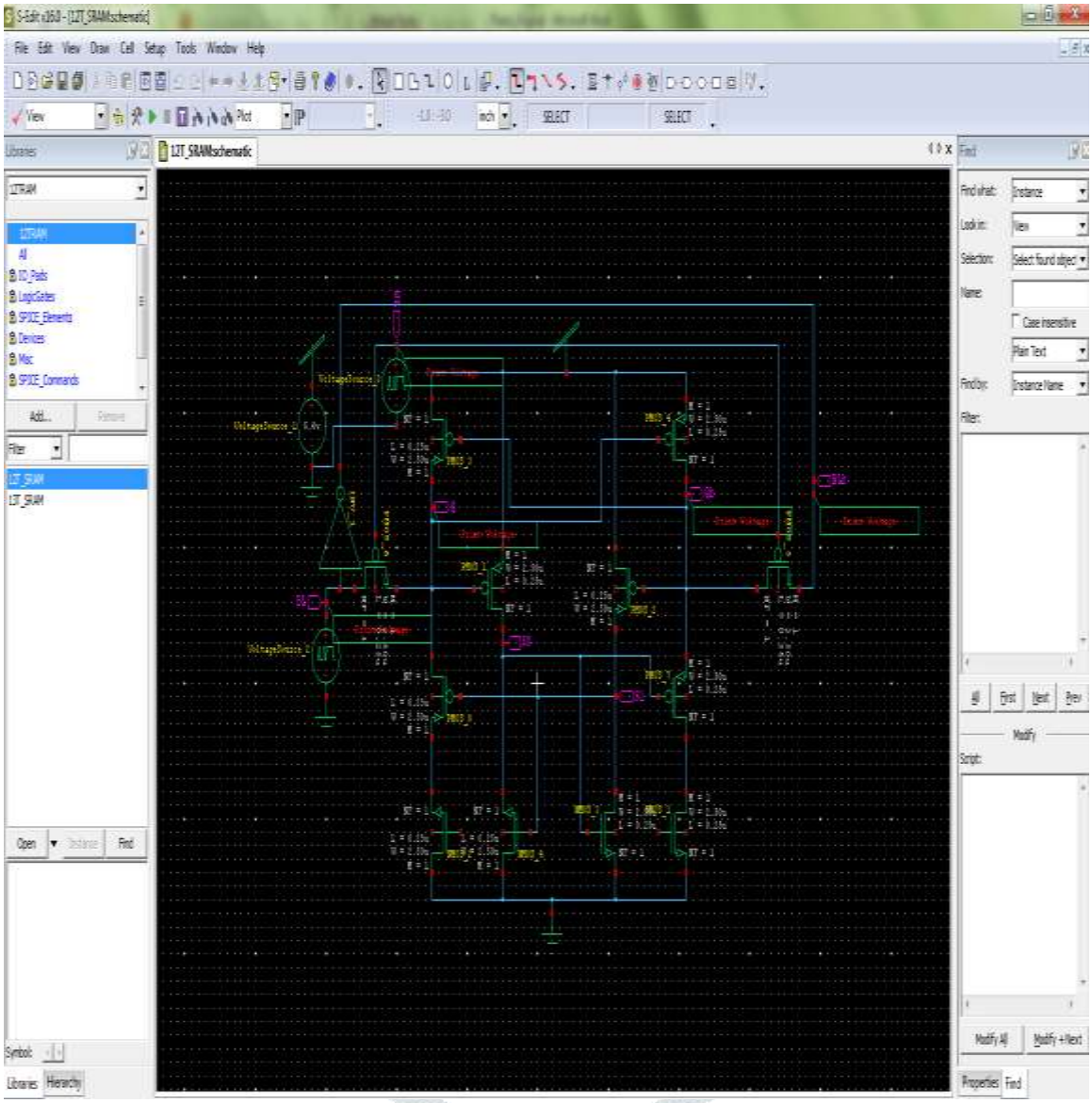

Figure 3: Proposed 12T RFID--SRAM Design

Figure 3 is demonstrating proposed WWL12T RFID-SRAM cell circuit geography for solid and stable space applications. The activity methods of a WWL12T RFID-SRAM cell with moderate access transistors (N-type) to lay the basis. It is clarify the detail read, write and backup tasks. The created 10 nm high performance (HP), low power (LP) and Single Event Tolerant space applications.

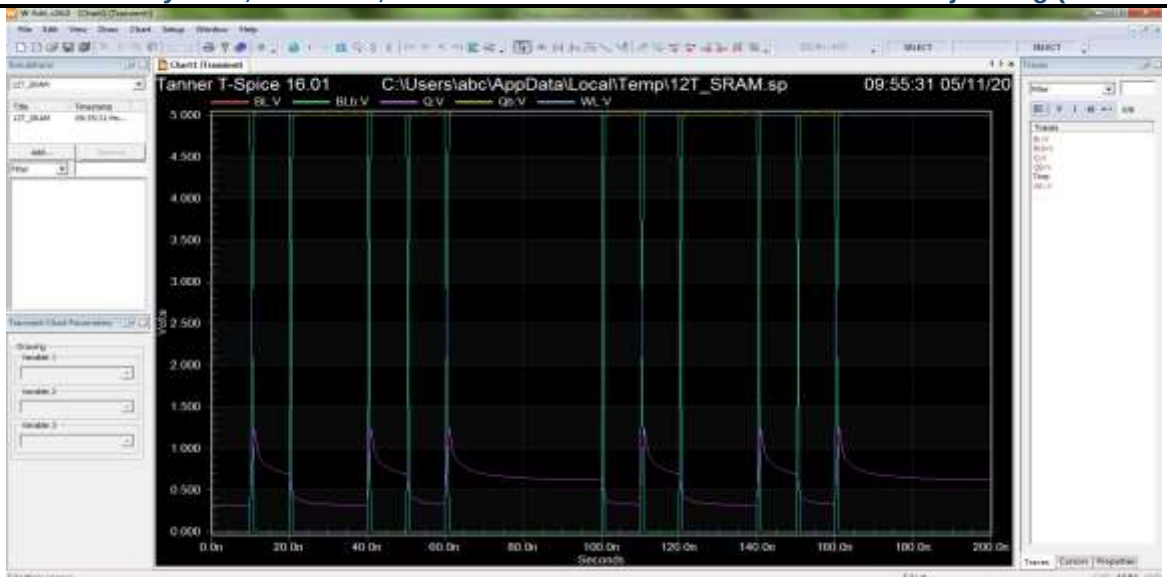

Figure 4: 12T RFID-SRAM waveform

Figure 4 is demonstrating yield waveforms. PGL3 and PGR3 assume a significant job in improving strength in the read method of activity. During the read activity, bitlines (BL and BLB) are kept at VDD, and the wordline (WL) is empowered to turn on PGL1 and PGR1.

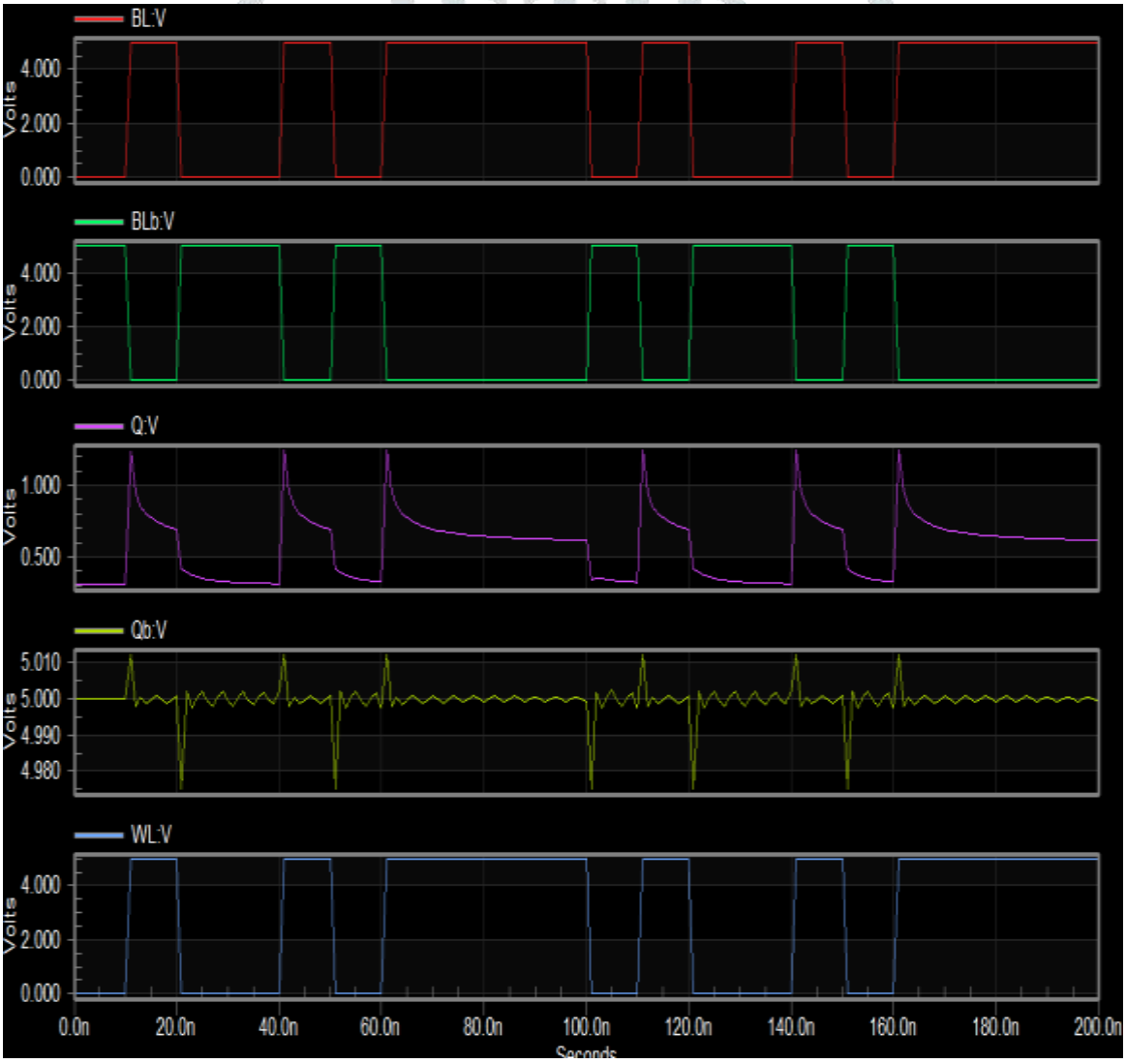

Figure 5: 12T RFID-SRAM voltage vs time output

Figure 5 shows the voltage versus time yield during different modes, in the hold mode, bit-lines are pre-charged to the VDD and the WL and WWL are kept at ground. PGL1, PGL2 PUL, and PDL are in the sub-limit district, and thus their sub-edge currents ought to be low for lower static power scattering.

Table 1: Result Comparison

Sr. No.	Parameters	Previous Work	Proposed Work
1	Design	DWA14T [Dynamic Loop-Cutting Write Assist]	WWL12T [self-Refreshing logic-based Write World-Line]
2	Area	1071 nm	686 nm
3	Read energy consumption	0.6V	0.164 V
4	Write energy consumption	0.6V	0.146 V
5	SRAM Cells	37	30
6	V_{DD} (V)	0.7V	0.6V

Table is showing comparison in terms of supply voltage, read and write energy consumption on the other hand stability and area. When read and write energy consumption value low than its stability high. Supply voltage is less means this circuits save power utilization. Less area is cause to low delay. Therefore proposed RFID WWL12T SRAM design achieves significant better performance than existing 12T design.

V. CONCLUSION

This research presents, a novel 12T RFID-SRAM memory cell for mitigating soft error in 65-nm CMOS commercial technology for RFID application is proposed. The main contribution of the proposed RFID memory cell is that not only can it tolerate single node upset, but it can also provide effective multiple-node upset protection. 1000 MC simulations are also carried out, and the obtained simulation results clearly confirm that process variation does not affect its SEU robustness. Simulation results shows that the proposed work achieves the significant improvement in terms of the performance parameters.

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