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A 13.42ps Resolution, Low-Power Time-to-Digital Converter and 0.519fJ Energy-Efficient Novel Voltage-to-Time Converter for High-Speed Time-Based ADC Application

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Abstract : This Voltage domain ADC architectures require high gain and high bandwidth opamps to amplify the signal for successive stages. The opamp design gets a bit challenging due to noise, small gain and lower overdrive voltage. Due to these limitations, the inclination shifted towards high-speed converters which don't require opamps. Time based Analog to Digital Converters (TBADC) is one such category of circuits. TBADCs are constituted from VTC followed by TDC with an encoder in the end. This work is concerned around the design of a high-resolution time to digital converter (TDC) and proposing a novel high-speed, low power consuming voltage to time converter (VTC) circuit. Both the circuits were implemented in Cadence Virtuoso EDA tool version 6.1.7 and Spectre was employed for running the simulations. TDC circuits had resolution of 13.425 ps and consume power of 1.873 µW. Process corner analysis and Monte Carlo analysis were performed on VTC design to determine worst possible deviations in performance. The proposed VTC exhibited delay of 23.79 ps with power consumption of 21.83 µW at 1 Volt. The presented TDC and VTC circuits can be used to design high-speed time-based Analog to Digital Converters.

Index Terms **-high speed, high resolution, low power design, time to digital converter, time-based analog to digital converter, voltage to time converter.**

I. INTRODUCTION

Voltage-domain ADCs consist of comparators and a feedback system, followed by a sample-and-hold circuit, used to determine the corresponding digital code for an analog input signal. However, they require high gain and high bandwidth opamps to amplify the signal for successive stages. Process of designing opamp gets a bit challenging due to noise, small gain and lower overdrive voltage [1]. Due to these limitations, there has been an increasing demand for high-speed converters, which do not require opamps. Time-based ADCs are one such kind of architectures [2]. TBADCs perform the conversion of analog signal to a digital code in two steps; an analog signal is initially converted to a time signal using a voltage-to-time converter, which is then converted into a digital code using a time-to-digital converter.

TDCs have been extensively used in ADCs and laser time of flight (ToF) measurements where transit time of laser pulse is measured [3]. Efforts were also invested in designing TDCs which were capable of having noise immunity but that came at the cost of high-power consumption [4]. Owing to the recent developments of noise immune TDCs, the digital phase locked loops (DPLLs) too attained an upgrade in noise performance [5]. Multichannel TDCs made by counter and delay line exhibits good temperature stability. It did not require any additional calibration circuitry as the resolution was locked to external reference crystal [6]. Introduction of multiple conversion levels can help in achieving wide measurement range at low resolution. This design involved multi-level conversion. The approach saw the use of differential delay cell for improving time resolution [7]. Adding and subtracting input signals has also been proposed in time domain signal processing. The design involved a time register for performing mathematical calculations with time signal [8]. Delay line TDC was used for high speed and clock was used to synchronize the pipeline stages. The sub-picosecond TDCs are widely used currently. Proceeding a step further to these designs, a novel TDC design proposed lately

which computed difference between two consecutive delay time and used that information to generate digital code [9]. However, all these TDC designs had a drawback of high-power consumption.

Analog input voltage to time conversion in time-based ADCs is performed by Voltage to Time Converters, also known as VTCs. A number of VTC designs have been proposed till date as discussed ahead. In [10], VTC circuit is proposed to operate at 5 GS/s. However, the circuit consumes high power of 3.6 MW and has a small input dynamic range. In [11], a VTC circuit is proposed at which the input signal is compared with a voltage ramp. Although this design in Reference consumes low power, its operation is limited to small sampling frequency. In [12], a VTC is proposed that consists of a track and hold circuit, level shifter and a pulse shape restorer which improves the linearity of the VTC. However, this design suffers from high power consumption. Takauji proposed a current starved inverter made up of dual stage structure which improved the overall dynamic range. Yi too proposed a folding architecture based VTC design for implementing TBADC [13]. However, both these circuits consumed high power.

Osheroff presented a current mirror structure to achieve high linearity and high speed but had disadvantage of high-power consumption. Jia proposed a VTC circuit based on Current starved Inverter which employed folded structure [14]. Linearity of the circuit was improved but the power consumption rose up. In reference [15], a modified VTC is presented to increment linearity but the input dynamic range is limited to 400 mV along with the disadvantage of high power consumption. A digital time-based ADC is proposed to reduce the chip area but still the power consumption remained relatively high [16]. All these circuits had a common drawback of high-power consumption. The objective of this paper is to design a low power, high resolution time to digital converter along with proposing a novel voltage to time converter circuit design equipped with low propagation delay and high energy efficiency.

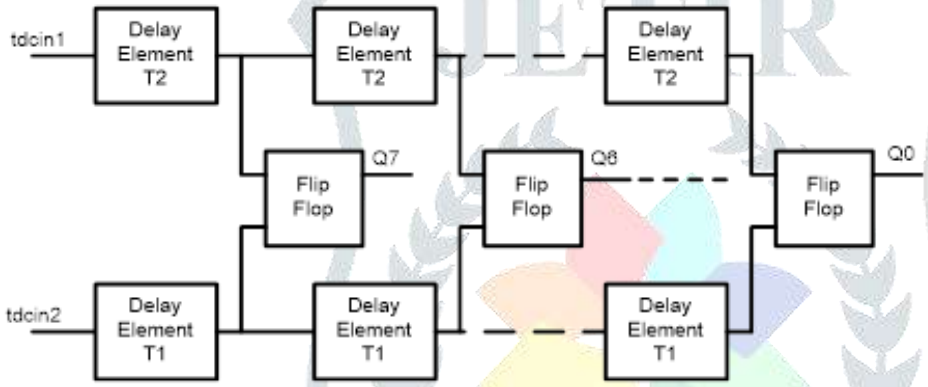

Figure 1: Block diagram of Vernier TDC circuit

II. TIME TO DIGITAL CONVERTER CIRCUIT

This section elaborates about the first circuit concerned with Time based ADCs, that is Time to Digital Converters. Vernier time to digital converter (VTDC) architecture has been considered for this work. The propagation delay $\boldsymbol{\tau}$ of a single delay element could be expressed as

$$\tau = \mathrm{C} * R \tag{1}$$

where:
C = load capacitance
R = resistance offered by circuit.
Resistance R can be elaborated by equation 2

$$R = V/I \tag{2}$$

where:
V = input voltage,
I = output current.

The current flowing at the output of MOSFET in saturation region is given by (5), which helps us further extend above equations and hence, the propagation delay of delay line.

$$I = K * (W/L) * [Vgs - Vth]^2 \tag{3}$$

$$R = [V * L] / [K * W * (Vgs - Vth)^2] \quad (4)$$

Analyzing the values from (1), (2), (3) and (4), we get the propagation delay value of the circuit as shown below

$$\tau = [C * V * L] / [K * W * (Vgs - Vth)^2] \quad (5)$$

where:
K = process transconductance parameter,
W = width,
L = length,
Vgs = Gate to Source voltage,
Vth = Threshold voltage,
$\boldsymbol{\tau}$ = propagation delay.

A detailed discussion on the vernier TDC follows ahead. It consists of two delay lines namely upper and lower. The two delay lines are constructed using CMOS inverters with different transistor dimensions in such a way that they have separate delay times T2 and T1. Resolution of vernier TDC is expressed using the below equation.

$$\text{Resolution} = T2 - T1 \quad (6)$$

An 8-bit TDC design has been presented here as shown in figure below. Input signal "tdcin1" is fed to the upper delay line with propagation delay T2 while sampling signal "tdcin2" is fed through the lower delay line with propagation delay T1. The difference of these two delay lines reaches the flip flops attached after every delay element. Flip flops have the function of capturing the status of the two delay lines. The outputs of the flip flops can be later on fed as an input to the encoder ahead for converting time signal to digital codes.

III. VOLTAGE TO TIME CONVERTER

VTC is an analog circuit, which converts an analog (continuous time and amplitude) signal to a time (continuous time and discrete amplitude) signal. Out of the various ways to implement VTC, current starved inverter (CSI) based VTCs are the most commonly used ones. It relies on converting an analog input signal to a time signal by charging and discharging a capacitor. Initially, four topologies of XNOR logic circuits were studied and compared. Then the optimal one out of those was taken into consideration for usage in Voltage to Time Converter circuit. The following sub-section deals with exclusive-NOR circuits.

A. XNOR

Two-input XNOR logic gate have been considered for this work. The output is HIGH when both of the inputs are similar, either HIGH or LOW. Otherwise, the output remains LOW. Four types of exclusive-NOR logic gates were explored for the purpose of this work, namely CMOS, TGL (Transmission Gate Logic), PTL (Pass Transistor Logic) and hybrid novel design [17]. The circuit schematics of these XNOR topologies are shown in figure below. Performance analysis was done in Cadence Virtuoso (mentioned in section 4 of this paper) so as to determine the optimal design to be considered for being employed in implementing high speed VTC circuit. The parameters considered were total power (combination of dynamic as well as static), delay, Power Delay Product or PDP. Performance comparison of the XNOR topologies has been tabulated in table 1.

Table 1: Parameters comparison of XNOR circuits with power supply of 1 Volt at 27^0 C

Parameters	**Conventional XNOR**	**PTL XNOR**	**TGL XNOR**	**Novel XNOR** [17]
Delay (ps)	42.198	42.647	22.3602	8.50525
Transient power (nW)	252.276	109.423	176.545	43.6787
Static power (nW)	25.5687	15.493	25.5318	0.000002
Total power (nW)	277.845	124.916	202.077	43.6787
PDP (aJ)	11.7245	5.32729	4.51848	0.37149
Transistor count	14	6	8	5

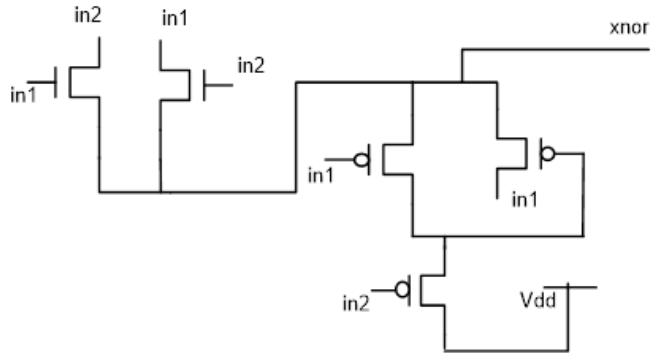

Figure 2: Circuit schematic of Novel XNOR logic gate [17]

XNOR circuits have been considered in a form that the complements of the inputs are not available, and henceforth, have to be obtained by passing them through an inverter circuit. The comparison table data showed that the novel hybrid design had the least propagation delay (8.5 picoseconds) and consumed lowest power (43.6 nanowatts) among all the designs. It also emerged as the most energy efficient design with figure of 0.37 x 10^{-18} Joules. The added advantage was the usage of minimum number of transistors (5) whereas on other hand conventional XNOR used 14, PTL used 6 and TGL topology used 8 transistors. Therefore, the novel hybrid XNOR design emerged out to be the optimal XNOR for high speed VTC circuit.

B. RISE CIRCUIT

Rise circuit consists of pmos PM0, PM1, PM2 and nmos transistor NM0 along with a load capacitance C0. Inverted clock signal is fed to the inverter structure composed of PM2 and NM0 as shown in figure 3. The upper half of rise circuit has PM1 with input voltage at its Gate terminal whereas a bias voltage is applied to Gate of PM0. Bias voltage keeps transistor PM0 permanently on. The addition of PM0 is done to facilitate the charging of capacitor C0 whenever Vin gets below the threshold voltage of PM1, resulting in turning it off.

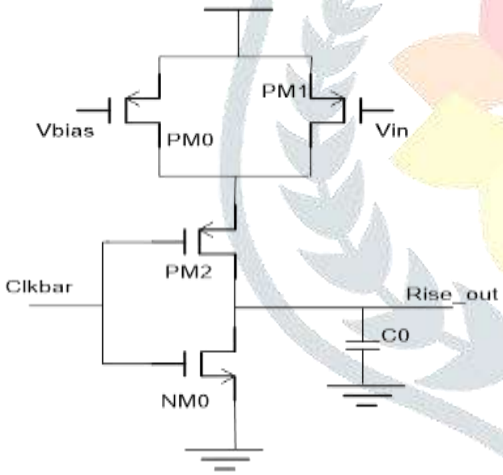

Figure 3: Rise circuit schematic

C. FALL CIRCUIT

Fall circuit is very much constructed on the lines of CSI structure. The only modification is addition of a driver transistor with a bias voltage controlled nmos transistor NM1 as shown in figure 4. The bias voltage keeps transistor NM1 permanently on. Clock signal is provided as a switching signal to turn on either of the two paths, that is charge or discharge. LOW signal at clock turns on PM3 and C1 starts charging while HIGH clock turns on NM3, hence, paving the way for the capacitor to start discharging.

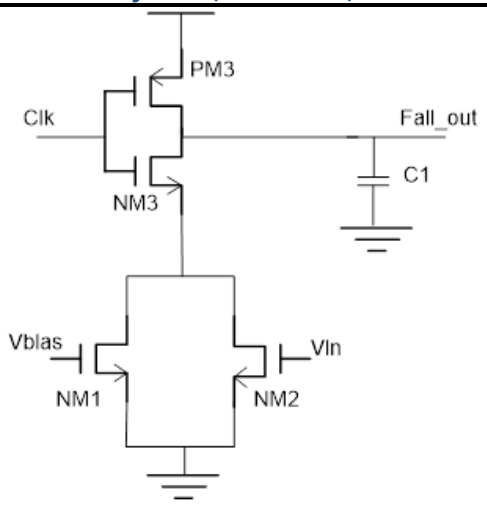

Figure 4: Fall circuit schematic

D. PROPOSED VTC CIRCUIT

The proposed VTC circuit is shown in the above figure. It comprises of three sub-circuits namely: rise circuit, fall circuit and xnor circuit. A series of three inverters have also been employed in order to invert the clock signal used, which needs to be fed into the rise circuit. The outputs from the rise circuit and fall circuit are fed as an input to the xnor circuit which ultimately gives a pulse width modulated waveform, referred to as the output of Voltage to Time Converter circuit.

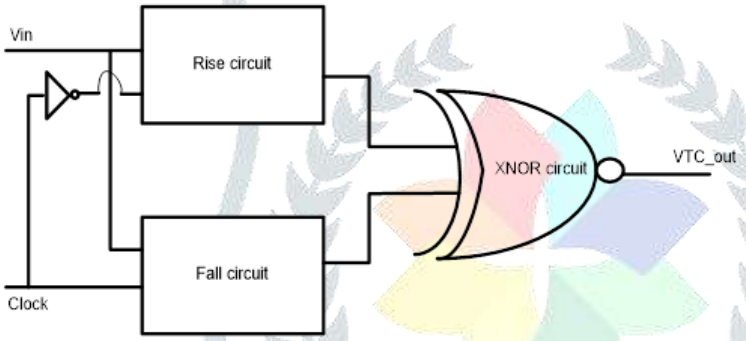

Figure 5: Proposed VTC circuit block diagram

IV. RESULTS AND DISCUSSION

All the circuits presented in this work have been implemented using Cadence Virtuoso EDA tool and the simulations have been carried out using Spectre. Vernier time to digital converter resolution was obtained by taking the difference between the resolutions of the upper and the lower delay lines. Upper resolution was 40.43 ps while the lower resolution was 27.01 ps. Hence the net resultant resolution of vernier TDC came out to be 13.42 ps. The output waveform of this converter is shown in figure 7 below. Here, “tdcin1” indicates the start signal and “tdcin2” is stop signal. The other notations “q7” to “q0” are the flip flop outputs, which are placed to capture the status of delay line elements.

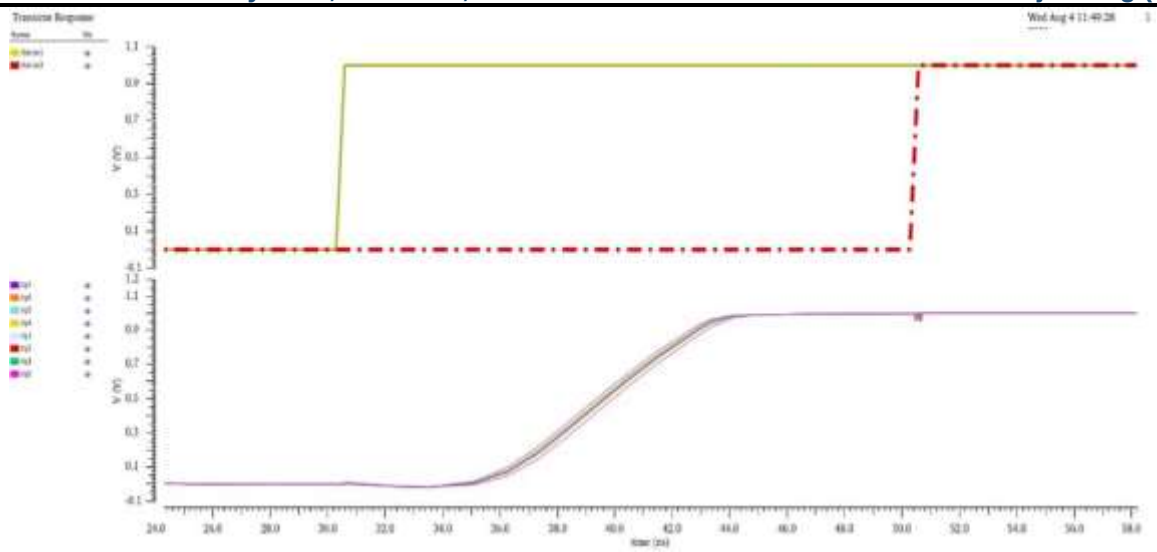

Figure 6: Output waveforms of vernier TDC with respect to input signals

The proposed Voltage to Time Converter circuit was simulated using gpdk45 technology node in Cadence Virtuoso software. Analog input signal fed in as input along with a sampling signal into the VTC block, which provides a pulse width modulated output time signal. The output waveforms associated with VTC is illustrated in figure 8. Process corner analysis indicates the circuit performance degradation or improvement in cases where either pmos or nmos or both transistors operate slow / fast. This results in five primary types of process corners namely slow-slow (SS), slow-fast (SF), nominal-nominal (NN), fast-slow (FS) and fast-fast (FF). NN process corner is also known as typical-typical (TT). VTC, in this work, exhibited mean power consumption of 22.45 micro-watts with a small deviation of 4.404 micro-watts.

Table 2: Performance comparison of Time to Digital Converter circuits

Parameters	**ISSCS** [18]	**ICCE** [19]	**TCSII** [20]	**MEJ** [21]	**TVLSI** [22]	**This work**
Architecture	Vernier	DLL	Ring oscillator	Dual DLL	TDL	**Vernier**
Process Technology (nm)	65	65	130	180	90	**90**
Verification method	Simulation	Simulation	Measure -ment	Measure -ment	Measure -ment	**Simulation**
Resolution (ps)	6.15	2.0	43.2	15.0	30.0	**13.42**
Power Consumption (mW)	2.5	69.7	1.72	75	2.22	**0.001873**

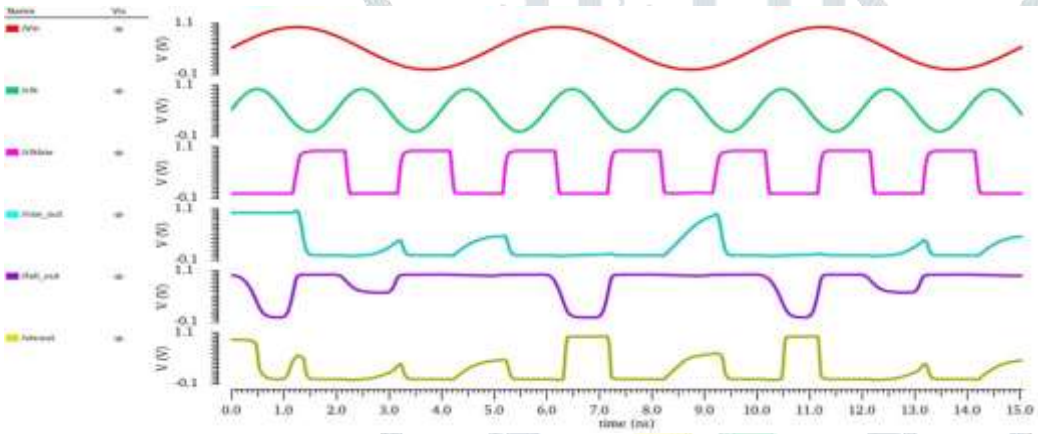

Figure 7: Output waveform of Voltage to Time converter with input and sampling signals

Monte Carlo simulations give the information on how much variation the concerned circuits can undergo when they are repeatedly used to carry out computations. This analysis provides mean value along with the standard deviation of the performance parameter for a particular circuit. The Monte Carlo simulations of proposed Voltage to Time Converter circuit are illustrated as follows. Figure 9 depicts the Monte Carlo simulation graph of total power consumption for 500 points. The mean power consumption was 21.6266 µW and the deviation observed was 928.103 nW. Similar analysis was carried out for propagation delay of voltage to time converter for 500 points whose mean value was -285.092 picoseconds (negative sign due to clock signal preceding input voltage signal at several points during Monte Carlo run) and the deviation observed in delay was 347.39 picoseconds.

Table 3: Process Corner analysis summary of VTC

Parameter	**Mean**	**Standard Deviation**
Transient power (µW)	18.36	2.021
Static power (µW)	4.082	2.445
Total power (µW)	22.45	4.404
Delay (ps)	-239.5	321.3
Power Delay Product (fJ)	-4.391	6.138

Table 4 compares the performance of proposed Voltage to Time Converter circuit with other previously published VTC designs. The propagation delay of presented circuit is the least, making it a high-speed design with delay of 23.79 picoseconds. It is followed closely by circuit proposed by Puglisi in [25] with 70 picoseconds delay. Hassan's VTC consumes least power of 0.35

microwatts. Power Delay Product (PDP) illustrates energy efficiency of circuits. The proposed VTC is the most efficient in terms of energy with figure 0.519 femto-joules followed closely by Bayoumi's VTC reported in [23].

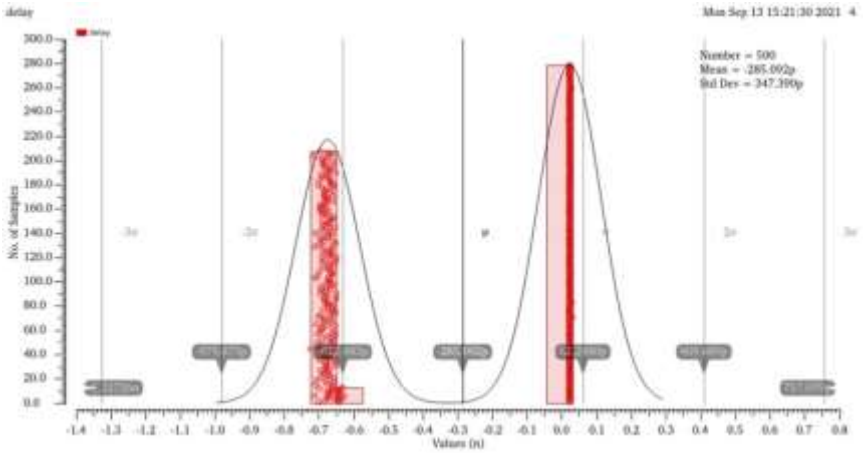

Figure 9: Monte Carlo Simulation of propagation delay of proposed VTC

Table 4: Performance Comparison of Voltage to Time Converter circuits

Parameters	Bayoumi [23]	Miki [13]	Hassan [24]	Jia [16]	Puglisi [25]	**This work**
Technology (nm)	65	28	130	65	65	45
Supply voltage (V)	1	1.2	1	1	1	1
Delay (ps)	96	128	$237x10^3$	102	70	23.79
Total Power consumption (µW)	159	180	0.35	477	1100	21.83
Power Delay Product (fJ)	15.26	23.04	82.95	48.65	77	0.519

V. CONCLUSION

This article presented low-power consuming Vernier Time to Digital Converter circuit with a resolution of 13.42 ps. An energy-efficient novel design of Voltage to Time Converter, implemented at 45nm technology node was also proposed in this paper. The presented circuits were compared with previous published works. Process corner analysis and Monte Carlo analysis of VTC circuit were also carried out to determine the deviation of circuit performance in non-ideal situations. The deviation of total power consumption and PDP are within acceptable bounds. Implemented in 45nm technology, the proposed VTC occupies an area of 188.59 μm^2. Time to Digital Converter and Voltage to Time Converter circuits find application in designing of time-based Analog to Digital Converters. An encoder, such as thermometer to binary, needs to be attached additionally, to the TDC circuit presented in this work, for implementing a time-based ADC circuit. The novel VTC design can be effective in designing a high resolution and low power consuming circuit for high-speed applications.

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