JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

4-BIT COUNTER DESIGN USING DIFFERENT LOW POWER DESIGN STYLES

[1]Preeti Sahu, [2]Dr. Payal Bansal

[1]Research Scholar, [2]Assistant Professor
[1]Electronics and Communication Engineering,
[1]Poornima University, Jaipur, India.

Abstract : In a simple word counters can be defined as a digital sequential circuit which used to counting clock pulses. It has a widest application in the flip-flop circuit. In the digital world counters also known as a device which used to store the number of time for processing a particular event with using clock signal. This paper enumerated with designing of 4-bit Up-down counter with different low power technologies. The circuit has been implemented on FPGA using Xilinx-14.7. Power Optimization has been done through DSCH-Microwind-3.5 software tool. All the parameters has compared with implementing the circuit using different techniques.

Index Terms **- Low Power concept, Counter circuit, Up-Down Counter, Clock Gating, Power Gating, Gate-Diffusion Input, Implementation of Up-Down Counter circuit, Parameters optimization in Counter circuit.**

I. INTRODUCTION

VLSI/ULSI has important role in the Nano-electronics and microelectronics world. These are used in many applications such as RF design, RISC processors, MEMS technology, Smart system design, IoT and IIoT system designing. When we used to design VLSI/ULSI chips 3 main parameters have to be remember named as Power, Area, and Delay. Generally power consumption is increased in the electronic system and the integrated circuits in particularly manner because of their complexity due to large number of circuits on a single chip. So there is needed design a circuit with low power consumption. The optimization is described in terms of generating the best design according to goal.

In VLSI system designing mostly three sources of power dissipation discussed namely as, Dynamic or circuit-switching power, Static Power and Short- circuit Power. Dynamic power is a very simple approach to estimate energy consumption in a CMOS circuit. Dynamic power is caused by switching activities of the circuit. Increment of dynamic power in circuit is depends on the higher operating frequencies which leads more frequent switching activities in the circuit. Dynamic power of circuit is described as given expression, where energy consumption in CMOS circuits is estimated by the capacitance to be switched. The charging and discharging of capacitance is known as most significant source of dynamic power dissipation in VLSI circuits.

$$P_D = C.V^2.F$$

Static power is related to the changes in states of the circuits, means that the static power is due to the changing of circuit states that are 0 to 1 or 1 to 0 rather than switching activities. In CMOS circuit leakage power is only source of static power dissipation. Low power consideration should be applied in digital CMOS technology at all levels of design abstraction and design activities. A low power design system also affects other features such as reliability, design cycle time, testability and design complexity. Chip area and speed are the major trade off considerations in designing of VLSI system.

II. PROPOSED SYSTEM

A. Counter Circuit:

Cascade network of flip-flops are used to construct counter circuit usually. They are used widely in digital circuit design and manufactured on various IC which incorporated as a part of larger digital circuit. Generally, counter is known as a sequential logic circuit which has a clock input signal and a group of output signals which represents an integer value. Implementation of Counters can be done in variety of ways, such as MSI and LSI integrated circuits, within ASICs, as general-purpose counter and timer peripherals in microcontrollers, as construct the shift Registers, and as IP blocks in FPGAs. Figure 1, has shown in below which clearly explained the architecture of a simple 4-bit counter circuit using D-flip-flops. The circuit used 4 D-Flip-flops which have clock signal and the inverted output has been provided to next circuit as their clock signal.

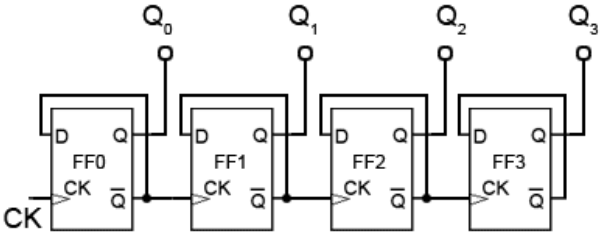

FIG 1: COUNTER CIRCUIT USING D-FLIP-FLOP

THE CIRCUIT GENERATED FOUR OUTPUT SIGNALS AS COUNTING THE PULSES FROM 0 TO 14 AS THEIR OUTPUT SIGNALS Y. THE NEXT SECTION DESCRIBED THE UP-DOWN COUNTER CIRCUIT, ITS ARCHITECTURE AND WORKING. THE OUTPUT SIGNALS Q0, Q1, Q3 AND Q4 OF THE CIRCUIT REPRESENT THE VALUES 2^3, 2^2, 2^1 AND 2^0, AS THE BINARY CODED VALUES 8421 RESPECTIVELY. THE SCHEMATIC DIAGRAM OF COUNTER CIRCUIT HAS SHOWN IN FIGURE 2 AS GIVEN BELOW.

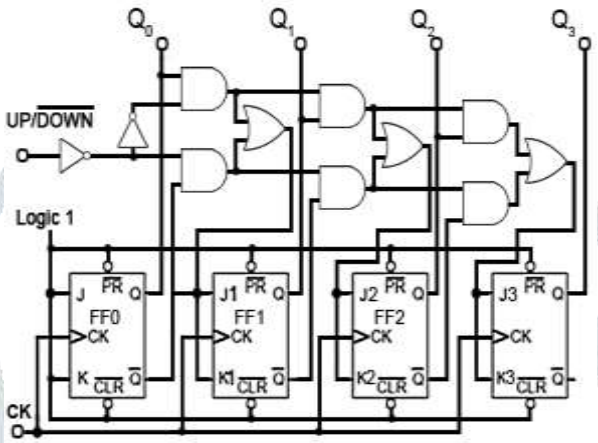

Fig 2: Architecture of 4-bit Up-down Counter circuit

Figure 2 as shown called as UP/DOWN counter which can be used to make a single counter that count either up or down, depends on value of logic state UP/DOWN signal. Working of the Up-Down Counter can be understood simply through table 1 as shown below. Up counter and down counter is combined together to obtain an UP/DOWN counter. A mode control (UP/DOWN) input is also provided to select either up or down mode. A combinational circuit is required to designed and used between each pair of flip-flop in order to achieve the up/down operation.

The table explained as the truth table of Counter circuit which counts the (15) digits from 0-14 to corresponding inputs at each clock pulse.

TABLE-1: TRUTH TABLE OF UP-DOWN COUNTER CIRCUIT

CLK	Reset	Up/down	O/P=Y			
			A	B	C	D
1	1	1	0	0	0	0
1	0	1	1	1	1	1
1	0	1	1	1	1	0
1	0	1	1	1	0	1
1	0	1	1	1	0	0
1	0	1	1	0	1	1
1	0	1	1	0	1	0
1	0	1	1	0	0	1
1	0	1	1	0	0	0
1	0	1	0	1	1	1
1	0	1	0	1	1	0
1	0	1	0	1	0	1
1	0	1	0	1	0	0
1	0	1	0	0	1	1
1	0	1	0	0	1	0
1	0	1	0	0	0	1
1	1	1	0	0	0	0

Clock signal is used to operate the circuit, Reset is used as control input which restart the counting at logic value '1' and output continued at Reset will be '0'. The Up/DOWN input used to select the inputs for Up or Down counting during operation.

III. PROPOSED METHODOLOGY

In this paper the proposed system has been designed and implemented with 3 different types of technology for parameters optimization and Power Minimization. These 3 techniques named as Clock Gating, Power Gating and Gate Diffusion Input (GDI). The gating techniques used widely in VLSI/ULSI Chip designing at Low Power, Clock Gating Technique improve the power and delay of the circuit as reduce its switching activities, Power Gating Technique used for minimize the static power as reduction in Leakage power of the circuit and GDI technique used to design Faster ICs as increase the speed of the circuit which make its performance faster than conventional design.

A. Clock Gating:

The Clock gating technique minimizes the power of circuit with reducing clock switching activities and the Power Gating scheme minimizing the power with adding sleep transistors as header and footer to the circuit. In this paper USR implemented using Clock Gating scheme which is shown in figure 3 & 4 as below. A basic block diagram of CG scheme is shown in figure 3. Where D-FF circuit is used to generate Gated Clock signal and then it is provided to the main circuit as driver signal. When 'En' is 1, Clk signal gated with D-FF circuit otherwise the circuit is off.

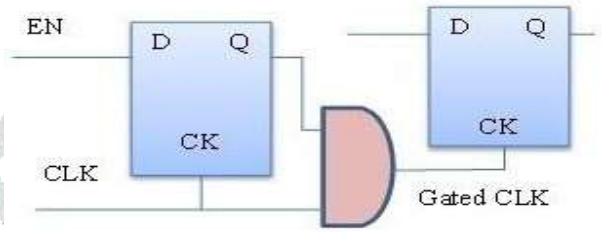

FIG 3: CLOCK GATED CIRCUITS

AND gate based CG implementation is easy to design and implementation for the circuit, a basic form of AND gate based CG scheme is shown in figure as below where AND gate is used to generate gated clock signal and this gated clock signal provided to circuit as driver signal. AND gate based CG scheme is shown in figure 4 as below.

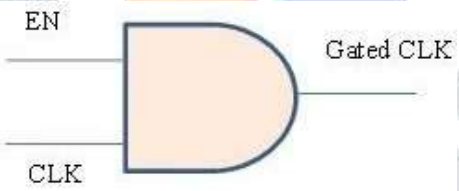

Fig 4: CG implementation with Gate based Technology

Clock gating is widely used for dynamic power reduction of the circuit and little bit of static power also. Power Minimization also increases the speed.

B. Power Gating:

The power gating circuit has 2 MOS transistors named as PMOS and NMOS as their header and footer respectively. A basic Power Gating circuit is shown in figure 5 as given below. PMOS transistor is used as header circuit of the implemented logic and NMOS circuit is used as footer circuit of implemented logic circuit. These header and footer circuit reduce the leakage current when circuit is not in used and minimize the overall power of the circuit.

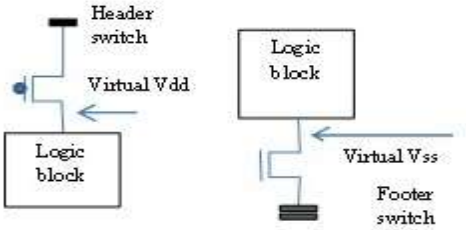

Fig 5: Power Gating Circuit

C. Gate-Diffusion-Input:

The gate diffusion input technique is the modified pattern of sleep transistor technique which reduce the delay and glitches form the circuit and make it faster. The basic GDI cell is shown in figure 6 which consider CMOS inverter with sleep transistor technique.

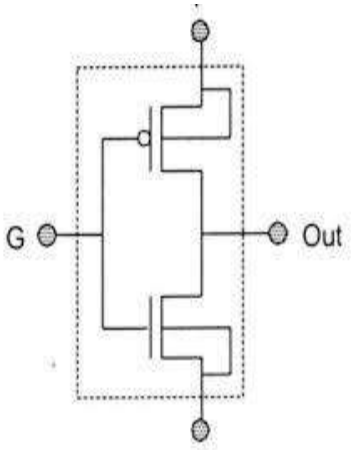

Fig 6: Basic GDI Cell

The basic GDI cell performs different operations to corresponded inputs G, P and N. This paper included the 4-bit counter circuit implementation with all 3-technologies and optimizes the parameters with all technologies.

IV. EXPERIMENTAL ANALYSIS

In this section the circuit implementation and simulation work is defined for designing low power 8-bit Universal shift register. Experiment of circuit is performed by XILINX-14.7 software tool with VHDL coding. I-Sim simulator is used to perform the simulation process and got the waveforms as corresponded output.

Also DSCH Micro-wind 3.5 Tool used to optimize the parameters and layout generation through their output and input signals.

The circuit layout has been drawn on 90nm and 45nm CMOS scaled Technology. Operating frequency selected as 5 GHz, Supply voltage is 5V and the input current is considered at0.520mA. This section is included the implementation of proposed system using different power minimization techniques. Figure 7 shown in below which is circuit diagram of Conventional design.

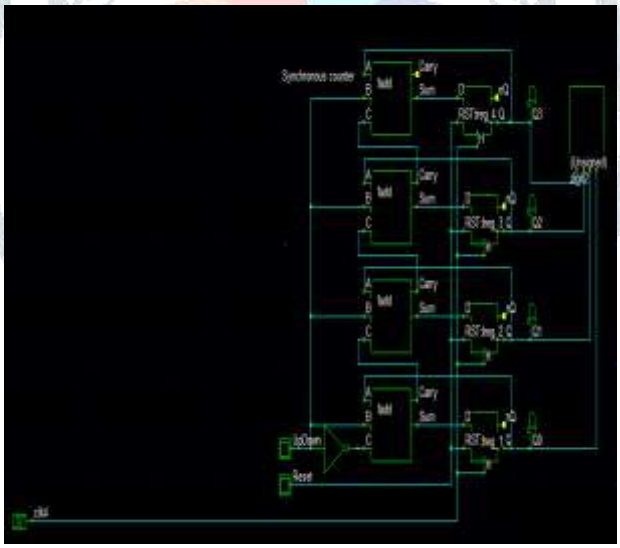

Fig 7: 4-bit Up-Down Counter Circuit

Figure 7, shown as above, having 3 input signals named as Clock, reset and UP/DOWN and a 7-segment display has been used as output display.

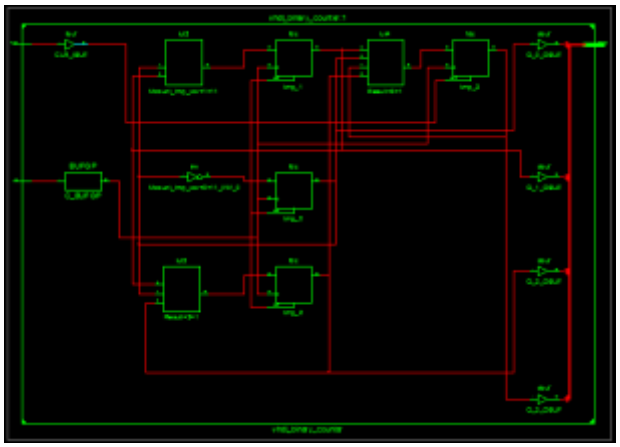

Fig 8: Technology view of 4-bit Up-Down Counter Circuit

Figure 8, shown as above is known as RTL schematic, which explained, all interconnects of the inputs and output nodes clearly. It is generated with Xilinx tool.

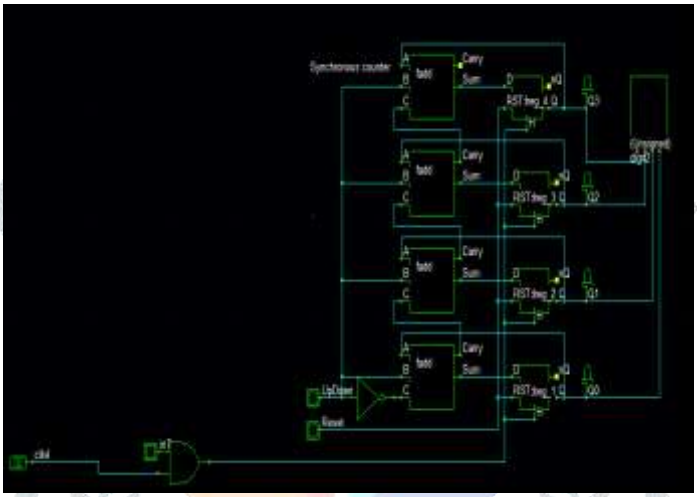

Fig 9: 4-bit Up-down Counter Circuit with CG Implementation.

The clock gated implementation of the proposed system is shown in figure 9 as above. Here the proposed system is implemented using AND gate based Clock Gating Technique which has better improvement in reduction of switching activities and delay from the circuit. Area is considered more than conventional design because of the external clock gating circuit.

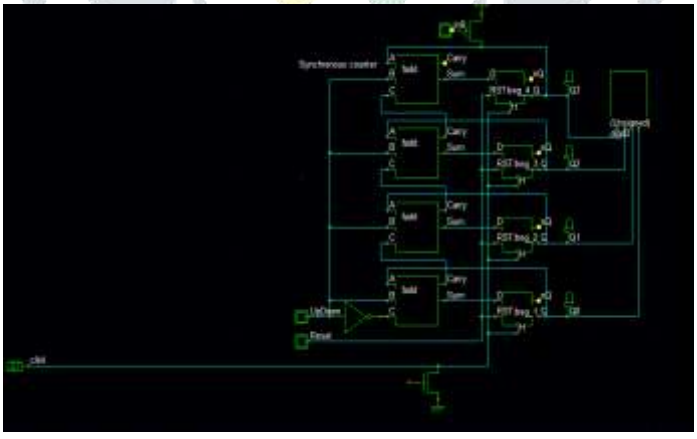

Fig 10: 4-bit Up-down Counter circuit with PG Implementation

The Power gating implementation of the proposed system is shown in figure 10 as above. It considered a PMOS transistor as their header and NMOS transistor as their footer circuit. The circuit has more area due to adding extra transistors but benefits to reduce leakage power in the circuit. So static power is less and overall power minimized through Power gating implementation. The next implementation has been done with GDI technique to improve speed of the circuit. A GDI based Counter circuit is shown in figure 11 as below.

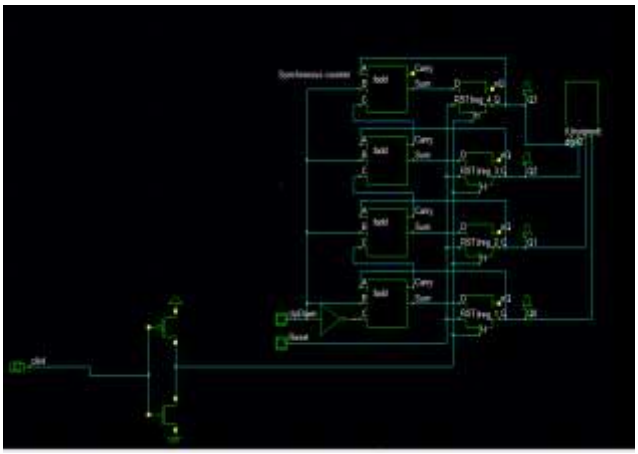

Fig 11: 4-Bit Up-down Counter circuit with GDI Implementation

A simple GDI based cell has been added to proposed system and simulate for faster speed. In the Next section Simulated results has been considered with corresponded input signals and also parameters optimization has been done successfully which is shown in tabular form.

V. RESULTS AND DISCUSSION

This section has been defined the Results which provided after simulating the circuit with their corresponded input signals. The power has been calculated with X-Power Estimator (XPE) tool. Results optimized in proposed system at 5GHz frequency and 1V supply voltage which explained in tabular forms. Figure 12 to 15 has shown the simulated waveform results of proposed system with different design styles.

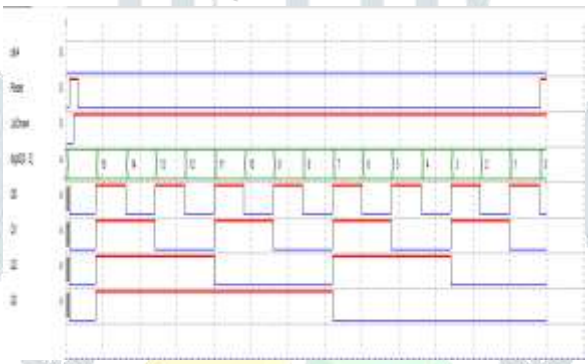

FIGURE 12: SIMULATION RESULT OF CONVENTIONAL 4-BIT COUNTER CIRCUIT

Simulation Results of Conventional Counter design is shown in figure 12 as above. When the clock pulse provided and Up/Down signal has logic '1' value than operation of counter started and it counts the 15 to 0 digits.

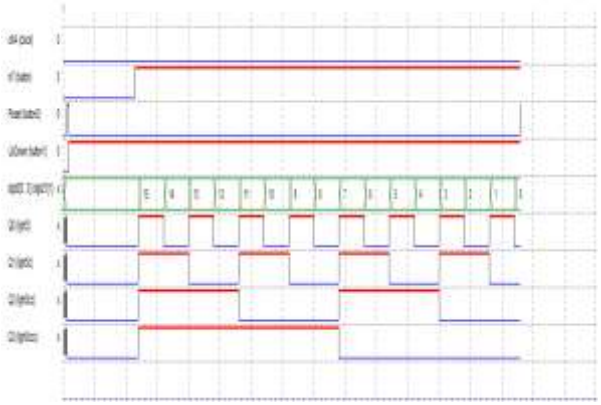

FIGURE 13: SIMULATION RESULTS OF PROPOSED SYSTEM WITH CG IMPLEMENTATION

A SIMULATION RESULT WITH IMPLEMENTING CLOCK GATED TECHNIQUE TO THE PROPOSED SYSTEM IS SHOWN IN FIGURE 13 AS ABOVE. HERE AND GATE BASED CLOCK GATED IMPLEMENTATION HAS DONE. CIRCUIT STARTS THE OPERATION ONLY WHEN EN SIGNAL OF CLOCK GATED CIRCUIT HAS LOGIC '1' VALUE. OTHERWISE THE CIRCUIT WILL BE IN OFF CONDITION AND DIDN'T PROVIDE ANY CLOCK SIGNAL TO FURTHER PROCESS OF PROPOSED SYSTEM.

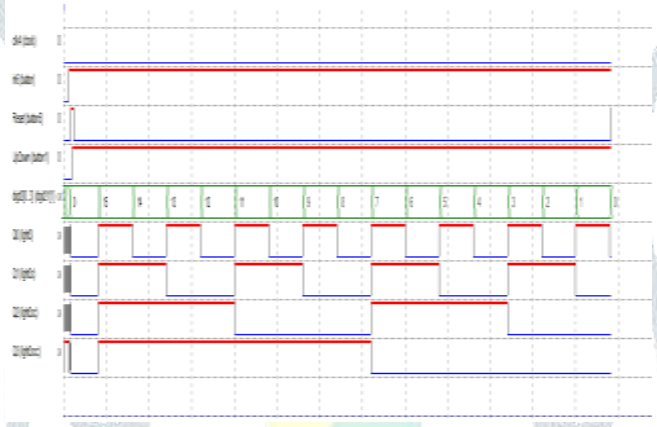

Fig 14: Simulation Results of Proposed System with PG Implementation

Power Gated implementation of the proposed system is shown in figure 14 as shown above. The Power Gated implemented counter circuit has less power consumption with reduction in leakage power. When circuit is inactive or not working condition the circuit will be off through header and footer circuits and no leakage has been placed which causes leakage reduction in the circuit.

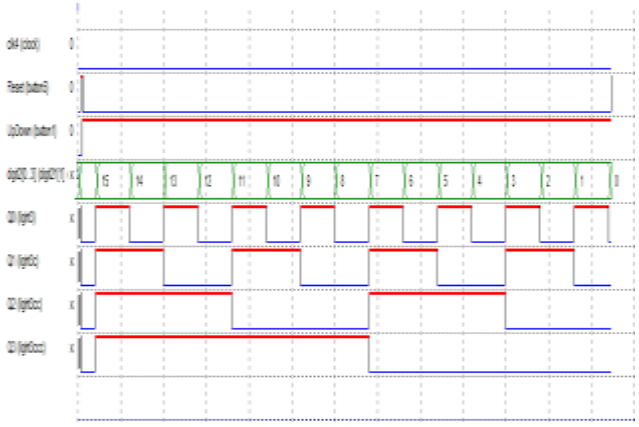

Fig 15: Simulation Results of Proposed System with GDI Implementation.

The GDI implementation of the proposed system has been successfully done completed and simulation waveform results shown in figure 15 as above. The GDI implementation improves the speed of the circuit and reduces the delay.

The parameter optimization results with different implementation shown in tabular forms as given below. Table 2, provided the Power optimization results through the CG, PG and GDI implementation and compared all with Conventional proposed system.

Table-2: Power Optimization in 4-bit Up-Down Counter Using different Technologies

Proposed Circuit	Power(mW)
4-bit Up-down Counter	**0.498**
4-bit Up-down Counter with CG Implementation	**0.374**
4-bit Up-down Counter with PG Implementation	**0.499**
4-bit Up-down Counter with GDI Implementation	**0.578**

VI. CONCLUSION

As above results, proved that CG scheme is better for minimizing power in the circuits. This scheme also has better solution for minimize the area utilization by devices and delay. With implementing power gating scheme shift register has been improved the power, delay and area utilization. Power has been improved by 40.65% with implemented design. Area increased by 4.76% but delay has been improved by 12.93%. Requirement of Low power devices are increases much more in IC world. So PG scheme has better solution in this way. Proposed and implemented design considers less area with minimize the leakage in the circuit. The proposed universal shift register design achieved low power and improved performance of the circuit. Speed of the proposed Counter system will be high than conventional Counter design.

REFERENCES

[1] Preeti Sahu, Dr. Santosh Kumar Agrahari, (2021), Optimization of Parameters in 8-Bit ALU circuit with Clock Gating Technique, in international conference ICGTET-2021, IEEE.

[2] Preeti Sahu, Dr. Santosh Kumar Agrahari, (2021), Power and Performance Optimization in 16- Bit ALU using Power Gating, in IC-Research-2021 (International Conference on Recent Trends in Electrical, Electronics & Computer Engineering for Environmental and Sustainable Development).

[3] Namrata Joshi, Ravi Kumar Jangir, (2019), Design of Low Power and High Speed Shift Register, IOSR Journal of VLSI and Signal Processing.

[4] Vandana Niranajana, (2018), "Low power and high performance shift registers using pulsed latch technique", ICTACT journal on microelectronics, volume: 03, issue: 04.

[5] S.A.Sivakumar, R.Sowmya, (2016), "Design of low power Universal Shift Register Using Pipe Logic flip flops", International Journal of Advances Research in Computer and Communication Engineering (IJARCCE).

[6] K. Anusha, A. Deepika, (2016), "Design and Implementation of Novel 8-bit universal Shift Register using Reversible Logic Gates", International Journal of Innovation in Engineering and Technology (IJIET).

[7] Saranya.M, V.Vijayakumar, 3T.Ravi, 4V.Kannan, (2013), "Design of Low Power Universal Shift Register", International Journal of Engineering Research & Technology (IJERT) Vol. 2 Issue 2.

[8] Paliwal, P., Sharma, J. B., & Nath, V. (2019). Comparative study on FFA architectures using different multiplier and adder topologies. Microsystem Technologies, 1-8.

[9] S. Daboul, N. Hahnle, S. Held, and U. Schorr, (Dec, 2018), "Provably Fast and Near Optimum Gate Sizing," in IEEE Trans. on Computer-Aided Design ofIntegrated Circuits and Systems, vol. 37, no. 12, pp. 3163–3176.

[10] Barman, J., & Kumar, V. (2018, May). Approximate Carry Look Ahead Adder (CLA) for Error Tolerant Applications. In 2018 2nd International Conference on Trends in Electronics and Informatics (ICOEI) (pp.730-734). IEEE.

[11] Tamil Chindhu, Shanmugasundaram, (2018), "Clcok Gating techniques: An Overview", proc. in IEEE conference on Emerging Devices and Smart Syatems.

[12] Khushbu Chandrakar, Dr. Suchismita Roy, (2017), "A SAT-based Methodology for Effective Clock gating for Power Minimization", accepted manuscript in JCSC.

[13] Preeti Sahu, Dr. Santosh Kumar Agrahari, (May, 2021), Low Power Design and Challenges in VLSI with IoT Systems, in International Conference on Advanced Computing and Communication Technology (ICACCT).

[14] Pritam Bhattacharjee, Alak Majumder, Tushar Dhabal Das, (2016), "A 90 nm Leakage Control Transistor Based Cloc Gating for Low Power Flip Flop Applications", in 59th International Midwest Symposium on Circuits and Systems (MWSCAS), 16-19 October 2016, Abu Dhabi, UAE, IEEE.

[15] R Keerthi Kiran, Dr. A B Kalpana, (2015), "Low Power 8, 16 & 32 bit ALU Design Using Clock Gating", in International Journal of Scientific & Engineering Research, Volume 6, Issue 8, ISSN 2229-5518.

[16] Kakarala Sandhya Rani, Krishna Prasad Satamraju, (2015), "A Novel Approach for Auto Clock Gating of Flip-flops", in IJSER, ISSN: 2347- 3878.

[17] Nandita Shriniwasan, Navamitha. S. Prakash, et al. (2015), "Power reduction by Clock Gating Technique", proc. in Science Direct, Smart Grid Technologies, Elsevier.

[18] Anand N, George Joseph, Suwin Sam, (2014), "Performance Analysis and Implementation of Clock gating techniques for Low Power Applications", proc. in IEEE conference on Science, Engineering and Management Research.

[19] Preeti Sahu, Dr. Santosh Kumar Agrahari, (December, 2020), Comparative Analysis of Different Clock Gating Techniques, IEEE, international conference ICRAIE.