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Three-phase H8 inverter with reduction common mode voltage and leakage current for TL-PV system

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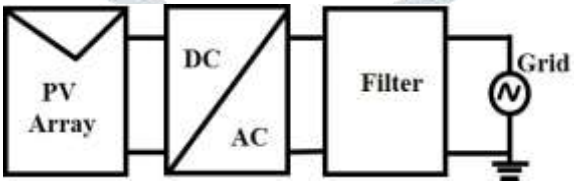
Abstract: Transformer-less inverter are commonly employed in grid-connected photovoltaic (PV) systems due to their small size, light weight, and low cost. In transformer-less PV inverters, on the other hand, common mode voltage reduction is one of the most critical challenges. Moreover, depending on the converter topology and modulation approach, numerous appealing single-phase transformer-less inverter topologies have been devised to eliminate the common mode voltage. Furthermore, the literature has paid little attention to three-phase topologies with low common mode voltage. To lower the common mode voltage, this paper offers a novel three phase eight switch inverter (H8) and related modulation approach. It's based on a three-phase (H6) inverter, although it works on a different concept. Performance experiments using MATLAB/Simulink are used to evaluate the efficacy of the proposed H8 design. Results show low variation in CMV and low THD in the output grid current, Low variation in CMV throughout the operation results in reduced leakage current.

Index Terms – ***Common mode current, common mode voltage, modulation index, transformer-less inverter, three phase inverter.***

I. INTRODUCTION

The inverter stage to using in this chapter for design the 3-Phase PV inverter reliability is affected by the size of dc-link capacitors. Because of its ease of design and implementation, the traditional 3-phase full-bridge inverter Fig.4. is often employed in PV applications. In grid-connected systems, transformer-less PV inverters are employed, as shown in Fig. 1(a).[1-3] The CMV challenges associated with the standard three-phase inverter are discussed in this section, as shown in Fig. 1. (b).



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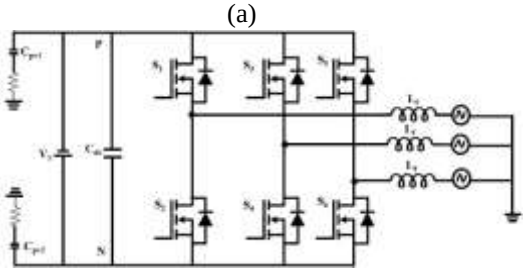

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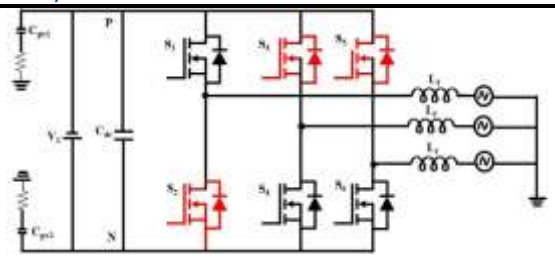

(c)

Fig.1.1: (a) Single phase grid linked system block diagram, (b) traditional three phase inverter (H6) design, (c) Mode of operation M4 (011)

To provide low leakage current output voltage in three-phase PV systems, modulation techniques and inverter design must be properly designed. With this configuration, the PV system works effectively [4-8]. Most galvanic isolation topologies, on the other hand, are generated by single-phase PV systems. Galvanic isolations are used to modulate three-phase systems. Thus, several three-phase TPV inverter topologies have been developed [9-11] as a result. The time-varying voltage magnitudes and growing leakage current limit the use of traditional modulation methods like SVPWM and DPWM. A Novel reduced common-mode voltage modulation (RCMV-PWM), such as AZPWM, NSPWM, and RSPWM, have been made in order to overcome CMV and CMC difficulties. A three-phase PV system's overall characteristics are ignored by RCMV-modulation techniques, which just reduce leakage currents [12-17].

In this research work, discusses modifications to the H8 design as well as a modulation strategy for reducing both common-mode voltage and leakage current throughout the grid cycle[3]. The design, operation, and overall performance of the inverter are all extensively examined. CMV, leakage current, and total harmonic distortion are measured using a 3-phase, six-switch TPV inverter (THD) [18-26]. Finally, the results of the simulation. The following structure, In a traditional three-phase system, the common mode voltage analysis is performed is discussed in section II, proposed topology and common mode evaluation is presented in section III, simulation results and conclusion are narrated in section IV and V.

II. THREE-PHASE PV SYSTEMS MODEL OF COMMON-MODE

The Resonant circuit between PV and grid is comparable to that of single-phase transformer-less inverter (TPV inverter). Leakage current and other variables like as parasitic capacitance (CPV) are provided (I_{leak}). Two of the five terminals are attached to input positive (P) and negative (N) terminals, while the other three are coupled to output filter terminals, as shown in Fig.2.1.

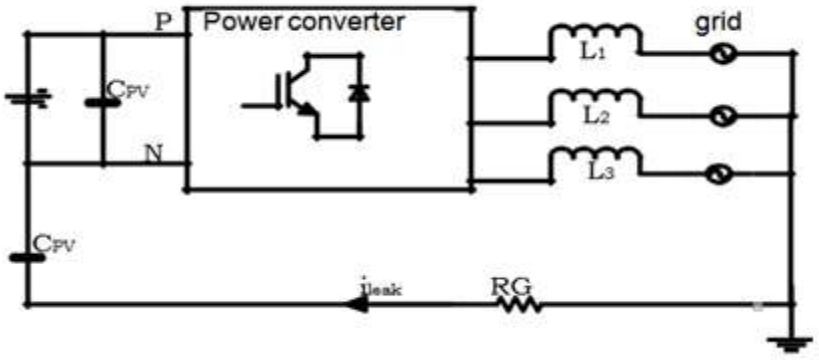

Fig. 2.1: Three-phase TPV inverter topology resonant circuit

The power converter block is shown as a voltage source in Fig.2.1, and this voltage source is then translated into smaller equivalent circuits (V_{AN}, V_{BN}, and V_{CN}). Power converter and resonant circuit variables influence leakage current. The common mode and differential mode voltages recorded across all phases are used to build the high-frequency model circuit for a 3-phase TPV inverter.

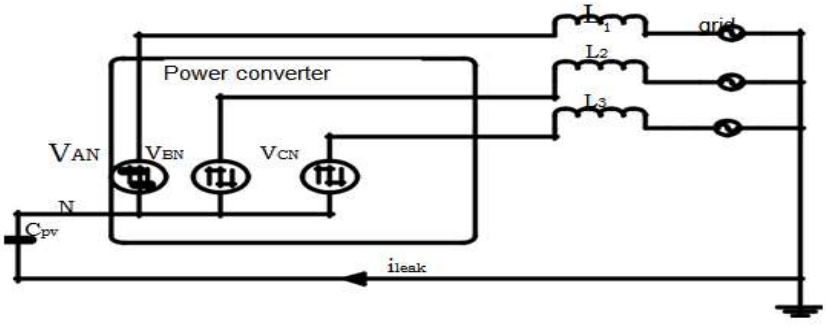

Fig.2.2: 3-Phase Simplified CM model circuit for TPV inverter.

The A and B are the focus of this investigation. Fig.2.2–2.3 show that the common-mode voltage is equal to the single-phase PV system when the filter inductors (L_1=L_2=L_3) are assumed to be identical (6).

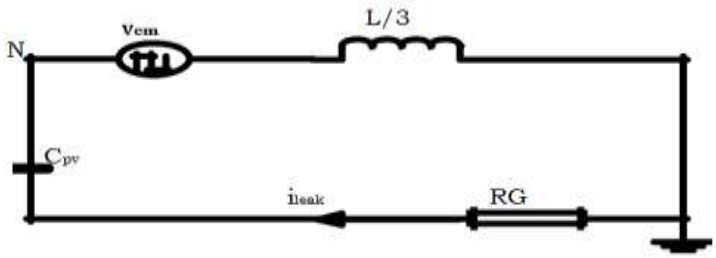

Fig.2.3: Model for three-phase TPV inverter topology with simplified CM model

Derivation principles for other phases, such as phase B, C and phase C, A may be used to the other stages. Model circuit for the three-phase TPV system shown at high frequency(Fig. 2.3). Using equation, which shows how 3-phase voltages are averaged to arrive at the CMV (1).

$$V_{CM}=\frac{V_{AN}+V_{BN}+V_{CN}}{3} \quad (1)$$

According to the preceding study, the creation of leakage current is strongly influenced by the CMV's reaction. It is thus critical to establish an appropriate inverter architecture and modulation method to eliminate leakage currents.

III. GALVANIC ISOLATION IN THE H8 MOSFET INVERTER DESIGN

It is possible for the PV arrays and the grid to lose current if the transformer is removed. To avoid this, make sure that all of the top switches are on or off at the same time. This is why a three-phase inverter (H6) requires additional switches and diodes to deliver galvanic isolation among the PV array and the utility grid. The H8 inverter circuit is shown in Fig.3.1.

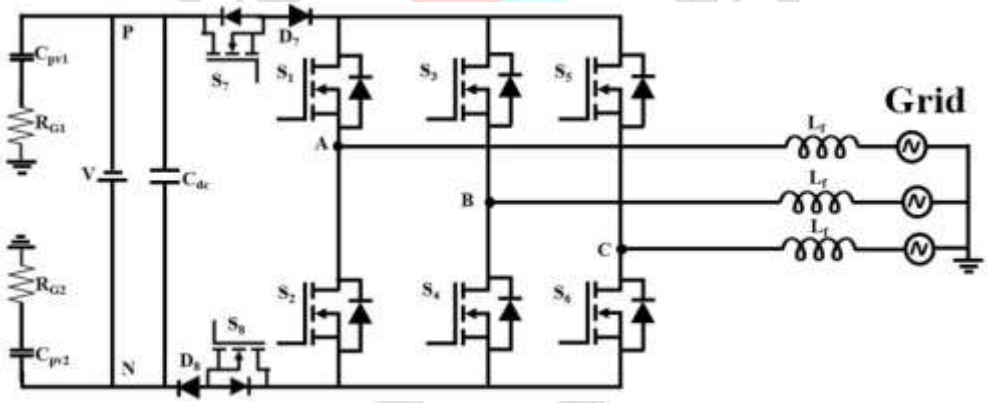

Fig.3.1: 3-phase (H8) inverter structure

In the current freewheeling paths between the dc source and the three-legs block, two more switches and two diodes (S7, S8) act as dc-bypass switches, and a capacitor divider on the dc side of the inverter allows for common-mode voltages up to 1/3 and 2/3 VDC for different operation modes.

IV. CMV MEASURE SCHEME OF MODULATION

The advantages and disadvantages of standard pulse-width modulation systems (SVPWM, DPWM), an improved conventional pulse-width modulation (ICPWM) A technique is suggested that reduces common-mode voltage and leakage current (Fig.4.1).

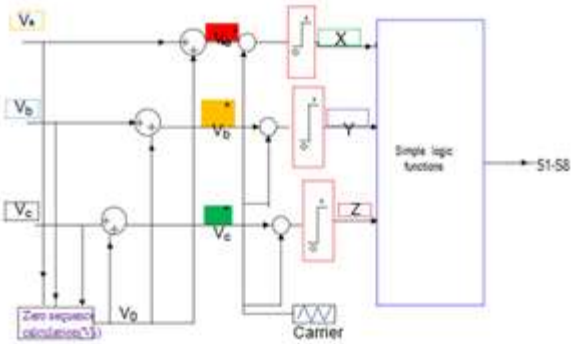

Fig.4.1: ICPWM scheme block diagram

Signals of sinusoidal amplitude are represented by voltages Va, Vb, and Vc. There's a zero sequence signal known as V_0, and m is the modulation index of that signal. For the maximum voltage, a sinusoidal signal (Va or Vb) is utilized as a reference (Vc). The modulating signals Va*, Vb*, and Vc* are then generated to injecting a zero voltage vector V_0. Once this is done, the logic signals are generated in a pattern of "X," "Y," and "Z" using just one carrier wave.

This may be achieved using a scalar method.

$V_a^* = V_a + V_0 = \text{msin}(wt) + V_0$

$V_b^* = V_b + V_0 = \text{msin}(wt - \frac{2}{3}\Pi)$ (2)

$V_c^* = V_c + V_0 = \text{msin}(wt + \frac{2}{3}\Pi)$ (3)

And V_0 is computed using the magnitude test.:

$V_0 = [sign(V_{max})](\frac{V_{dc}}{2}) - V_{max}$ (4)

The subsequent switching waveforms for S_1, S_3, S_5, S_7, and S_8 are constructed using simple logic operations, as shown in Fig.4.2.

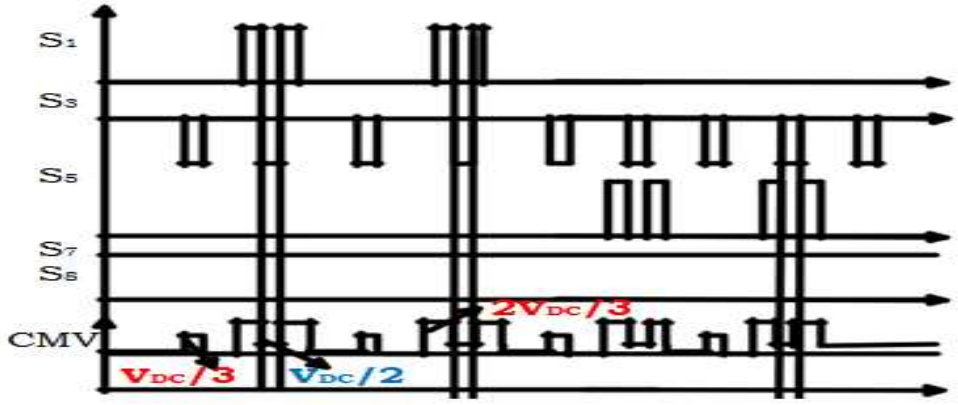

Fig. 4.2: H8 switching pattern and CMV.

In existing modulation systems, the suggested carrier-based modulation strategy is straightforward and easy to utilize in practice to obtain the appropriate output voltage waveform. As a result, the logic operations are listed below:

$S_1 = X + \bar{Y}\bar{Z} = 1$ $S_2 = \bar{X} + YZ = 0$

$S_3 = Y + \bar{X}\bar{Z} = 0$ $S_4 = \bar{Y} + XZ = 1$ (5)

$S_5 = Z + \bar{X}\bar{Y} = 0$ $S_6 = \bar{Z} + XY = 1$

$S_7 = S_8 = X.\bar{Y} + Y.\bar{X} + Z.\bar{Y} = 1$

By reducing the CMV from VDC/3 to 2VDC/3, the suggested ICPWM approach reduces the CMV by 1/3. Table 1: H8 inverter ICPWM modes.

Table.1:ICPWM operating modes

Mode	V_{AN}	V_{BN}	V_{CN}	Vcm
Mode-1(1001)	V_{DC}	0	0	$V_{DC}/3$
Mode-3(0101)	0	V_{DC}	0	$V_{DC}/3$
Mode-5(0011)	0	0	V_{DC}	$V_{DC}/3$
Mode-2(1101)	V_{DC}	V_{DC}	0	$2V_{DC}/3$
Mode-4(0111)	0	V_{DC}	V_{DC}	$2V_{DC}/3$
Mode-6(1011)	V_{DC}	0	V_{DC}	$2V_{DC}/3$
Mode-7(1110)	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$

The output switching functions S_1-S_8 may be calculated at (4.1) if the input logic signals XYZ=100, which is associated with mode1 (1001). As a result of this mode1, only the top switch of phase A as well as the lower switches S_4 and S_6, as well as the D_7 and S_8 and D_8 are turned on.

$S_1 = X+\bar{Y}\bar{Z} = 1$ $S_2 = \bar{X}+YZ = 0$

$S_3 = Y+\bar{X}\bar{Z} = 0$ $S_4 = \bar{Y}+XZ = 1$ (6)

$S_5 = Z+\bar{X}\bar{Y} = 0$ $S_6 = \bar{Z}+XY = 1$

$S_7 = S_8 = X.\bar{Y}+Y.\bar{X}+Z.\bar{Y} = 1$

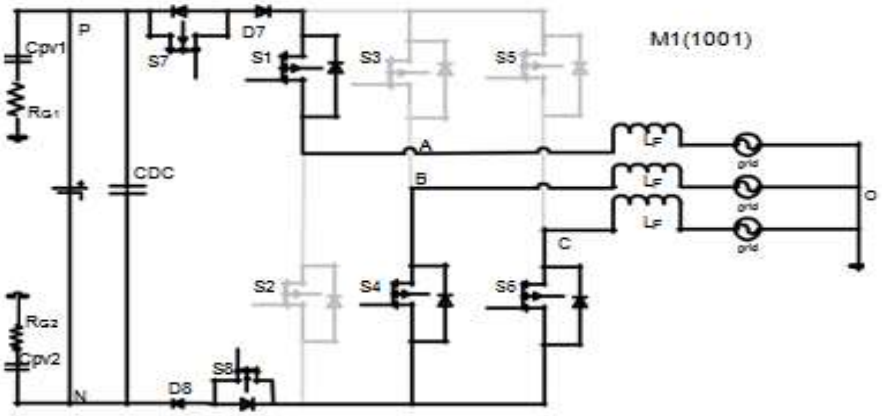

Fig. 4.3: Mode-1 H8 MOSFET inverter.

In this mode, $V_{AN}=V_{DC}$, $V_{BN}=V_{CN}=0$, hence CMV:

$$V_{CM}=\frac{V_{AN}+V_{BN}+V_{CN}}{3}=\frac{V_{DC}+0+0}{3}=\frac{V_{DC}}{3} \quad (7)$$

When XYZ=010, the output switching functions S_1-S_8 may be generated, as shown in Fig.4.9. (0101). Lower switches S_2, S_6, and S_7 are illuminated in Fig.4.9, while the upper switch S_3 is not. Fig.4.9

$S_1 = X+\bar{Y}\bar{Z} = 0$ $S_2 = \bar{X}+YZ = 1$

$S_3 = Y+\bar{X}\bar{Z} = 1$ $S_4 = \bar{Y}+XZ = 0$ (8)

$S_5 = Z+\bar{X}\bar{Y} = 0$ $S_6 = \bar{Z}+XY = 1$

$S_7 = S_8 = X.\bar{Y}+Y.\bar{X}+Z.\bar{Y} = 1$

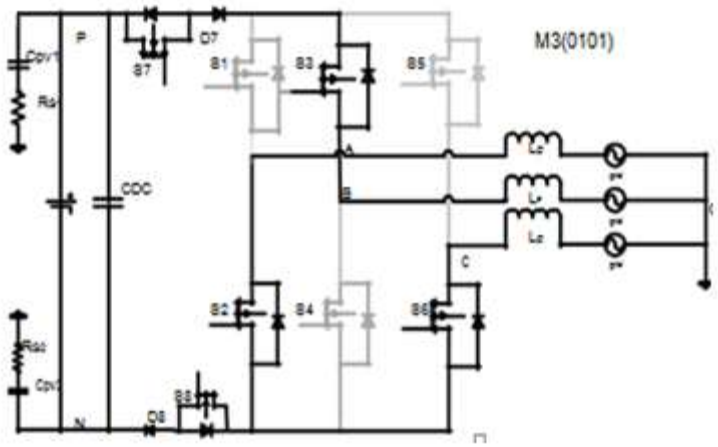

Fig. 4.4: Mode-3 H8 MOSFET inverter.

In this mode, $V_{AN}=V_{CN}=0$, $V_{BN}=V_{DC}$, therefore CMV:

$$V_{CM}=\frac{V_{AN}+V_{BN}+V_{CN}}{3}=\frac{0+V_{DC}+0}{3}=\frac{V_{DC}}{3} \quad (9)$$

If XYZ=001, then (12) gives the output switching functions S_1-S_8 for mode-5 (0011). The lower switches S_2, S_4 and S_8, D_8 and the upper switch S_5,S_7, $D_7$with phase C and the rest of the switches are turned off.

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$$S_1 = X+\bar{Y}\bar{Z} = 0 \qquad S_2 = \bar{X}+YZ = 1$$
$$S_3 = Y+\bar{X}\bar{Z} = 0 \qquad S_4 = \bar{Y}+XZ = 1 \quad (10)$$
$$S_5 = Z+\bar{X}\bar{Y} = 1 \qquad S_6 = \bar{Z}+XY = 0$$
$$S_7 = S_8 = X.\bar{Y}+Y.\bar{X}+Z.\bar{Y} = 1$$

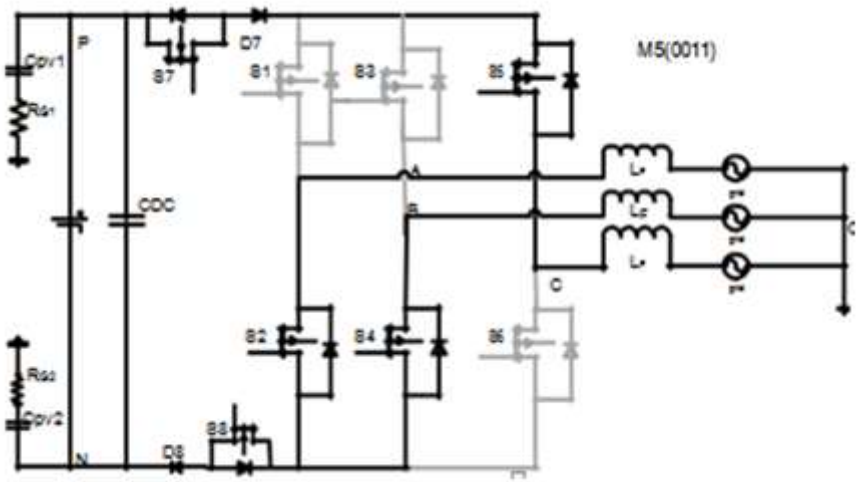

Fig. 4.5: Mode 5 H8 MOSFET inverter architecture

In this mode, VAN=VBN=0, VCN=VDC, therefore CMV:

$$V_{CM}=\frac{V_{AN}+V_{BN}+V_{CN}}{3}=\frac{0+0+V_{DC}}{3}=\frac{V_{DC}}{3} \quad (11)$$

If XYZ=110, then (14) gives the output switching functions S_1-S_8 for mode-2 (1101). As illustrated in Fig.4.11, The lower switches S1, S3, and S7 are all turned on, while the top switch S6 with phase C is turned on and the rest of the switches are turned off.

$$S_1 = X+\bar{Y}\bar{Z} = 1 \qquad S_2 = \bar{X}+YZ = 0$$
$$S_3 = Y+\bar{X}\bar{Z} = 1 \qquad S_4 = \bar{Y}+XZ = 0 \quad (12)$$
$$S_5 = Z+\bar{X}\bar{Y} = 0 \qquad S_6 = \bar{Z}+XY = 1$$
$$S_7 = S_8 = X.\bar{Y}+Y.\bar{X}+Z.\bar{Y} = 1$$

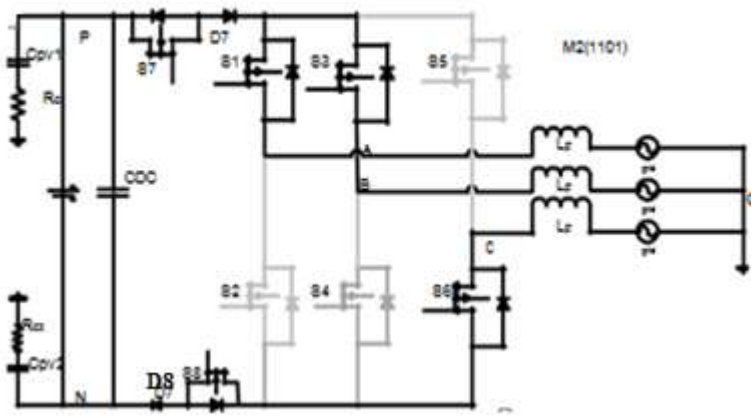

Fig. 4.6 : Mode 2 H8 MOSFET inverter architecture.

Because the output voltages are VAN=VBN=VDC and VCN=0, CMV is calculated as follows:

$$V_{CM}=\frac{V_{AN}+V_{BN}+V_{CN}}{3}=\frac{V_{DC}+V_{DC}+0}{3}=\frac{2V_{DC}}{3} \quad (13)$$

If XYZ=011, then (16) gives the output switching functions S_1-S_8 for mode4 (0111). As illustrated in Fig.5.2, up on the switches S_3, S_5 and S_7 are ON, while the down on the switch S_2 is ON and the rest of the switches are turned off.

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$$S_1 = X+\bar{Y}\bar{Z} = 0 \qquad S_2 = \bar{X}+YZ = 1$$

$$S_3 = Y+\bar{X}\bar{Z} = 1 \qquad S_4 = \bar{Y}+XZ = 0 \quad (14)$$

$$S_5 = Z+\bar{X}\bar{Y} = 1 \qquad S_6 = \bar{Z}+XY = 0$$

$$S_7 = S_8 = X.\bar{Y}+Y.\bar{X}+Z.\bar{Y} = 1$$

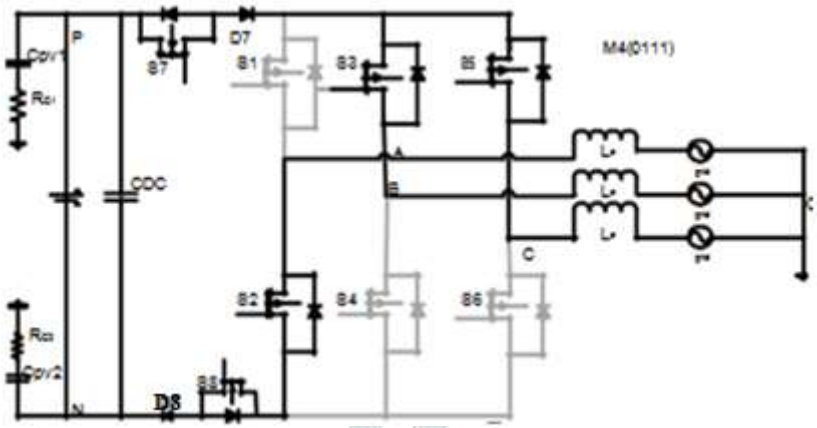


Fig. 4.7: Mode-4 H8 MOSFET inverter architecture.

The voltages at output side are V_{AN}=0, V_{BN}=V_{CN}=V_{DC}, hence CMV is obtained as follows:

$$V_{CM}=\frac{V_{AN}+V_{BN}+V_{CN}}{3}=\frac{0+V_{DC}+V_{DC}}{3}=\frac{2V_{DC}}{3} \quad (15)$$

If XYZ=101, then (18) gives the output switching functions S_1-S_8 for mode-6 (1011). As illustrated in Fig.5.3, upon the switches S_1, S_5 and S_7 are ON, while the down switch S_4 is ON and the rest of the switches are turned off.

.In this mode, V_{AN}=V_{CN}=V_{DC}, V_{BN}=0, therefore CMV :

$$V_{CM}=\frac{V_{AN}+V_{BN}+V_{CN}}{3}=\frac{0+V_{DC}+V_{DC}}{3}=\frac{2V_{DC}}{3} \quad (16)$$

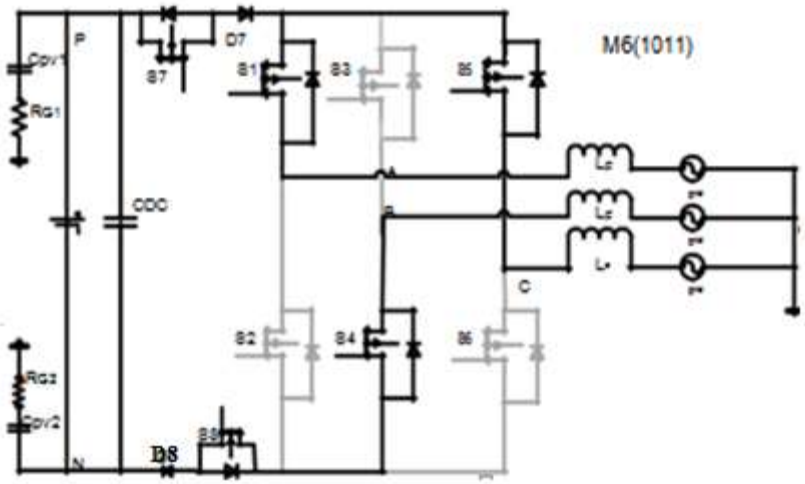


Fig. 4.8: Mode-6 H8 MOSFET inverter architecture.

When the input logic signals XYZ=111, the output switching functions S_1-S_8 are connected with mode-7. For example, in Figure.5.4 the upper and lower switches are on while the decoupling switches are off.

$$S_1 = X+\bar{Y}\bar{Z} = 1 \qquad S_2 = \bar{X}+YZ = 1$$
$$S_3 = Y+\bar{X}\bar{Z} = 1 \qquad S_4 = \bar{Y}+XZ = 1 \qquad (17)$$
$$S_5 = Z+\bar{X}\bar{Y} = 1 \qquad S_6 = \bar{Z}+XY = 1$$
$$S_7 = S_8 = X.\bar{Y}+Y.\bar{X}+Z.\bar{Y} = 0$$

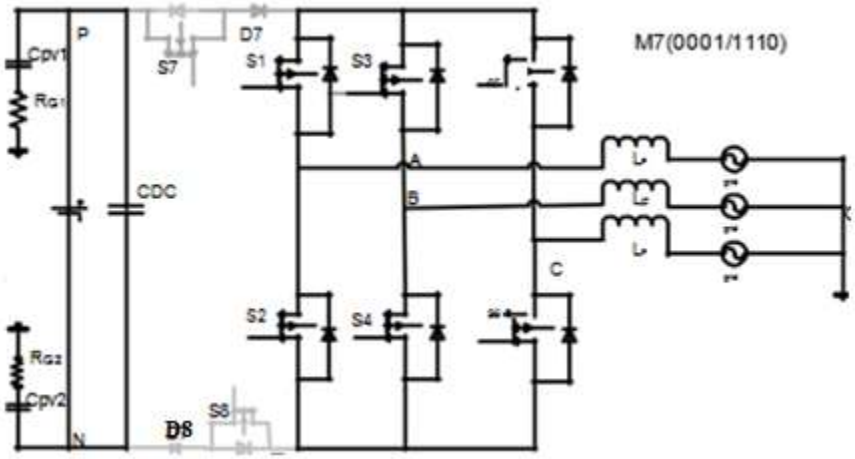


Fig. 4.9 : Mode-7 H8 MOSFET inverter architecture.

The voltages at output sides are $V_{AN}=V_{BN}=V_{CN}=V_{DC}/2$, therefore CMV :

$$V_{CM}=\frac{V_{AN}+V_{BN}+V_{CN}}{3} = \frac{\frac{V_{DC}}{2}+\frac{V_{DC}}{2}+\frac{V_{DC}}{2}}{3} = \frac{V_{DC}}{2} \qquad (18)$$

Since the dc-decoupling branch reduces the common-mode voltage by $V_{DC}/3$, the former six modes of operation are identical to the standard H6 arrangement. As a result, CMV is minimized with lower leakage current. For example, the ICPWM scheme reduces CMV and CMC while keeping the distinctive properties of traditional modulation schemes.

V. MATLAB SIMULATION RESULTS

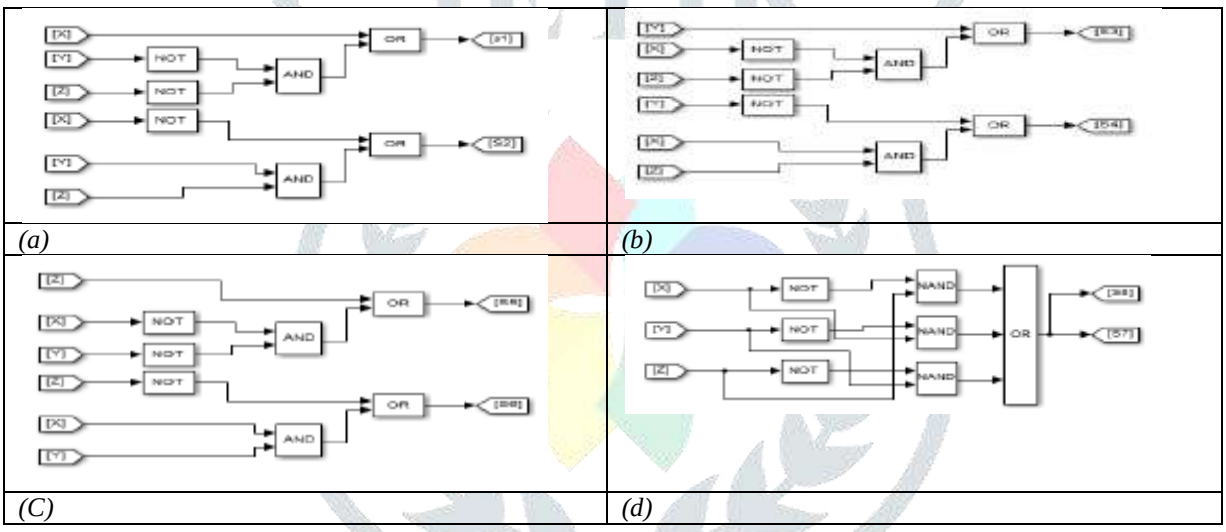
Comparing the H8 MOSFET inverter to the H6 inverter to verify in MATLAB/Simulink software tool, is an interesting exercise. All simulation parameters are shown in Table.2. This parameter for both SVPWM and ICPWM are modulated at the range of frequency 10 kHz, while the proposed DPWM technique is modulated at an even higher frequency of 15 kHz.

Table. 2: Selected parameters for simulation

Parameters	Values
Input voltage(Vin)	$300V_{DC}$
DC-link capacitors,C_{DC1},C_{DC2}	2μF
Inductors (L_f)	5mH
Capacitor (C_F)	1μF
Modulation-Index(M_a)	0.8
Resistance (R_L)	10Ω
Capacitors (C_{PV1}, C_{PV2})	220nF
Ground Resistors,(R_G)	11Ω

With full-bridge capacity, an inverter pulse generator system. For the H8 inverter, toggles between the dc-link and full-bridge inverters.

Logic functions of the Proposed H8 Inverter



(a) *(b)*

(C) *(d)*

Fig.5.1. The switching functions in terms of logic gates are shown (S1-S8)

5.1. Output Performance

The output waveforms of the stated topologies for common Common modulation schemes (CMS) like SVPWM and DPWM are shown in Figures 5.2 and 5.4. SVPWM and DPWM provide unipolar three-level output voltage and sinusoidal output current with significant current ripples.

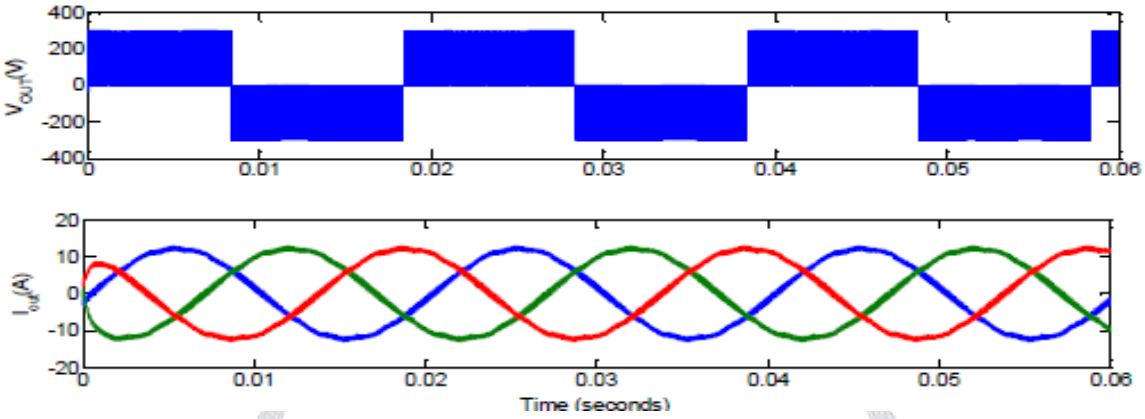


Fig. 5.2: SVPWM H6 TPV inverter output voltage and current

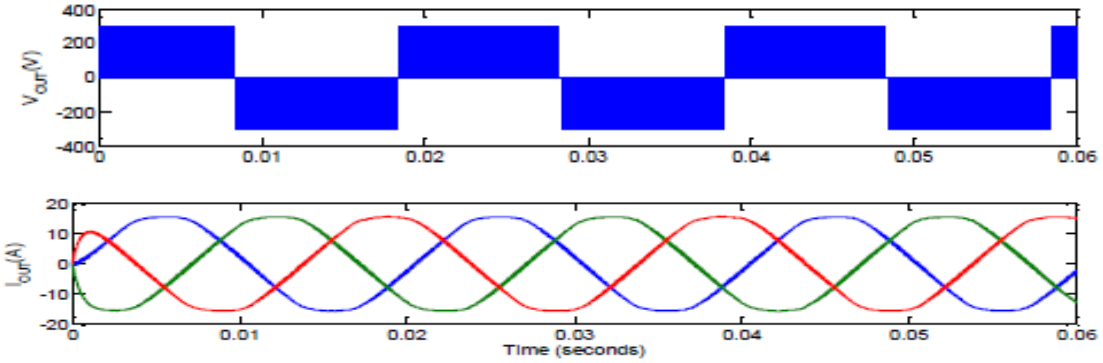


Fig. 5.3: DPWM H6 TPV inverter output voltage and current

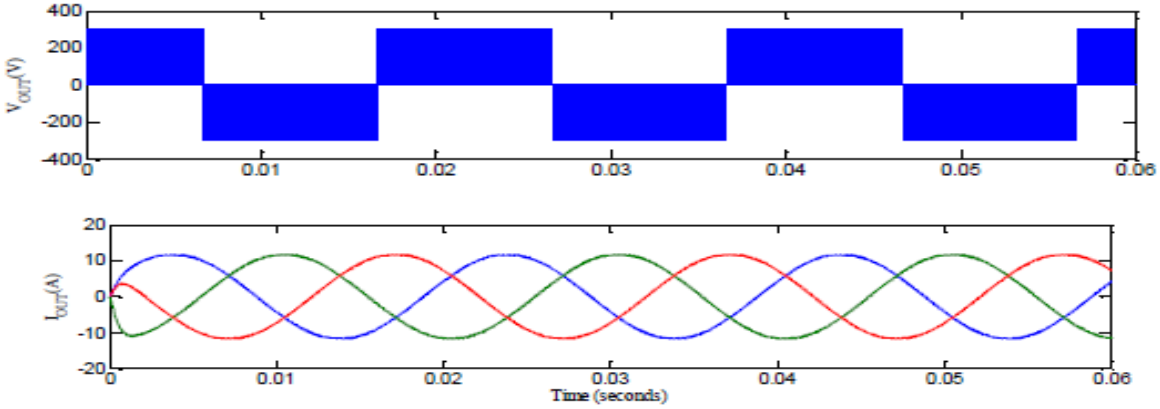


Fig. 5.4: H8 TPV ICPWM inverter voltage and current.

To the reduced leakage current, the proposed H8 topology with ICPWM scheme results in unipolar three-level output voltage and sinusoidal load current Fig.5.3. The output voltage fluctuates from 0 to +VDC or 0 to -VDC during the course of a grid cycle. ICPWM preserves the distinguishing characteristics of classic modulation schemes, such as the usage of zero states. Unipolar modulation minimizes losses and current ripples compared to bipolar PWM. Therefore, a smaller filter is needed, resulting in cheaper costs and smaller dimensions.

5.2. Common-mode

Fig.5.5-5.7. illustrates the common-mode characteristics of a three-phase H6 TPV inverter using typical modulation techniques. Using zero vector states in every PWM cycle results in poor CMV characteristics for SVPWM and DPWM. Fig.5.4 and 5.6 shows that bigger common-mode currents are generated. These waves are bigger than those of other popular topologies, and this is Fig.5.5-5.7.

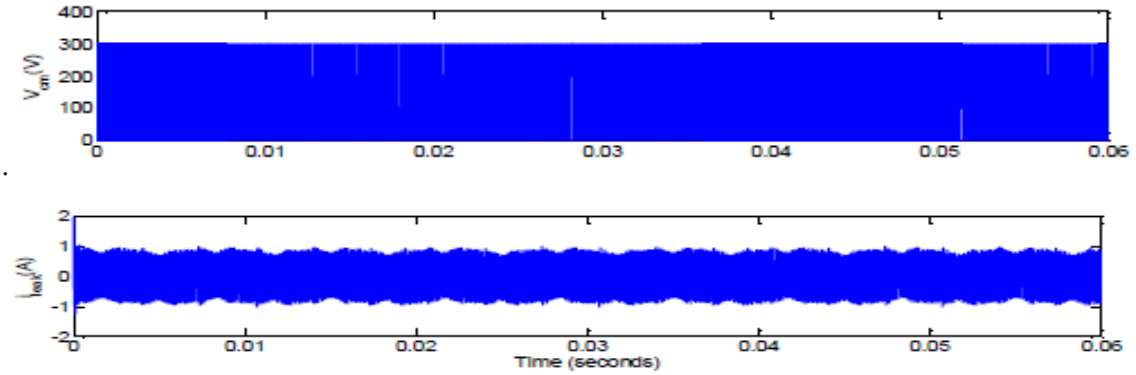


Fig. 5.5: voltage and current draw of SVPWM H6 TPV inverter

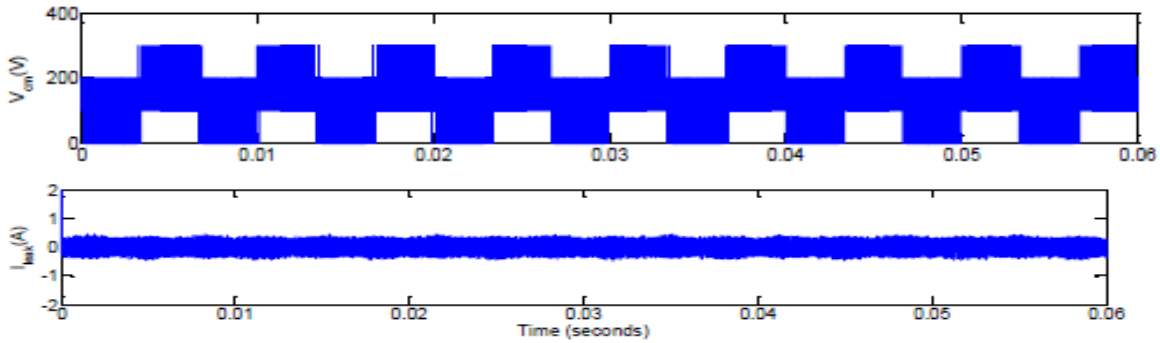


Fig. 5.6: Voltage and leakage current CM-DPWM H6 TPV inverter.

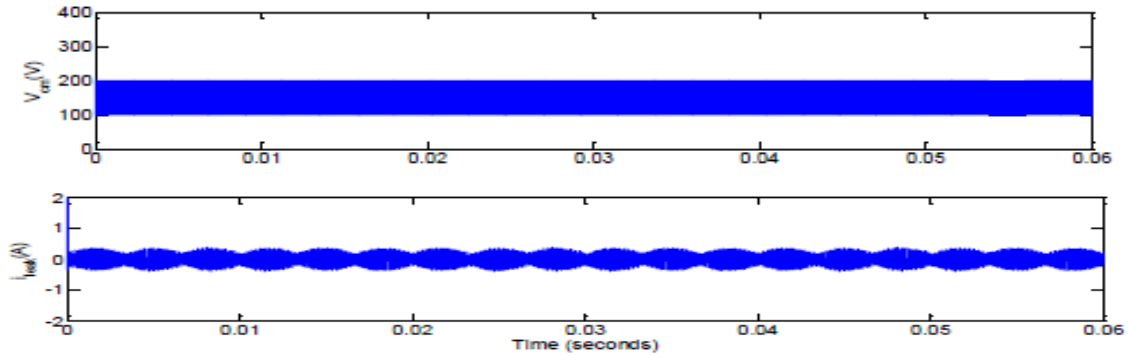


Fig. 5.7.: Voltage and leakage current CM-ICPWM H8 TPV inverter.

Because dc-decoupling switches (at mode-7 or state-7) are configured to create unipolar output voltage with lower leakage current during freewheeling time, the CMV is reduced by 1/3. This relies on the mode of operation of dc-decoupling switches S_7 or S_8. Depending on S_7 or S_8, the CMV varies from $V_{DC}/3$-$2V_{DC}/3$ to $V_{DC}/3$-$V_{DC}/2$.

The suggested H8 TPV inverter design offers galvanic separation during freewheeling. CMV and leakage current are both reduced in the H8 TPV inverter design with ICPWM modulation, as shown in Fig.5.5-5.7. SVPWM, DPWM, and ICPWM CMV waveforms for a H6 TPV inverter are shown in Fig.5.8–5.10. SVPWM and DPWM in the typical H6 architecture with SVPWM and DPWM have poor common-mode behavior, ranging from 0-$3V_{DC}$/3-V_{DC} to 0-$3V_{DC}$/3-V_{DC}. With DPWM the CMV drops to 0-V_{DC}, but it remains time variable (see Fig.5.4).

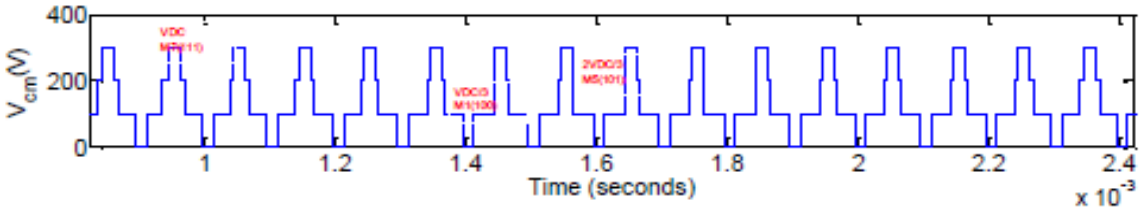


Fig. 5.8: Microscopic SVPWM H6 common-mode voltage waveform

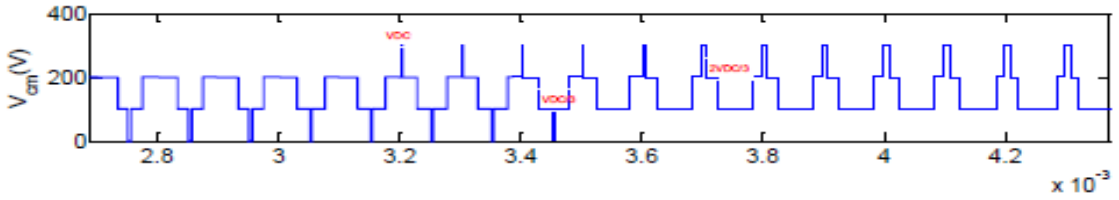


Fig. 5.9 : DPWM common-mode voltage waveform of H6 topology

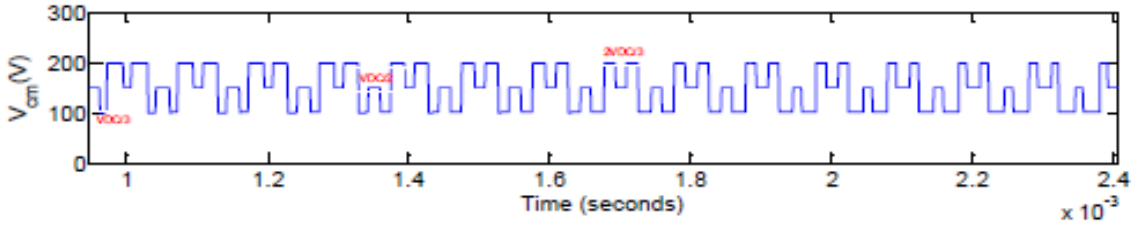


Fig. 5.10: Microscopic H8 topology common mode voltage waveform using ICPWM.

Fig.5.8 shows that the common-mode voltage ranges from V_{DC}/3 to V_{DC}/2-2V_{DC}/3. To cut leakage current to a quarter of the input DC-link voltage, the proposed ICPWM modulation scheme's CMV ranges from V_{DC}/3-V_{DC}/2-2V_{DC}/3 compared to the conventional modulation methods. Galvanic isolation switches in the freewheeling path are to blame for this. Minimal switching losses and three-level output voltage are coupled with ICPWM in the proposed H8 design (reduced CMV, CMC and low THD).Verifyingby MATLAB/Simulink FFT analysis, Figures 5.5 to 5.7 show the total harmonic distortion (THD) of the aforementioned topologies in relation to output current. A THD of 4.07 percent and a THD of 2.79 percent, respectively, is measured for output load current ripples using the H6 topology with SVPWM and DPWM.

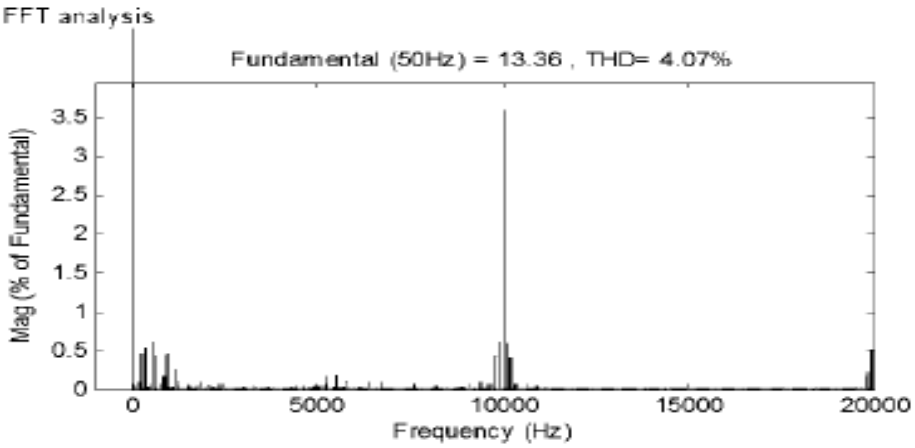


Fig. 5.11: Output current THD of the H6 TPV inverter

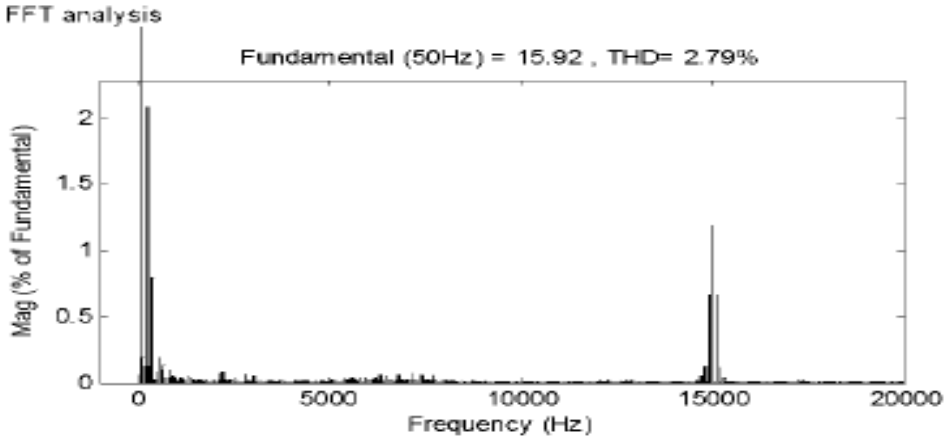


Fig. 5.12: Output current THD of the H6 TPV inverter

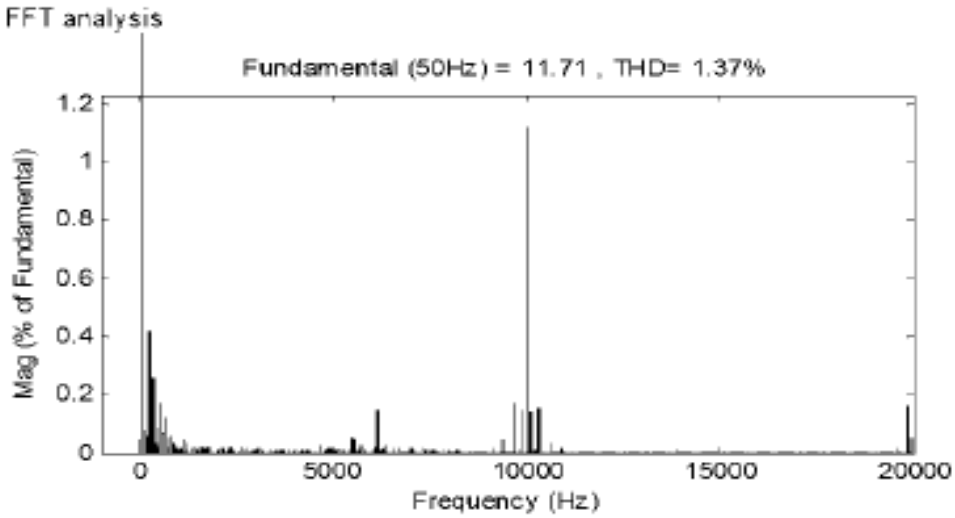


Fig. 5.13: THD of the output current of the H8 TPV inverter.

Increased leakage current and a deficient CM are to blame for this. Low THD current ripples of 1.37 percent are achieved by the proposed H8 inverter topology, which is less than the H6 design. H6 and H8 TPV inverters with modulation schemes are summarized in Table.3. ICPWM modulation has the best overall performance for unipolar line-line output voltage, the lowest switching losses for standard modulation schemes (SVPWM and DPWM), and the lowest RCMV, CMC, and THD for standard modulation schemes (RCPWM) for RCMV-modulation.

Table.3: Multiple topologies are examined in depth.

Parameter	H6 Inverter		H8 inverter
	SVPWM	DPWM	ICPWM
V_{LL}-pattern	Unipolar	Unipolar	Unipolar
Switching- frequency(kHz)	10	15	10
CMV(V)	0-VDC	0-VDC	1/3VDC- 2/3VDC
Leakage-current(A)	0.91A	0.73A	0.20A
THD %	4.07	2.79	1.37

VI. CONCLUSION

This paper begins with confirming the three-phase full-bridge inverter and then deriving the three-phase PV system's CM mode model circuit step by step to comprehend the TPV inverter's generalized principles. A H6 inverter is utilized in most PV systems; however its capacity to manage common-mode voltage and leakage current is unknown. When using a TPV inverter, it is critical to ensure that the output voltage is not leaking. Based on the advantages and disadvantages of the H6 TPV inverter, a "H8 inverter" with galvanic isolation and MOSFETs as primary power devices is proposed. A unique carrier modulation method is explained and demonstrated in this paper. In terms of CMV, leakage current and harmonic distortion, the suggested ICPWM modulation approach for the H8 inverter is examined and confirmed. As a consequence, the H8 TPV inverter design with ICPWM scheme reduces CMV and leakage current while maintaining PV system performance. It provides unipolar output voltage, decreased switching losses, and lower CMV, CMC, and THD for typical modulation systems. This would be extremely beneficial to a three-phase PV system.

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