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Design and Analysis of 5-Level Cascaded H-Bridge Multilevel Inverter with Photovoltaic System

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Abstract : A multilevel inverter is a power electronic device that is capable of providing desired alternating voltage level at the output using multiple lower-level DC voltages as an input. Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage applications. Multilevel inverters nowadays are used for medium voltage and high power applications. This paper presents a design and analysis of 5-level cascaded H-bridge multilevel inverter with photovoltaic system. The modular cascaded multilevel topology helps to improve the efficiency and flexibility of PV systems. To realize better utilization of PV modules and maximize the solar energy extraction, a distributed maximum power point tracking control scheme is applied to both single- and three-phase multilevel inverters, which allows independent control of each DC-link voltage. The simulation is performed using MATLAB-SIMULINK software.

IndexTerms **- 5-Level, Cascaded H-Bridge, Multilevel, Inverters, Three-Phase, Grid-Connected.**

I. INTRODUCTION

A multi-level converter (MLC) is a method of generating high-voltage wave-forms from lower-voltage components. A power inverter, or inverter, is a power electronic device or circuitry that changes direct current (DC) to alternating current (AC). The input voltage, output voltage and frequency, and overall power handling depend on the design of the specific device or circuitry. The inverter does not produce any power; the power is provided by the DC source. A power inverter can be entirely electronic or may be a combination of mechanical effects (such as a rotary apparatus) and electronic circuitry. Static inverters do not use moving parts in the conversion process. Power inverters are primarily used in electrical power applications where high currents and voltages are present; circuits that perform the same function for electronic signals, which usually have very low currents and voltages, are called oscillators.

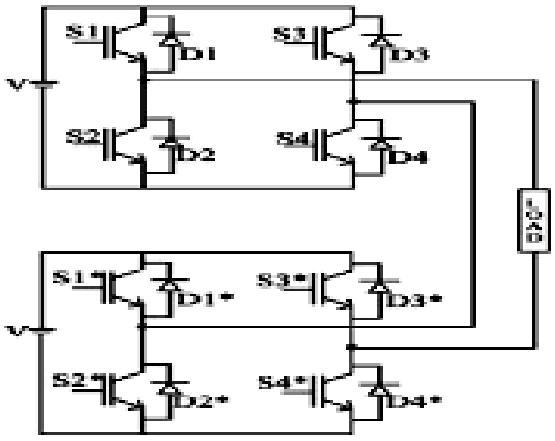

Figure 1: Basic diagram of five level cascaded inverter

The cascaded multilevel inverter made of a series of H bridge (single-phase full-bridge) inverter units. Every full-bridge can produce three different voltage outputs like -*V*dc, 0, and +*V*dc. Though, five multilevel inverters can produce staircase waveform as shown in Figure 1. The numeral of output phase voltage levels in a cascaded multilevel inverter equation is 2*S* + 1, here *S* is the number of DC sources. Every H-bridge module generates a quasi-square waveform by phase-shifting the switching timings of its positive and negative phase legs.

Cascaded H-Bridges is the basic structures for multilevel inverters: In Cascaded H-Bridges each DC power source is connected to an H-bridge inverter. Basically the single inverter has four switches. By using switching combinations, the single inverter can create three different AC voltage outputs.

II. BACKGROUND

S. Dhara et al.,[1] presents a novel 1-φ, 5-level inverter is proposed, which employs a HB structure to eliminate voltage oscillations from v_{CPV} without compromising with the dc-bus utilization or symmetric operation. This is achieved by integrating a switched capacitor network with the HB structure. All the necessary analysis and design procedures are included to support the various claims. The claims are further validated using MATLAB simulations and experiments on a laboratory prototype..

M. Ali et al.,[2]. A large dataset is prepared for two-angle and four-angle operation of MPUC-5 under various dc-link voltages and constraints with which an ANN-based controller is trained. A neural network with a hidden layer is trained with the backpropagation technique; and once a correlation is developed, the network can be operated for a wide range of operating conditions. The robustness of the controller is verified through simulation in MATLAB/Simulink environment and validated by experimental emulation in an hardware in loop environment.

B. P. Reddy et al.,[3] The proposed MLI is efficient to operate the PPMIM drive in both normal as well as fault conditions with rated power/torque. The proposed MLI-fed PPMIM drive performance with open circuit/short circuit of switch and source fault conditions are analyzed. The proposed MLI scheme is validated with the Ansys Maxwell finite element method (FEM) as well as laboratory testbed on a 5-hp 9-phase PPMIM drive under normal as well as open circuit switch/source fault conditions.

K. Wang et al.,[4] A zero-sequence voltage injection-based NP voltage balancing method is proposed. For a high modulation index range more than 0.5, a decoupled voltage-balancing method based on COPWM is used. By combining the two modulations and voltage-balancing methods, the NP voltages can be balanced under the full modulation index range with reduced switching losses. Simulation and experimental results are presented to confirm the validity of this method.

B. Prathap Reddy et al.,[5] The proposed MLI scheme is realized with three five-leg inverter modules. Each five-leg inverter module will generate three-level voltage across the phase, thereby resultant voltage seen by each phase winding is five-level voltage in 3PH-12PO mode. This multilevel voltage will improve the torque ripple profile of the motor drive. In addition, the proposed MLI scheme along with phase grouping will enrich the linear modulation range of the pole-phase-modulated induction motor (PPMIM) drive in nine-phase four-pole (9PH-4PO) mode.

M. T. Fard et al.,[6] a hybrid Si/SiC 5L-ANPC inverter is developed with a synchronous optimal pulse(SOP) width modulation strategy for controlling the switches in cell 2 and finite-control-set model predictive controller(FCS-MPC) for those in cell 3 of the inverter. Consequently, in the proposed topology, the SiC devices are merely used for the high-frequency switches in cell 3 and the rest of the low-frequency switches are configured with Si IGBTs. This Si/SiC hybrid ANPC inverter concurrently provides high efficiency and low implementation cost at high-speed operation mode. Simulation and experimental results are provided to verify the effectiveness of the proposed hybrid inverter.

P. Kant et al.,[7] A new approach to improve the power quality of medium voltage induction motor drive (MVIMD) at both utility and drive end is presented. Here, 3-multi-winding transformers (MWT) (T_1, T_2, T_3) are utilized and each MWT converts 3-phase input AC-supply into two isolated 5-phase AC-supplies with unique (18°) phase-shift among them. Moreover, due to unique (±6° and 0°) angle in the primary sides of these MWTs, the line current drawn from the grid has 60-pulses.

M. B. Satti et al.,[8] presents the use of less number of semiconductor switches while keeping a similar number of yield voltage levels made the proposed GCPS effective, less expensive, and less complex in structure. In addition, its voltage and current THD are practically identical with the frameworks existing in the writing.

Y. P. Siwakoti et al.,[9] presents an analysis and design of a new boost type six-switch five-level (5L) active neutral point clamped (ANPC) inverter based on switched/flying capacitor technique with self-voltage balancing. Compared to major conventional 5L inverter topologies, such as neutral point clamped, flying capacitor, cascaded H-bridge, and ANPC topologies, the new topology reduces the dc-link voltage requirement by 50%.

Z. Wang et al.,[10] presents a comprehensive design and validation of a compact all-silicon carbide (SiC) 250-kW T-type traction inverter with a power density of 25 kW/l and 98.5% peak efficiency. All the operation modes and switching transitions in a T-type phase leg are analyzed to model the semiconductor power losses over a fundamental cycle. Special attention has been paid to investigate the behavior and losses due to the reverse conduction of the SiC MOSFETs.

T. T. Davis et al.,[11] a neutral point (NP) voltage balancing scheme suitable for three phase 5-level active NP clamped and T-type NP clamped (TNPC) inverters is discussed. Carrier-based pulsewidth modulation is used for the balancing of dc-link capacitors and floating capacitors (FC) in the inverter. The FC voltages are regulated with the help of redundant switching states of pole voltage levels and the dc-link capacitor voltages are controlled using zero-sequence voltage injection.

L. Zhang et al.,[12] The common-ground-type topology can eliminate common mode (CM) leakage current by connecting the negative terminal of the photovoltaic(PV) directly to the neutral point of the grid, which bypasses the PV array's stray capacitance. The dual-buck-based topology guarantees increased robustness since the dc-link cannot be short-circuited by a shoot-through event.

III. PROPOSED MODEL

In proposed three phase, six switch, full-bridge inverter is used to reduce the harmonic level. The SVM technique based PWM very help full to making the switching pulse with better perform output. In this paper, constant switching frequency and variable switching frequency based on carrier pulse width modulation methods are presented and compared. A new modulation method called trapezoidal triangular multi carrier (TTMC) SPWM is implemented and compared with other methods. This new modulation method gives advantages in multilevel inverter to minimize the percentage of total harmonic distortion (THD) and to increase the output voltage.

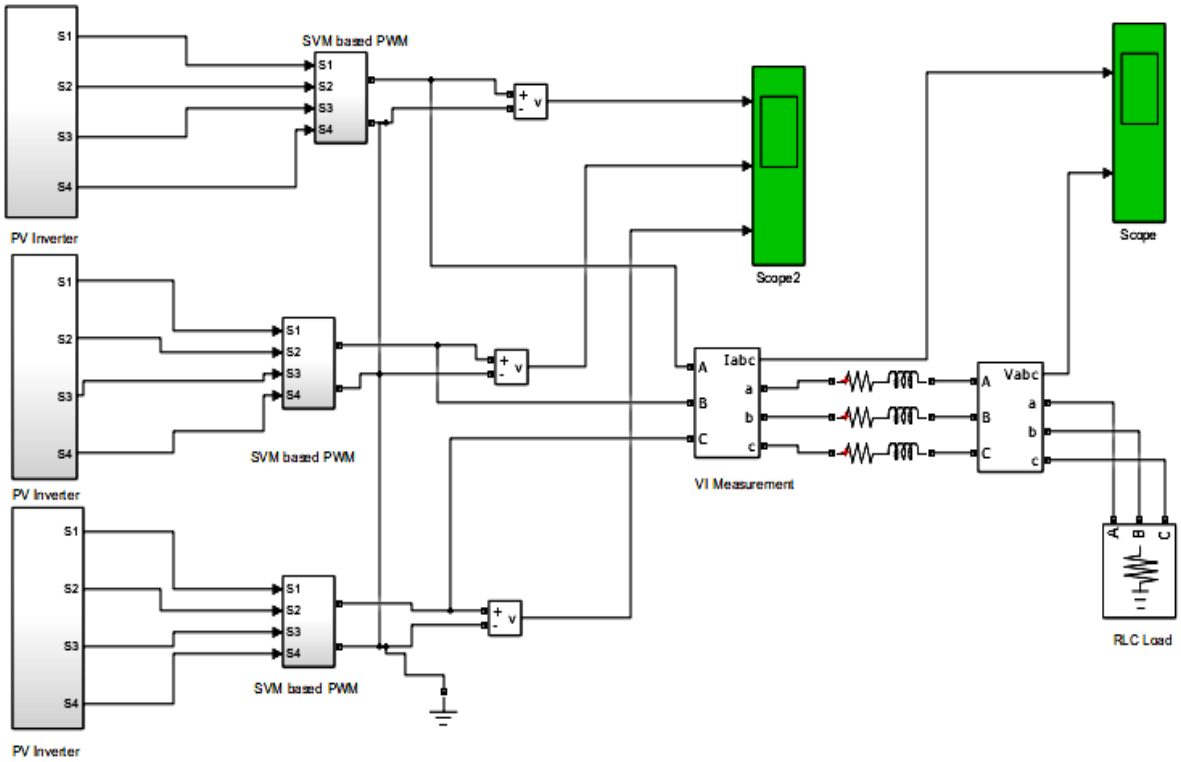

Figure 2: Proposed model

Figure 2 is showing proposed cascaded H-Bridge multilevel PV inverter. This model consist various sub models which is described in details.

Sub-Modules

- PV Cell
- Inverter
- SVM based PWM (SPWM)
- Analysis

IV. SIMULATION RESULTS

The implementation of the proposed model is done over MATLAB 9.4.0.813654 (R2018a). The various electrical toolbox and blocks helps us to use the functions available in MATLAB Library for various design strategy.

Case –I

The waveform simulated value is assigned for sine wave and S1, S2, S3 and S4 carrier wave. The phase angle in rad is 0.

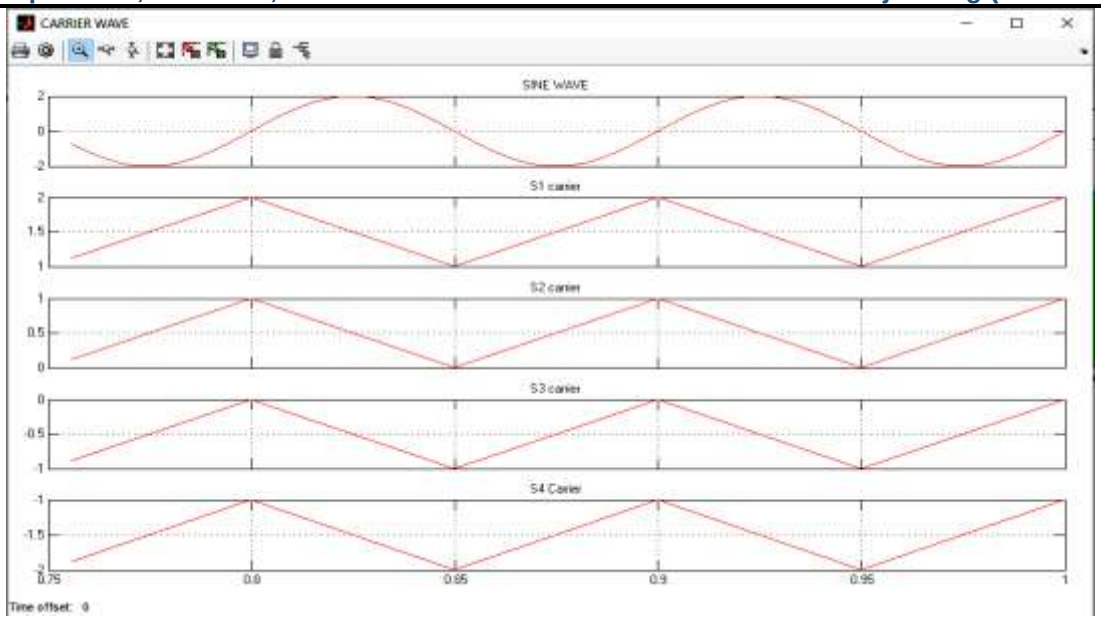

Figure 3: Sine wave and Carrier wave

Figure 3 is showing the sine wave and all carrier wave. A theoretical sine wave is an "pure" wave in that it has no harmonics and involves zero bandwidth in the recurrence space. X hub is showing the time scale and Y pivot is showing the adequacy of wave. A switching succession framed by a few switching conditions of the converter is performed and the normal estimation of the yield voltage must correspond with the ideal reference.

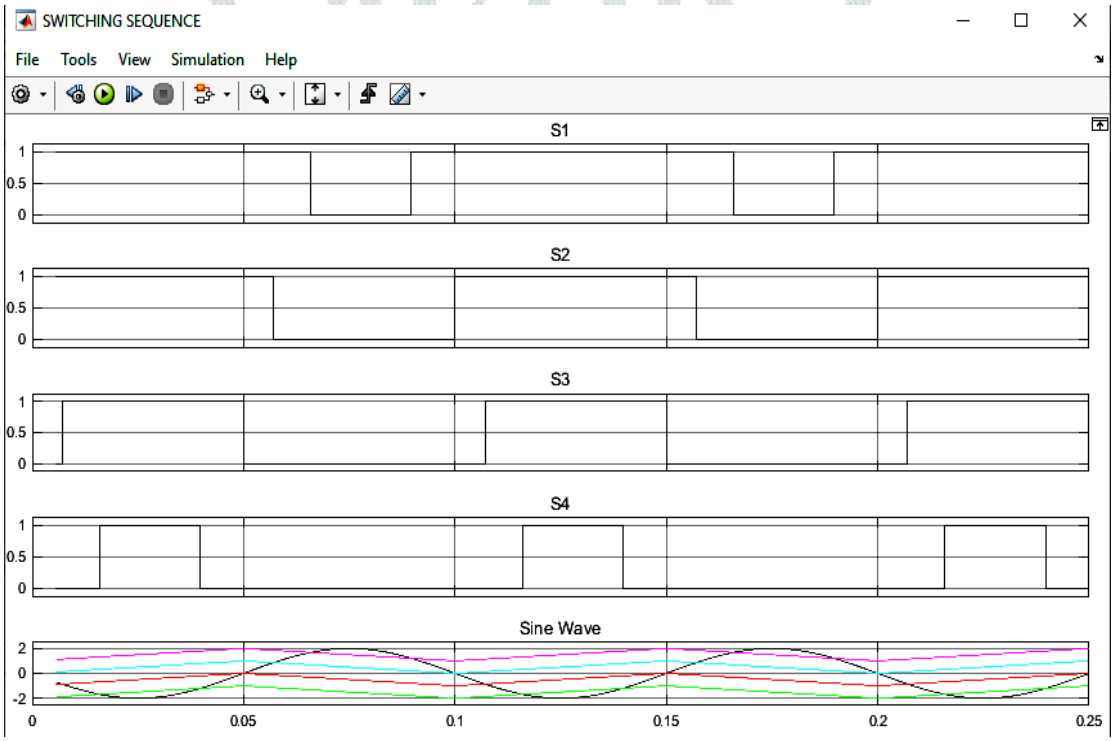

Figure 4: Switching Sequence

A switching grouping shaped by a few switching conditions of the converter is performed and the normal estimation of the yield voltage must concur with the ideal reference.

Case –II

The waveform simulated value is assigned for sine wave and S1, S2, S3 and S4 carrier wave. The phase angle in rad is 2*pi/3 or 120’ phase shift.

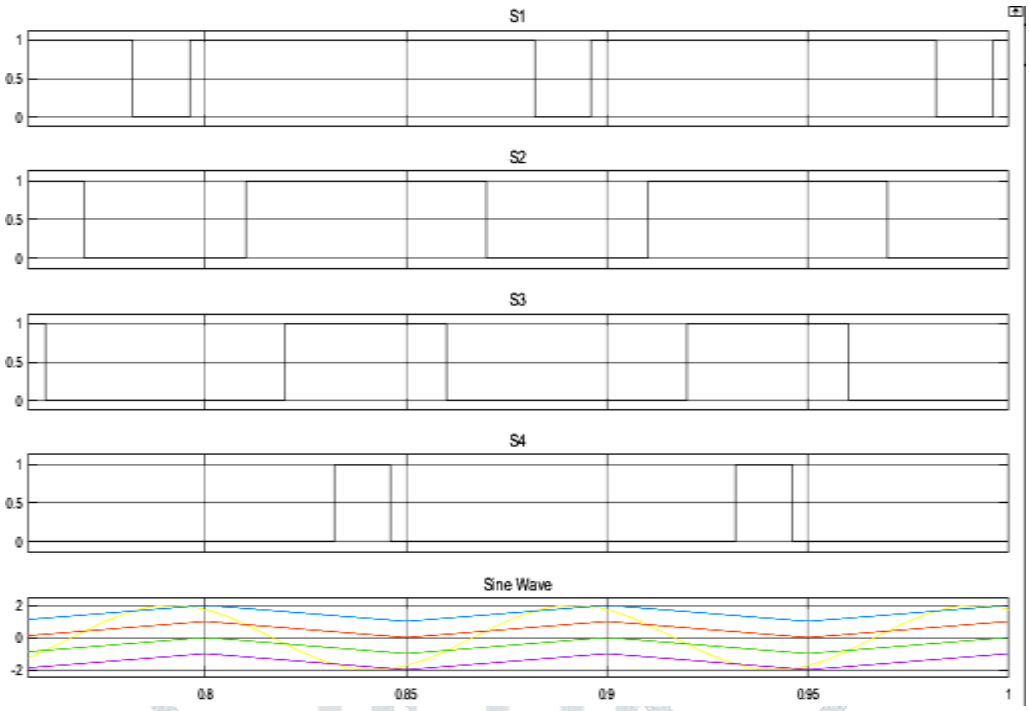

Figure 5: Switching Sequence shifted 120’

Figure 5 is showing the switching sequence of S1, S2, S3 and S4. A switching sequence formed by several switching states of the converter is performed and the average value of the output voltage must coincide with the desired reference.

Case –III

The waveform simulated value is assigned for sine wave and S1, S2, S3 and S4 carrier wave. The phase angle in rad is -2*pi/3 or -120’ phase shift.

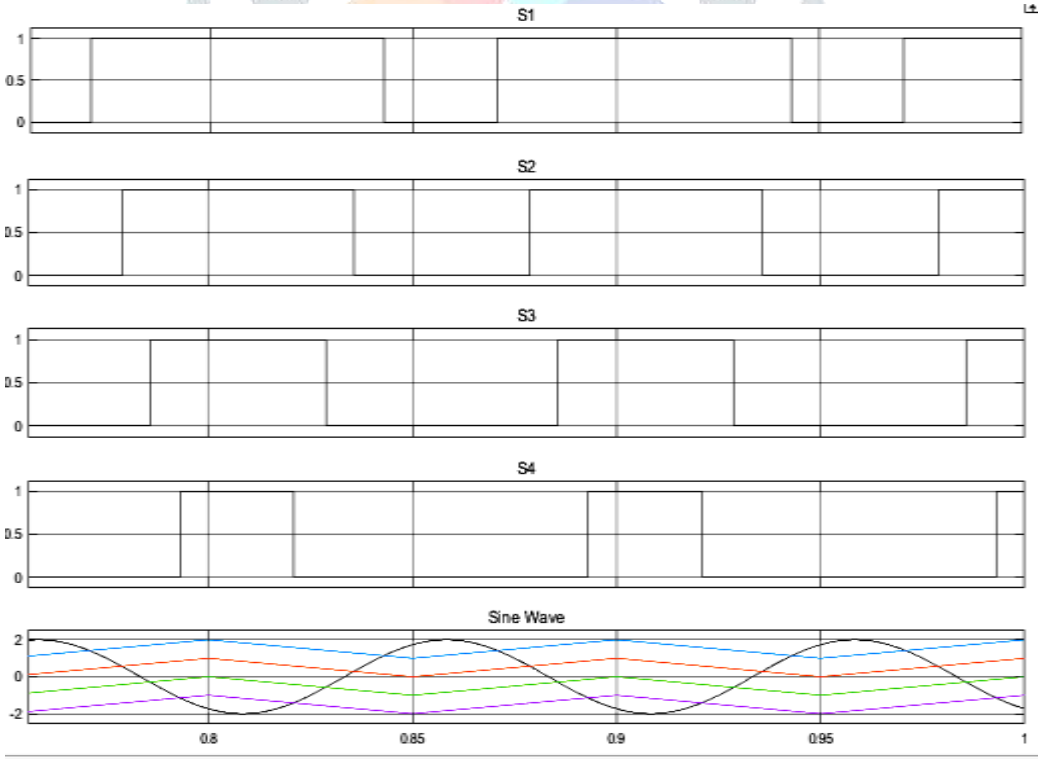

Figure 6: Switching Sequence shifted -120’

Figure 6 is showing the switching sequence of S1, S2, S3 and S4. A switching sequence formed by several switching states of the converter is performed and the average value of the output voltage must coincide with the desired reference.

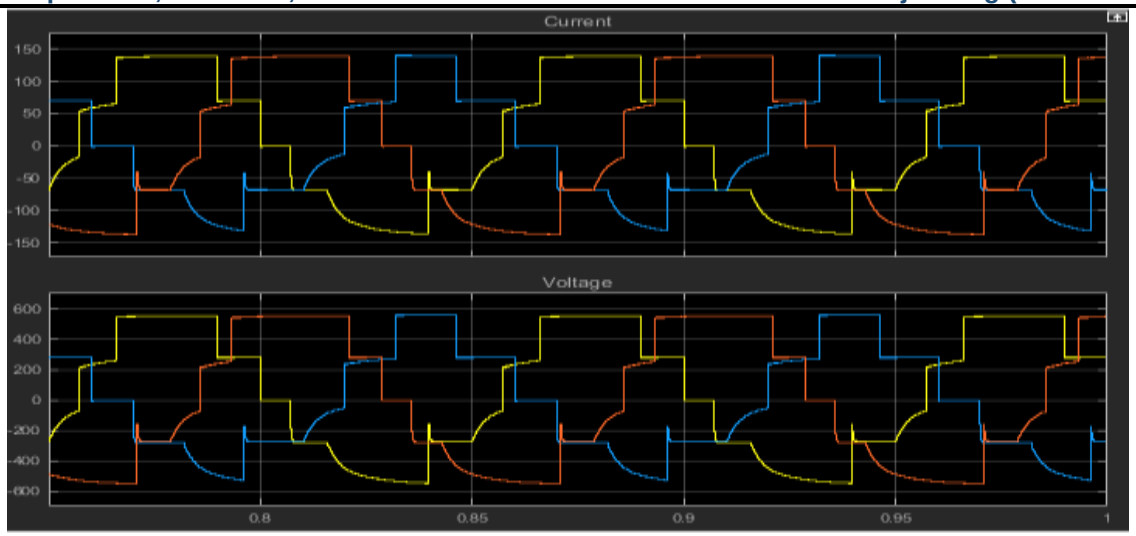

Figure 7: Inverter Output

Figure 7 is showing the multilevel inverter output current and voltage. The output voltage is 550 Voltage and current is 140 A.

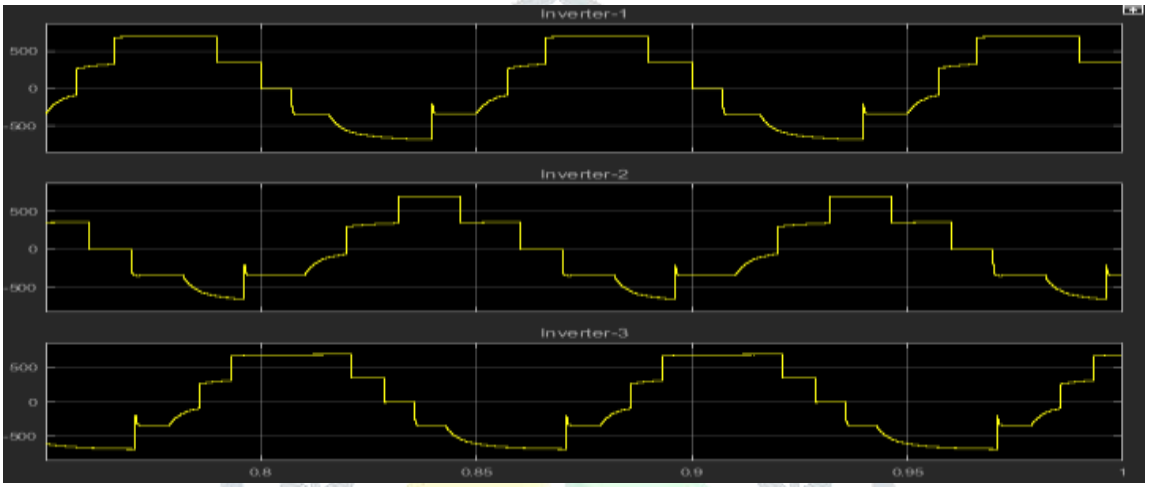

Figure 8: Inverter Voltage

Figure 8 is showing the multilevel inverter cases output voltage. All three cases have approx 550Voltage at different angle.

Solar Irradiance of PV1

In this subsection, after keeping the starting input conditions of the PV modules at 1000W/m^2 irradiance and 25'C temperature, the temperature of PV1 is changed to 35'C.

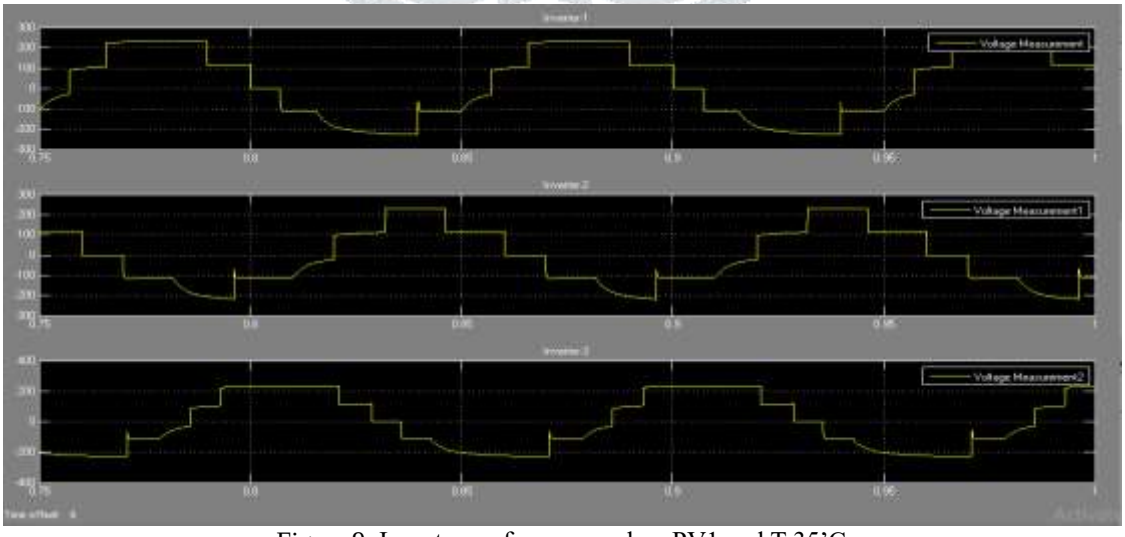

Figure 9: Inverter performance when PV1 and T 35'C

In this condition conditions consider the solar irradiance of the module PV1 is changed from 1000 to 600W/m^2.

Step Change in Temperature of PV 2A

The temperature of PV2A is changed from 25'C to 35'C in this subsection.

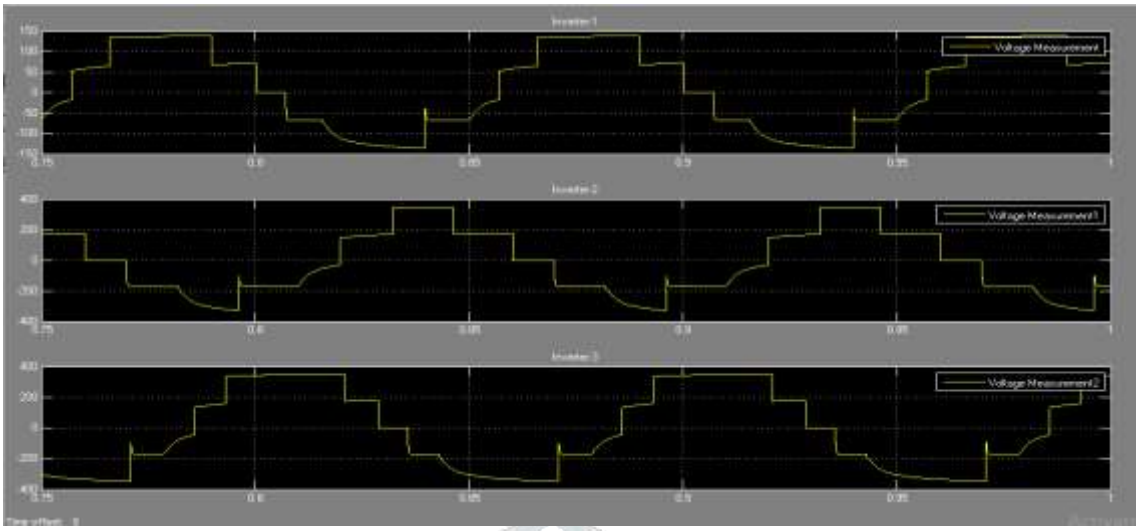

Figure 10: Inverter performance when PV2A and T 35'C

Step Change in Solar Irradiance and Temperature of PV 1

In this subsection, both solar irradiance and temperature of $PV1$ are varied from $1000 W/m^2$ and $25'C$ to $600 W/m^2$ and $35'C$

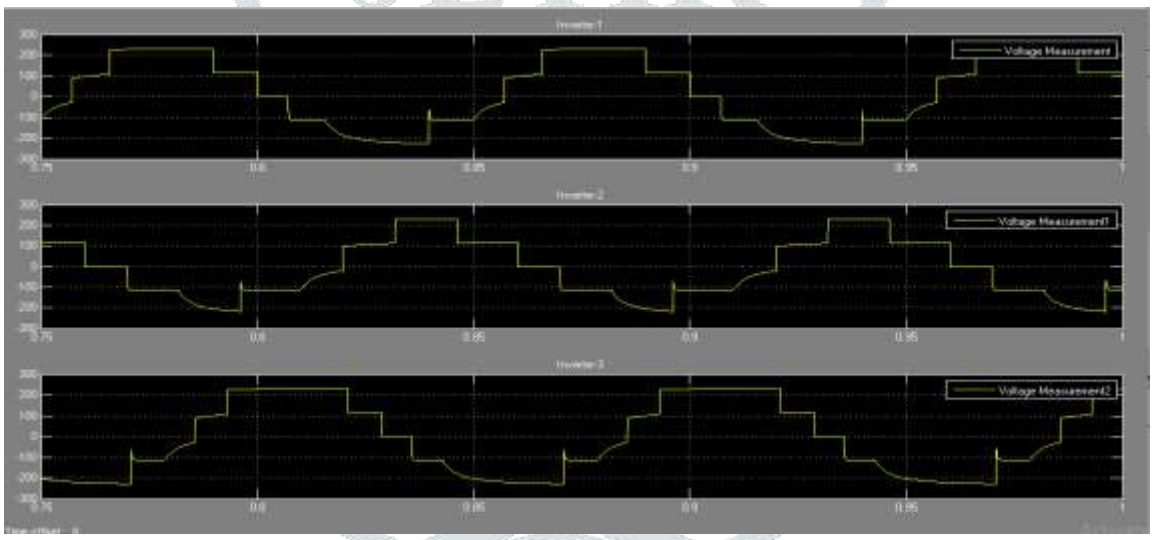

Figure 11: Inverter performance when PV1 $1000 W/m^2$ and $25'C$ to $600 W/m^2$ and $35'C$

Table 1: Simulation parameters

Sr No.	Parameters	Proposed Work
1	PV irradiance	1000 W/m^2
2	Switch	3 MOSFET and 12 IGBT
3	Inverter output voltage	550 V
4	Inverter output current	140 A
5	Inverter voltage 0 angle	550V
6	Inverter voltage +120 angle	550V
7	Inverter voltage -120 angle	550V

Table 2: Result Comparison

Sr No.	Parameters	Previous Work [8]	Proposed Work
1	Methodology	Grid Connected Photovoltaic Systems	SVM based PWM
2	Switch per level	6	5
3	Switch type	MOSFET and IGBT	MOSFET and IGBT
4	Power (W)	600	770

V. CONCLUSION

This paper presents design and analysis of 5-level cascaded H-bridge multilevel inverter with photovoltaic system. The simulated outcomes shows that the MPPT productivity, inverter effectiveness, and in general proficiency which are developed as reproduction system. The simulation is performed using MATLAB-SIMULINK software. Therefore it is clear from the simulated results that the proposed model gives significant better results than existing work in terms of the switch per level, power generation.

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