JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue

JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)

An International Scholarly Open Access, Peer-reviewed, Refereed Journal

Analyzes the performance of Solar PV-BESS connected to MLI-UPQC with Fuzzy Logic Controller

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ABSTRACT:

This study examines the design and performance of a UPQC that has built-in shunt and series controllers. The UPQC is used to improve the quality of power-related distortions such as voltage sags and swells, as well as harmonics that are caused by non-linear grid loads. Solar PV and Energy Storage Systems can be used to provide electricity to UPQC. Solar PV actually gives active power to the loads. However, due to climatic conditions, solar power may not be consistent at all times. As a result, there may be some power supply distortions, at which point the Battery Energy Storage Systems will kick in and give power to the load, especially during long-term voltage outages. As a result, the BESS's voltage support capability can be enhanced, reducing the voltage regulation algorithm's complexity in the long run. In order to regain the enhanced power quality, simulations for multilayer inverters with PI controllers and multilevel inverters with fuzzy logic controllers are performed in this article. The suggested system will reduce harmonics and improve system performance to a suitable level. The simulation results of this proposed method can be performed by using MATLAB/SIMULINK Software.

Keywords:-Battery Energy Storage System, Multilevel Inverters, PV (Solar Photovoltaic), Quality of Power, UPQC (Unified Power Quality Conditioner), FLC (Fuzzy Logic Controller).

I. Introduction:

Conventional huge scope centralized electricity generation incorporates non-renewable energy source terminated power plants, thermal energy stations, hydroelectric dams, wind ranches, etc. These are presently overwhelmed by a shortage of non-renewable energy sources, inordinate outflows, and blackouts brought about by lengthy transmission lines [1]. When voltage and frequency are taken into account, "Quality of Power" refers to an electrical framework's ability to deliver an ideal power supply with an unadulterated commotion free sinusoidal wave shape that is constant 100 percent of the time. In any case, almost all loads will produce normal unsettling effects in the structures, resulting in deviations from the ideal power supply [2]. EPRI led a review in the United States somewhere in the range of 1992 and 1997 to decide the normal length of unsettling influences.Many devices, such as dynamic voltage restorers (DSTATCOM) and UPQC, which are also known as power quality improving devices, are available to enhance and compensate the quality of power related problems caused by using loads and to protect sensitive loads from grid side voltage quality issues. DSTATCOM [3] is a shunt-connected power electronic system that compensates for power quality problems caused by system loads such as reactive current, harmonics, and load imbalance. DVR's are used to compensate for grid voltage sags and swells in the power electronic topology [4]. DSTATCOM and DVR are joined to frame an UPQC [5], which comprises of a consecutive associated shunt and a series compensator. Consequently, while the geography of the SeAF and DVR is comparable, their control approach recognizes them [6], with the distinction in view of the application errands. The HSeAF Hybrid series

dynamic channel is suggested for tending to both voltage and recent concerns. In principle, the HSeAF (Hybrid series dynamic channel) will dispense with voltage contortions at the PCC, make up for sounds in the framework, and accomplish great power quality [7]. Most of the exploration has focused on three-stage HSeAFs, with a couple of cutting edge examinations on their single-stage application. PV frameworks have been joined with bound together power quality conditioners (UPQC) [6-7]. The series dynamic power channel is utilized to make up for power quality issues, which is a significant capacity of UPQC, and the test consequences of the single-stage PV framework incorporated with UPQC just fill the role of a DVR, permitting them to go about as both a series dynamic power channel (S-APF) making up for mains voltages and an equal APF (P-APF) making up for load flows. The SPV-UPQC-P, a double-stage PV system incorporated with UPQC, was assessed exclusively involving virtual simulations in [9].This system, on the other hand, only compensates for imbalances in load reactive power and grid voltage [11]. As a result, no consideration has been given to the destruction of grid voltage and load fault current. This paper proposes a Solar PV and BES system coordinated UPQC with Fuzzy Logic Controller to overcome power quality issues, reduce harmonics, and increase system response speed

II. System Modelling and Analysis

The structure of Photovoltaic-Battery Energy Storage System- Unified Power Quality Conditioneris portrayed in Figure-1. The three phase system is made for the Photovoltaic-Battery Energy Storage System based Unified Power Quality Conditioner model. The PV-BESS-UPQC is planned by utilizing a series and shunt APF compensators that are related by a DC-Link Split Capacitor. The PV System and Battery Energy Storage System are associated in comparing to the DC-Link. A lift converter interfaces the PV to the DC-connect. Also, the BESS is connected to the DC-interface by means of a buck-support converter. The series compensator works in basically the same manner to a controlled voltage source in that it decreases supply voltage hangs, grows, interferences, and voltage music. The shunt compensator, then again, decreases the current music of the heap. The series and shunt APF compensators are associated by communicating inductors [5-6].

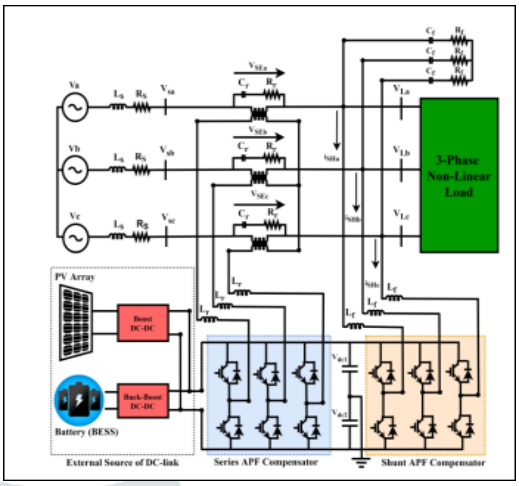

FIGURE 1. UPQC system configuration

Harmonics are generated as a result of the converter switching action and are removed using a ripple filter. The voltage was injected into the grid via a series injection transformer by using a series compensator. In this research work a three phase non-linear load is employed. The PV-BESS-UPQC configuration process starts with an exact estimation of the PV exhibit, split capacitor, DC-interface reference voltage, and different parts. The shunt compensator is built in. Harmonics are produced as a result of the switching action of the converter and are removed using a ripple filter. The shunt compensator is intended to control the PV array's peak output power while also mitigating current harmonics.

III. Designing of PV-BESS based UPQC:

The designing of Photovoltaic system, Battery Energy Storage system based UPQC system consists of thebuck-boost and boost converters and controllers are all incorporated in the system model as shown in Fig. 2. The Battery Energy Storage System is associated with a buck-help converter DC Link capacitor which is associated in equal for working on the productivity and dependability of UPQC simultaneously to lessen the power quality related issues. Absolute power stream is indicated in the model as (7).

$$\boldsymbol{P_{total} = P_{pv} + P_{BESS} - P_{LoadDC-link}} \quad (1)$$

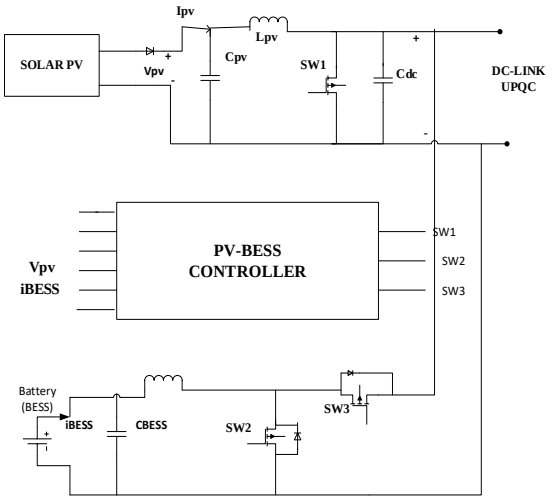

FIGURE 2. PV-BESS system configuration

IV. Simulating of Photovoltaic System:

The Photovoltaic model is taken from the library of "Simulink" has utilized in this work. The PV model is made up of PV module strings that are connected in parallel. Mainly the construction of this PV module is aimed to attain the I_{pv}, V_{pv}, P_{pv} (current, voltage and the power)ratings as per our requirement. MPPTcan be used to under certain irradiance and temperature conditions for the increment in efficiency of a PV module. The duty cycle of the connected DC-DC boost Converter will have the pulses that are generated by the MPPT algorithm. Many types of MPPT techniques are classified. But we will consider only perturb and observe (P & O) in this implementation work. Because it is more accurate to track the maximum power precisely in this work. The P & O algorithm can be implemented as shown in below flowchart (3).

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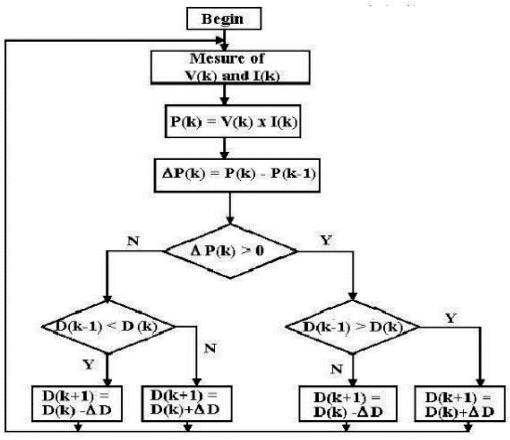


FIGURE 3. Perturb & Observe Algorithm Flow Chart

The controller that is controlling the step-up converter(DC-DC boost converter) is as shown in figure 4, which is used to improve the power of PV system. The DC-DC boost converter controller receives a DC voltage error, V_{DC}, and then operates. The voltage error is calculated by comparing it to the reference voltage, Vref, which is set to 700V. The instantaneous DC-DC Boost converter output DC voltage V_{DC} is used as the reference voltage. Then, $_{VDC,\ error\ (t)}$) is approximated by using a PI controller to reduce $V_{DC,error\ (t)}$. Mathematically, the approximation can be deduced from (8) and (9):

$$V_{DC,error}\ * = K_{p,1}\left(V_{DC,error}(t)\right).dt + K_{i,1}\int_0^t \left(V_{DC,error}(t)\right).dt \quad (2)$$

$$V_{DC,error}(t) = V_{ref} + V_{DC}(t) \quad (3)$$

Where $k_{p,1}$ and $k_{i,1}$ are two constants that represent the PI_1 controller's proportional and integral gains, respectively. In that order, the values are 0.1 and 0.1. In this PV-BESS topology, due to overcharging of can shorten he life of the battery. So, to overcome this the DC-DC step-up converter's topology is utilized in the system to make the battery system stable and restricts it from getting over charged.

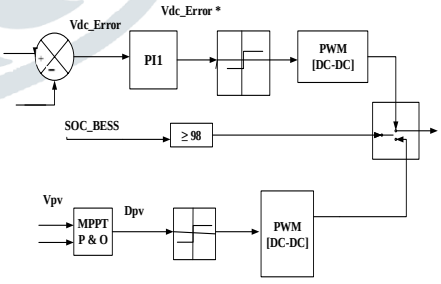


FIGURE 4. Robust Controller for PV DC-DC Boost Converters

V.BATTERY ENERGY STORAGE SYSTEM MODELLING

Batteries are typically made up of one or more electrochemical cells that are linked either in parallel/ series for BESS modelling. In general, battery models are categorized on the basis of models of electrochemical and electrical circuit and the rest of the models are usually derived from these models. For example, integrating current improves

the Peukert's equation model of a battery. The equation of Stepherd is also an electrochemical model. Because of efficient tools such as MATLAB/SIMULINK, a mathematical model is used in this work. Among all of these batteries, Lithium-Ion battery is considered because of its high density and energy of power and has a low maintenance cost.

a) Controlling topology of a PV-BESS

Figure 5 shows a bidirectional Buck-Boost DC-DC controller with embedded internal and external control loops for charging and discharging.

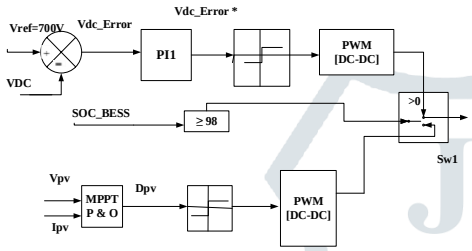


FIGURE 5. Controlling scheme of BESS based Buck-Boost Converter

Active power provided by a properly configured external control with a frequency droop, i.e., fdroop, keeps the frequency stable. The internal control loop is made up of two parts: a voltage control loop for system voltage stabilization and a current control loop for adjusting the filter output current for quick dynamic response. The measured PV dc link voltage (VDC) is contrasted to the reference DC Link voltage (VDC, ref), and the difference is sent to the voltage controller outer loop via the PI_2 controller to yield current reference. The method is mathematically expressed as follows: (10) and (11)

$$.V_{DC,error}(t) = V_{ref}V_{DCref} * (t) \quad (4)$$

$$i_{t,ref} = K_{P,2}\left(V_{DC,error}(t)\right) + K_{i,2}\int_0^t (V_{DC,error}(t))dt \quad (5)$$

Where $k_{p,2}$ and $k_{i,2}$ are the two fixed values that represent the PI_2 controller's proportional and integral gains. The values are 1.477 and 3077, respectively. When the PV module's active power falls below a certain threshold, the voltage frequency components fall below a certain threshold. The gate's BESS and lower frequency components are delivered for a DC-DC converter in discharging modes that are generated.

VI. Working of Fuzzy Logic Controller based PV-BESS-UPQC

A. Synchronization Technique of STF-UVG

To extract the synchronization phases from the supply voltage, the proposed STF-UVG technique employs a simple, non-iterative method. The below figure (6) provides the STF technique which is some part of the UPQC. The three-phase voltage supply is represented in a matrix form, and for the conversion of source voltage from the abc to $\alpha\beta 0$ Clarke transformation matrix is utilized[1–4].

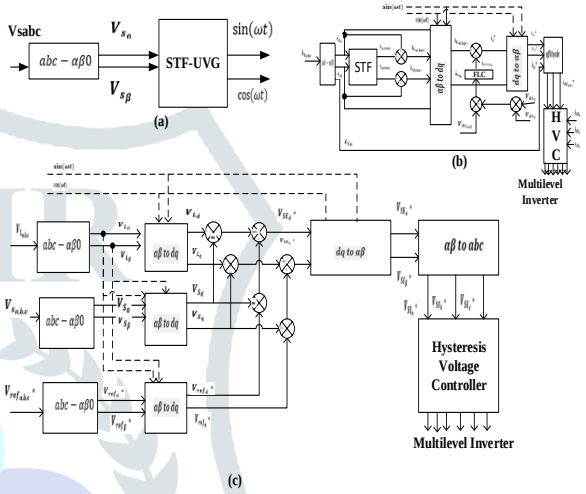


FIGURE 6. Block diagram of STF when it has a FLC Controller (A) Self Tuning Filter-UVG (B) controlling scheme of Shunt APF (C) controlling scheme of Series APF

In the $\alpha\beta$-domain,consideration of only two phases will takes place.The formation of fundamental and harmonic components can takes place with supply voltage when it is distorted. The relationship is portrayed in (12).

$$\begin{matrix} V_{s\alpha} \\ V_{s\beta} \end{matrix} = \begin{matrix} V_{s\alpha(fund)} \\ V_{s\beta(fund)} \end{matrix} + \begin{matrix} V_{s\alpha(har)} \\ V_{s\beta(har)} \end{matrix} \quad (6)$$

The STF method is used to extract the fundamental components. By using of this method the harmonic components in the system can be suppressed. As a result, phases of synchronization are removed with greater precision, and the extraction quality is enhanced.

$$\begin{matrix} V_{s\alpha(fund)S} \\ V_{s\beta(fund)S} \end{matrix} = \frac{K_1}{S}\begin{bmatrix} V_{s\alpha\ S} \\ V_{s\beta\ S} \end{bmatrix} - \begin{matrix} V_{s\alpha(fund)S} \\ V_{s\beta(fund)S} \end{matrix} + \frac{2\pi F_{C1}}{S}\begin{bmatrix} -V_{s\beta(fund)S} \\ V_{s\alpha(fund)S} \end{bmatrix} \quad (7)$$

Constant gain parameter will be denoted by K_1, and f_{c1} represents the frequency at cut-off region. The K1 rating is estimated to be between 20 and 80, whereas the fc1 rating is determined by the system frequency. The rating for K_1 in this project is estimated to be 20 Hz, and the rating for f_{c1} is estimated to be 50 Hz. The working of a phase locked loop element (PLL) will be overcomes by using a technique known as UVG andin UPQC topology the phases of synchronization will be engendered effectively and efficiently while the distortions in the supply voltage are still in the process.

B. Controlling and Compensation of Series APF

The frequency and phase information of STF-UVG can be used to In abc-domain the reference voltage signal $V_{ref,\ abc}$which is connected in three-phase can be calculated by using frequency and phase information of STF-UVG as mentioned in (13) The maximum peak voltage magnitude, Vm, max peak, is calculated using the fundamental load voltage's peak amplitude. The supply voltage and reference voltages are should be in phase with PCC. With the d-frames representing the peak amplitude load reference voltage and the q-frames representing zero.

$$\begin{matrix} V_{refa}\ * \\ V_{refb}\ * \\ V_{refc}\ * \end{matrix} = V_{m_{max-peak}} \begin{bmatrix} \sin(wt) \\ \sin\left(wt - \frac{2\pi}{3}\right) \\ \sin\left(wt + \frac{2\pi}{3}\right) \end{bmatrix} \quad (8)$$

By using this STF-UVG the generation of phases of which are synchronized and distorted voltage supply at PCC for the fundamental component can be extracted and the obtained frequency is utilized to achieve the axis of reference in the frames of dq to generate the axis of reference in the dq-frames. In the dq-frames, the reference voltage signal is acquired with only two phases and the Park transformation matrix.

C. Controlling and Compensation of Shunt APF

To extract the harmonic component of the load current, the suggested STF on -domain is used. The load current i_L signal can be divided into fundamental and harmonic components by focusing on the $\alpha\beta$-domain. The rating for K_1 in this project is estimated to be 20 Hz, and the rating for fc_1 is estimated to be 50 Hz. In this controlled topology utilized dq-axis currents. Therefore the conversion of $\alpha\beta$ into dq-frame is shown in equation (9):

$$i_{lq} = i_{l\alpha} \cos(wt) + i_{l\beta} \sin(wt) \quad (9)$$

There is no need for transformation in the $\alpha\beta$0-domain. The magnitude of the fundamental current at load side is denoted by the d-DC frame component, whereas the magnitude of the harmonic current is denoted by the oscillating AC frame component.

The PI controller error $e_{1(t)}$ between reference dc-link voltage V_{dc} and total instantaneous dc-link voltage is then reduced to calculate $i_{error,\ dc}$(15) and (16) provide the arithmetic calculation (16),

$$i_{errordc} = k_{p,4}\, e1(t) + k_{i,4} \int_0^t e1(t)dt \quad (10)$$

$$e_1(t) = V_{dc,ref} - \left(V_{Cap1}(t) + V_{Cap2}(t)\right) \quad (11)$$

In PI4 controller the proportional gain is denoted by $k_{p,4}$=0.3 and the integral gain is denoted by K_{i4}=2. By using these values we can attain reference current if grid in the frame of dq, which is as follows:

$$i_{L_d} * = i_{L_{d(har)}} - i_{errordc} \quad (12)$$

Following that, the current signals $i_{L,d}$and $i_{L,q}$are changed into abc-domain by injecting the currents of Grid. Combining (18) and yields the reference current $I_{sH,abc}$(19). In the shunt converter to engender the gate pulses the comparison in between the reference supply currents and measured supply currents need to be done.

$$\begin{matrix} i_{L_d}\ * \\ i_{L_\beta}\ * \end{matrix} = \begin{bmatrix} \sin(wt) & \cos(wt) \\ -\cos(wt) & \sin(wt) \end{bmatrix} \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} \quad (13)$$

$$\begin{matrix} i_{SH\alpha}\ * \\ [i_{SHb}\ *] \\ i_{SHc}\ * \end{matrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{L\alpha}\ * \\ i_{L\beta}\ * \end{bmatrix} \quad (14)$$

VII. Multi-level converters with PI controller:

Multilevel inverters concept has been around the year 1975. Three level inverter was the main basis for the introduction of Multilevel Inverters. So, after introducing this multilevel inverters many different topologies has developed to provide the sufficient requirements in the system.The multilevel inverters/converters are composed of power semi-conductor switches with the lowest dc voltage

sources to execute power conversion by integrating a staircase voltage waveform.

a) Cascaded H-Bridge Inverters

The below figure will explains us about the structural arrangement of a cascaded H-bridge MLI. The H-bridge is formed by connecting separate source of DC to a single phase full-bridge inverter. In this topology different switches like S_1, S_2, and S_3& S_4 are operated by using DC source to the output of AC. This combined topology will form an inverter. So, this each inverter level can produce 3-types of voltages like $+V_{dc}$, 0, $-V_{dc}$. $+V_{dc}$ will be turned on by switches $S_1$and S_2 whereas $-V_{dc}$ will be turned by using S_2 and S_3 switches. When all the four switches are in ON position, then the voltage at output is zero. The rotating current results of the various full-bridge inverter levels are connected in series, resulting in a voltage waveform that approaches the amount of inverter output. In this topology m=2s+1 is known as the phase voltage level of output which are in-builted in a cascaded H-bridge inverter. The Van is known as the phase voltage Van i.e., is equal to all the voltages in the circuit:-Van=V_{a1}+V_{a2}+V_{a3}+V_{a4}+V_{a5}.The below figure 7 will tells us about the 11-level H-Bridge MLI

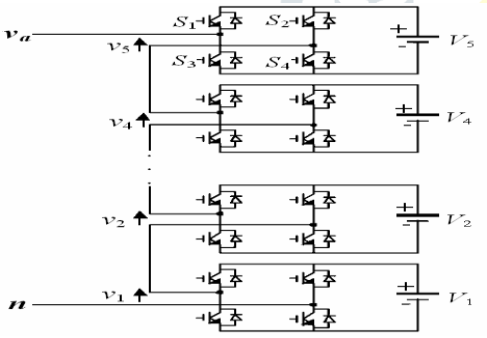


Fig 7. Layout of a H-bridge MLI

b) MLI with Fuzzy Logic Controller:

The mathematical method which is sophisticated for solving problems of simulation with a numerous inputs and outputs variables, that method is known as Fuzzy Logic method. The Fuzzy Logic Controller (FLC) can offer the critical and specific logics like Boolean algebra. This research provides anelementarysummary of fuzzy logic principles. Today, mathematical models that obey physical laws, stochastic models, or models derived from mathematical logic are commonly used to describe control systems. The commoneffort of such a model is determining how to proceed from a given tricky to a suitable calculatedexemplary. Without a question, today's advanced computer technology allows it; however, managing such systems remains incredibly hard [14-[15].

Figure 10 depicts the four major components inFLC system: the fuzzification interface, the fuzzy inference engine, the fuzzy rule matrix, and the defuzzification interface.

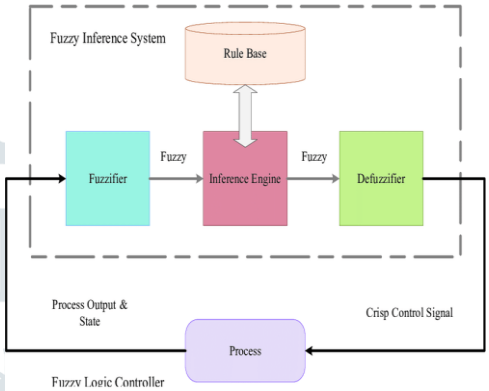


Figure 8. Fuzzy logic controller

The figure below depicts the Fuzzy Logic Controller's membership functions. There are two inputs considered, error in figure (9) and change in error in figure (10), and the outputis displayed in figure (11).

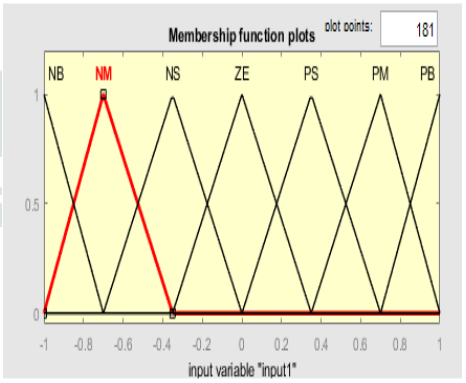


Figure (9): error

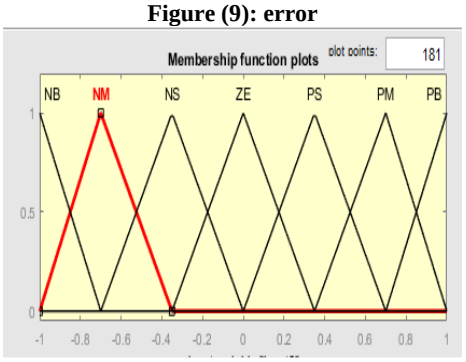


Figure (10): change in error

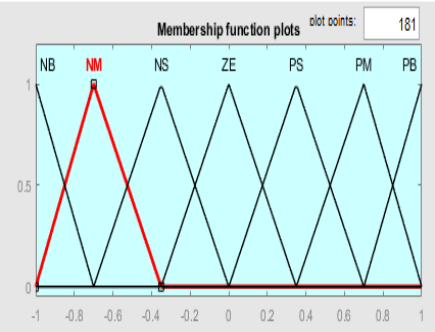


Figure (11): output

Table 2: Rules of FLC

CE/E	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

The above table consists of the 7x7=49 rules, whereas

Negative Big=NB; Negative Medium=NM; Negative Small=NS; Zero Error=ZE; Positive Small=PS; Positive Medium=PM; Positive Big=PB.

VIII. SIMULATION RESULTS:

Multilevel Inverter with Fuzzy Logic Controller:

Case-1:

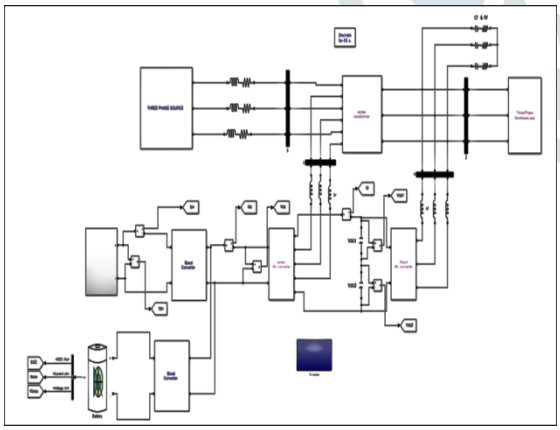
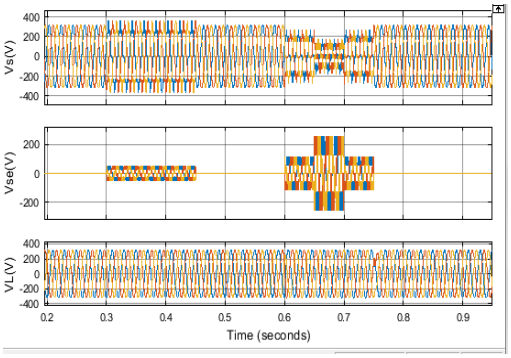
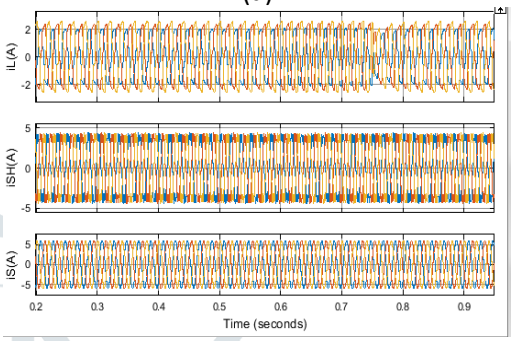


Fig 12: simulation model of case-1

The above figure depicts the performance of a UPQC built with a multi-level inverter and a FLC in the regard of voltage harmonics at PCC and the harmonic-sag combination. The case study is carried out without the BESS and PV being connected.



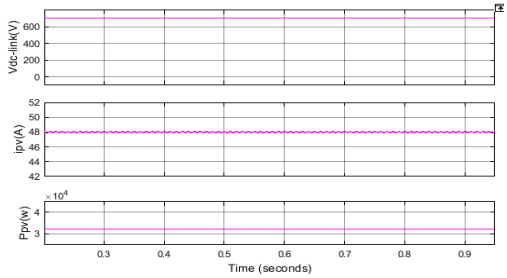
(a)



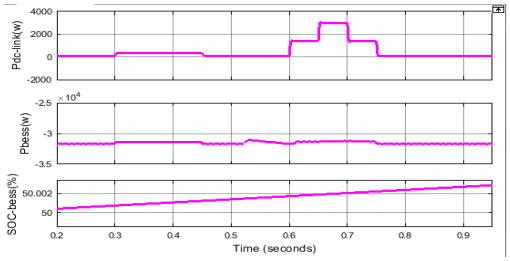
(b)

Fig 13(a) Voltage waveforms of Source, Injected series APF and Load & (b) Currents waveforms of Source, Injected shunt APF and Load

As obtained in the above figure (13) A- indicates the V_{DC} (DC link voltage) remains unchanged at a value of 700V in case study-1. The current of PV is approximately equal to the 46.2 A which is mentioned in the figure 13(B) and the P_{PV} is 32 KW. In Fig. 13(c), the P_{DC}(power at DC Link) is increased from 0.3s to 0.45s to compensate for voltage harmonics 13(D). Furthermore, the DC power is increased from 0.6s to 0.75s, which allows harmonics to be reduced and the load to be supported even when the source voltage is insufficient. The P_{BESS} (power of the Battery Energy Storage System) is shown in 13(E), and when harmonics and sag occur due to an increase in BESS current, the power of the BESS is slightly increased during 0.3s to 0.45s, and alsofrom 0.6s to 0.75s. Fig. 13(F) depicts the SOC(state of charge), and the operation of charging of the BESS can be observed throughout the process.



(a)



(b)

FIGURE 14. (a) Waveforms-SOC of BESS, DC Link o/p power, BESS power & (b) Waveforms-Power and current of PV, voltage at DC Link

As obtained in the above figure (14) A- indicates the voltage of DC link remains unchanged at a value of 700V at the combination of voltage sag and harmonic condition. The current of PV is approximately equal to the 46.2 A which is mentioned in the figure 14(B) and the power of PV is 32 KW. In Fig. 14(c), the power at DC Link is increased from 0.3s to 0.45s to compensate for voltage harmonics 14(D). Furthermore, the DC power is increased from 0.6s to 0.75s, which allows harmonics to be reduced and the load to be supported even when the source voltage is insufficient. The power of the Battery Energy Storage System is shown in 14(E), we can observe the slight increment in the power of BESS for the period of 0.3s to 0.4s and 0.6s to 0.75s when harmonics and sag occur due to an increase in BESS current. Fig. 14(F) depicts the state of charge (SOC), and the operation of charging of the BESS can be observed throughout the process.

Case-ii

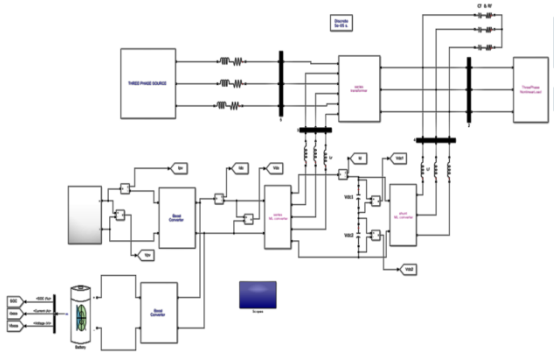
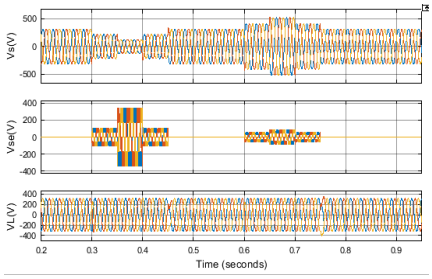
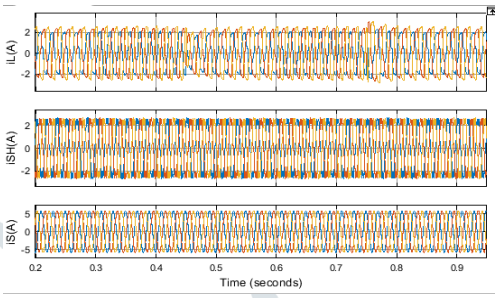


Fig 15: Simulation Model for case-ii

The graph above depicts the performance of a UPQC built with a multilevel inverter and a fuzzy logic controller when subjected to PCC voltage harmonics and the combination of harmonic and sag. The case study is carried out in the absence of the PV and BESS.



(a)



(b)

FIGURE Fig 16 (a) Voltage waveforms of Source, Injected series APF and Load & (b) Currents waveforms of Source, Injected shunt APF and Load

As obtained in the above figure (16) A- indicates the voltage of DC link remains unchanged at a value of 700V at the combination of voltage sag and harmonic condition. The current of PV is approximately equal to the 46.2 A which is mentioned in the figure 16(B) and theP_{pv} (power of PV)is 32 KW. In Fig. 16(c), we can observe the slight increment in the power of BESS for the period of 0.3s to 0.4s and 0.6s to 0.75s which allows harmonics to be reduced and the load to be supported even when the source voltage is insufficient. The power of the Battery Energy Storage System is shown in 16(E), and when harmonics and sag occur due to an increase in BESS current, the power of the BESS is slightly increased during 0.3s to 0.45s, and the power of the BESS is slightly increased during 0.6s to 0.75s. Fig. 16(F) depicts the SOC (state of charge), and the operation of charging of the BESS can be observed throughout the process.

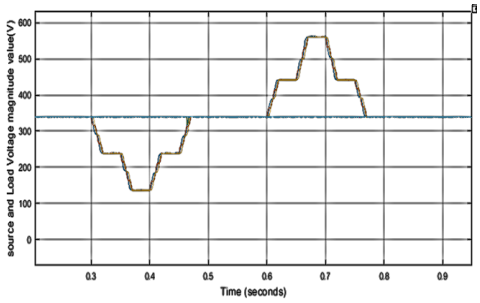


FIGURE 17. Detected Voltage (Case study-2)

The simulation is performed by taking the Time V_s voltages of the Source and Load into account, as shown in the above figure. When the waves are subjected to the operation, we can also see how they form.

Comparison Table of Total Harmonic Distortion for PI and Fuzzy Logic Controllers:

Case study-1(with PV-BESS)

parameter	2-level Inverter	MLI with PI	MLI with Fuzzy
current (harmonics injected into the supply)	2.51%	1.60%	1.36%
current (harmonics injected into the supply and sag condition)	2.48%	1.60%	1.36%
voltage	0.52%(condition)	0.52%(condition)	0.52%(condition)

According to Case Study-1, i.e. the current (harmonics injected into the supply) the 2-level inverter has 2.51 percent THD, the multilevel inverter with PI controller has 1.60 percent THD, and the multilevel inverter with Fuzzy controller has 1.36 percent THD. In the condition of current (harmonics injected into the supply and sag condition)is 2.48 percent in a 2-level inverter, 1.60 percent in a MLI with PI controller, and 1.36 percent in a MLI with FLC. In the Voltage condition, however, all THD values obtained are the same, i.e., 0.52 percent for all techniques used in this paper.

Case study-2(with PV-BESS) part-a: That shows equal Sags and Swells of Voltage

Parameter	2-level inverter	MLI with PI	MLI with fuzzy
Under Balanced sag & swell condition for current	2.51%	1.11%	0.65%
THD under the condition of voltage sag of current	2.53%	1.10%	0.64%
voltage	0.52%(condition)	0.52%(condition)	0.52%(condition)

From the above Case Study-2 the scenario A can be explained as THD for balanced voltage sags and swells and their parameters will be as Under Balanced sag & swell condition for currentthe 2-level inverter has 2.51% of THD,and MLI with PI controller has 1.11% of THD whereas in MLI with FLC the THD value is decreased to 0.65%. In the condition of THD under the condition of voltage sag of current islike 2.53% in 2-level inverter, 1.10% in multilevel inverter with PI controller, The current under voltage harmonic condition, the 2-level inverter has 2.51 percent of THD, the multilevel inverter with PI controller has 1.11 percent of THD, and the multilevel inverter with Fuzzy controller has 0.65 percent of THD. In the condition of THD of current which is considered under voltage harmonic with the condition of sag is 2.53 percent in a 2-level inverter, 1.10 percent in a MLI with PI controller, and 0.64 percent in a MLI with FLC. However, in the Voltage condition, all THD values obtained are the same, namely 0.52 percent for all techniques used in this paper. The FLC (Fuzzy Logic Controller) produces the best results among all.

Case study-2(with PV-BESS) part-b: That shows unequal Sags and Swells of Voltage

parameter	2-level Inverter	MLI with PI	MLI with Fuzzy
Under UnBalanced sag & swell condition for current	2.48%	1.47%	1.31%
THD under the condition of voltage swell of current	2.48%	1.51%	1.33%
voltage	0.53%(condition)	0.53%(condition)	0.53%(condition)

From the above Case Study-2 the scenario B can be explained THD for unbalanced voltage sags and swells and their parameters will be as i.e. Under Un Balanced sag & swell condition for current condition the 2-level inverter has 2.48% of THD, and MLI with PI controller has 1.47% of THD whereas in MLI with FLC the THD value is decreased to 1.31%. THD under the condition of voltage swell of current values are like 2.48% in 2-level inverter, 1.10% in

multilevel inverter with PI controller, whereas the multilevel inverter with Fuzzy controller has 1.33%. But in the Voltage condition all the THD values obtained are same i.e., 0.53 for all the techniques used in this paper. Among all these the Fuzzy Logic Controller gives the best results.

IX. CONCLUSION:

Harmonic distortion, voltage sags and swells, voltage interruptions under unbalanced loads, and distorted grid voltage were all factors to consider when constructing a three-phase UPQC. With the integration of these Photovoltaic and Battery Energy Storage Systems, as well as UPQC, Active Power Distribution will be achieved in network conditions. Integrating the above three systems into one allows for the absorption and supply of active power in the system. Because renewable energy is not completely dependable due to its environmental reliance, implementing a BESS will help to alleviate renewable energy scarcity. As a result, the BESS's voltage support capability can be increased, and the voltage regulation algorithm's complexity can be reduced in the long term. Both PI and Fuzzy controllers, as well as PV-UPQC based BESS, are used in the proposed system's Series and Shunt Controllers to optimize system performance. The total harmonic distortion values of several controllers and multilevel inverters are compared at the end of this study. This research models multilayer inverters with PI controllers as well as multilevel inverters with fuzzy logic controllers in order to regain the increased power quality. To generate the simulation findings, the MATLAB/SIMULINK 2018a software was used.

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