JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

A HIGH PERFORMANCE GATE DIFFUSION INPUT TECHNIQUE BASED FULL SWING AND SCALABLE 1-BIT HYBRID FULL ADDER

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ABSTRACT:
A compact fluid cell is based on Gate Diffusion Input (GDI) and Conventional Complementary Metal-Oxide Semiconductor (CCMOS) then it is known as the Full Adder (FA) and these concepts were proposed for the task. Computer Aided Design (CAD) tool in a 45 nm CMOS process has been used for the simulation. Exceptional performance improvements were observed in the proposed design in terms of Product Delay (PDP) and speed. In order to test performance criterions on larger portions, the FAs were reduced and expanded to 32 bits. The five of the ten existing projects worked impeccably when they were expanded to 32 bits as well as the proposed design. Furthermore, the best performance criterion was achieved in large cascade circuits by the main proposed design. A FA is a complementary logic circuit that adds two input electrons into a sum of one's. The circuit consists of 3 1-input binary adding units, which are called "flippers". Each 1-input binary adding unit consists of first and second inverters having zero input bias voltage and one output with an intermediate state. When both of the two input electrons are "0", the first and second inverters will be off i.e., all their output voltages are zero. But when an input electron is a "1", its corresponding first and second inverters will turn on, providing an intermediate output voltage (V) for its summing up with second inverter. With this intermediate output voltage, the third inverter can cross add the binary numbers of these 1-input adding units to get their final binary sum which is called FA's sum.

KEY WORDS: GDI FA Cell, CCMOS, PDP, Low Power, CPL

INTRODUCTION:

The most widely and common used basic methods of arithmetic's in many systems of VLSI is the addition[3]. There are many other related functions in arithmetic which are calculation subtraction, address, multiplication, division, etc. It plays a huge and important role in VLSI for upgrading and designing a performance with the full 1-bit adder hence the use of binary adders is done for this task[4]. A wide variety of the full add-ons use mostly non-identical technologies and logical designs, and perhaps aimed for reducing power dissipation as well as increasing speed. In the recent years there is a huge expansion of portable digital equipments that requires effective and efficient processing in the tiny areas of silicon[3], the representation of the integrated circuits (IC) with appropriate operating criterion has been significant. Reduced low operating waves and supply voltages are popular ideas in reducing power consumption in IC's. Nevertheless, minimum years of volt voltages often lead to reduced drive current

and reduced operating frequencies resulting in more circuits with delays. For that reason, the solution for achieving improved performances of digital circuits relies heavily on overall design of circuits for functional circuits[1]. Therefore, energy-efficient design methods with the right speed have recently gained a great deal of interest among researchers in order to enhance the performance of modern digital circuits.

Adder as a whole is an integral part of arithmetic in microprocessors, VLSI and digital signal processing units. The Addition operation is considered as an essential arithmetic function for repetition, subtraction, division, and many other similar function. FAs are the important side based on many arithmetic works. In addition, 1-bit FA is considered basically in the overall structure for all designing add-ons[5]. Perhaps, There is a major impact on the overall performance of logic units and complex arithmetic due to the advanced design of FA. In this work, we introduce a new cascade approach to the FA with the Gate Diffusion Input strategy as well as the common CMOS concept. The FA effectiveness is confirmed in comparison with the other ten FAs are top notch. Performance test of FAs in large programs, all expanded into 32 bits.

EXISTING HYBRID FULL ADDERS:

For well organized circuits to meet the demand in present time portable devices, researchers used many FA cells. FA cells are thin film accumulators as an electrolyte. Based on logical design techniques, FAs can be divided into two main groups which are hybrid logic and single logic. FA using CPL is considered the main and the only first FA topology. Due to the issue of power outages, the use of CPL has become a major threat to modern power circuits. The CCMOS-based FA designing is simple, durable and has driving ability hence it is widely used in developed IC designs[5]. Perhaps, the issue remains with the high transistor calculation (TC), high input impedance and high power consumption[4]. CCMOS and CPL logic are taken as FAs with single logic because of the advantages for implementation of just one logic technique.

PROPOSED FULL ADDER DESIGN:

The GDI-based technique provides, above all, a low-power and high-speed circuit design with least Transistor Count, or power outages, which limit its broad application. To solve these restrictions, a hybrid of GDI and CCMOS has been developed in this paper. To reduce TC, this study uses GDI-based gates of logic on the side of input[1]. On the output side, the CCMOS logic produces power levels equal to the supply voltage (Vdd) and ground (Gnd)[2]. The suggested FA's representation that is designed and functionality are explained in the following paragraphs. To construct an FA, the logic interpretation must be carefully examined, and the interpretation can be observed using the entire adder truth table. If Cin is 0, Cout is an AND operation, and Sum is an XOR action. When Cin is 1, Cout is an OR operation, and Sum is an XNOR operation[1].As a result, FA implementation would necessitate the use of the AND-OR module for Cout creation and the XOR-XNOR module for Sum generation.

Table 1: Logic interpretation with GDI cell

Inputs for GDI Cell			Output	Function
G	P	Q		
A	V_{dd}	$\overline{B}$	$\overline{AB}$	NAND
A	$\overline{B}$	Gnd	$\overline{A+B}$	NOR
A	$\overline{B}$	B	$AB+\overline{A}\overline{B}$	XNOR
A	B	$\overline{B}$	$A\overline{B}+\overline{A}B$	XOR
C_{in}	A	B	$\overline{C_{in}}A+C_{in}B$	2:1 MUX

Figure 1 depicts the planned FA diagram. The suggested architecture uses the NAND-NOR gate as know (compliant AND-OR) and XNOR-XOR (conforming XOR- XNOR) modules as internal nodes instead of the AND-OR and XOR-XNOR modules. The GDI-based 2: 1 multiplexers(MUX) with NAND-NOR and

XNOR-XOR modules were added to the cascade to transfer the needed signals to the output terminals based on Cin[1]. Cout and Sum are calculated using the GDI-based network's results (compatible with Cout and Sum). The CCMOS converters transform the entire signals collected from the GDI network to produce Cout and the final sum in the final phase[1].

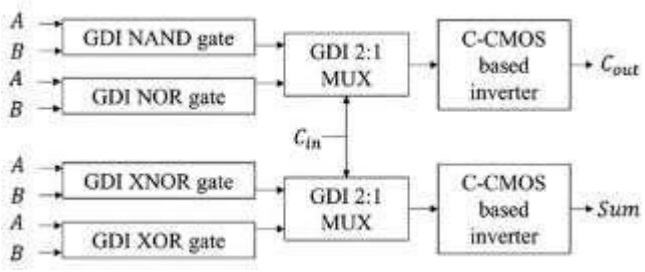

Figure 1 Block diagram of Proposed FA

According to the block diagram, the proposed FA is built with GDI gates. The NAND-NOR and XNOR-XOR modules provides intermediate signals that are utilized as a 2-1 data input: MUX. Cin picks the signals you wish to shift to the output terminals and is a part of MUXes (one Cout MUX and the other Sum)[1]. Finally, CCMOS inverters are employed to provide the full output desired.

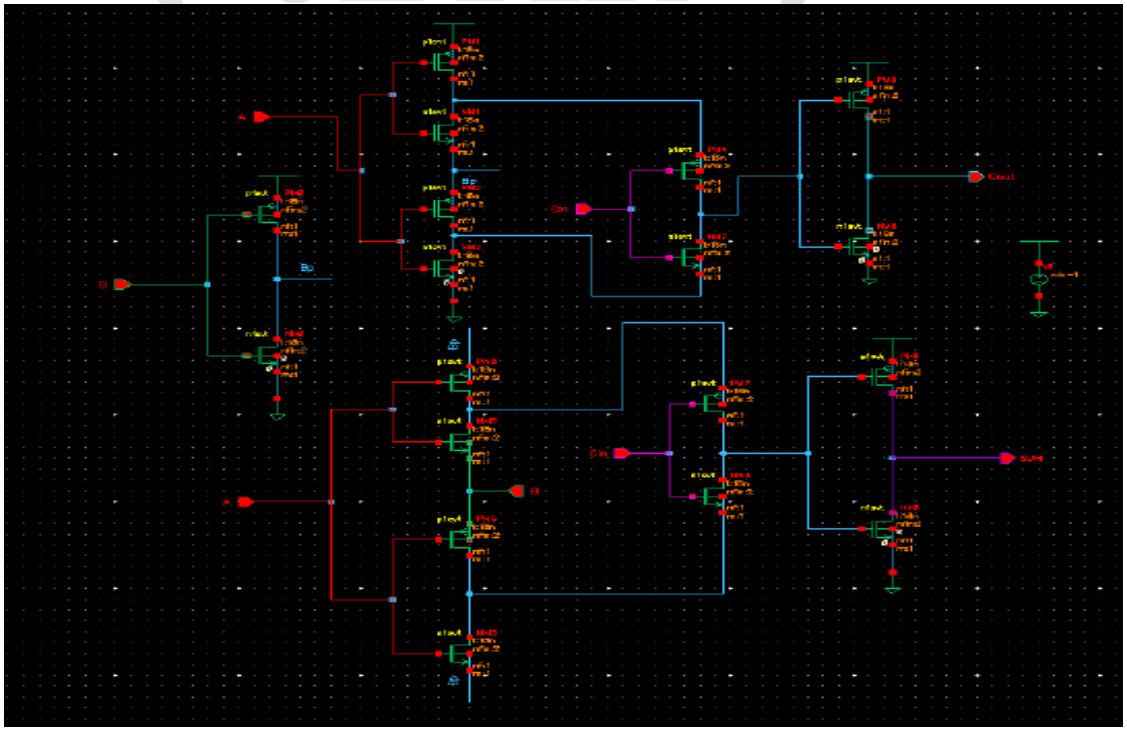

Figure 2 Schematic Diagram ofProposed FA

RESULTS:

Cadence Virtuoso was used to simulate all of the adders in 45nm gpdk CMOS technology. Different design methodologies are used to measure energy losses, delays, and power outages (PDP). These measurements are used to produce the designs of mathematical models of power supplies. This procedure aims to assess which design methodology is most conducive for evaluating voltage drop and decay phase losses in full adders and whether the level of complexity has any effect on these values. Full adders with less power consumption are important for digital chips these days. It is easy to design a full adder from

basic gates like NAND, NOR, and XOR. The proposed full adder achieves the most effective compared to other 10 existing full adders.

The full adder delay for the proposed full adder is very less compared to the worst case delay for existing Full Adders (FAs). With these figures, the proposed full adder is mostly suitable for pipelining designs with tight delay constraints. Furthermore, a simple design of hybrid full adder is presented that is useful in edge-level logic designs where bit insertion latency is important. The findings of comparing Power, Delay, and PDP are shown in Tables below.

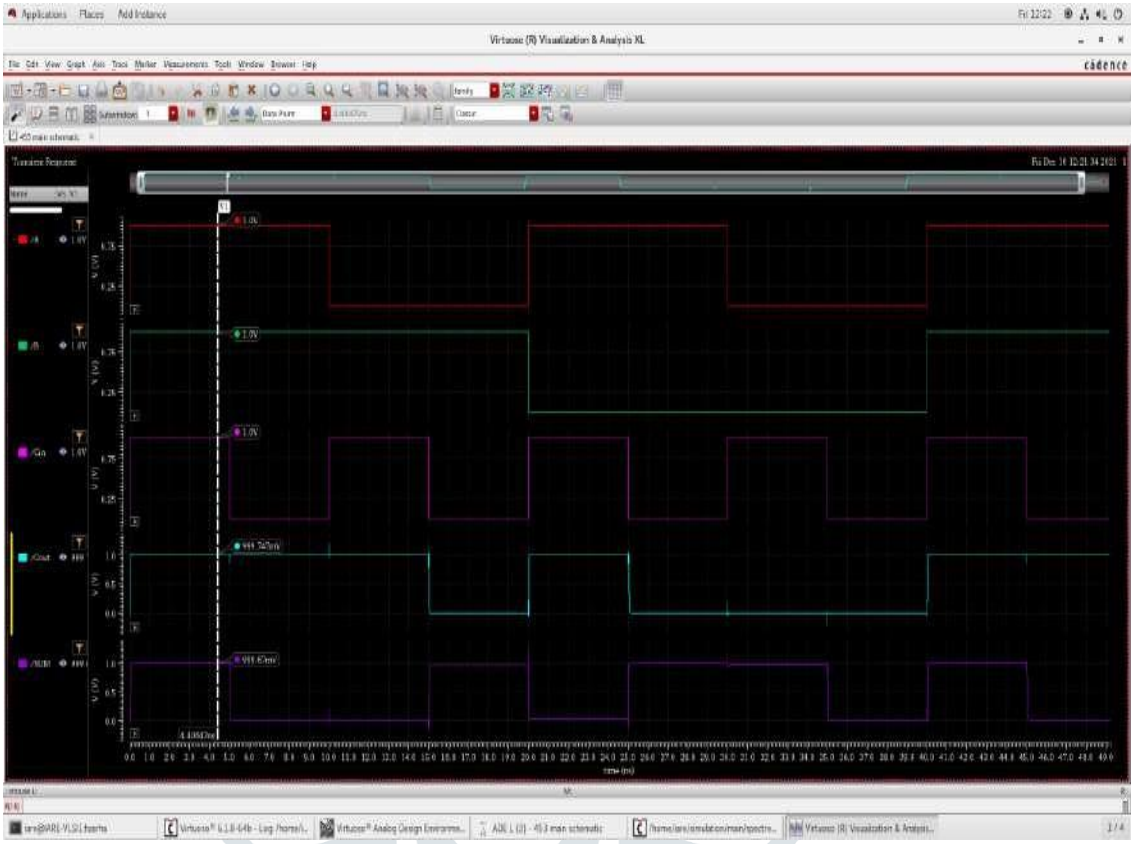

Figure 3 Transient response of the Proposed FA

Table 2: Observation of Average Power

Full Adder	**Number of bits**			
	04	08	16	32
C-CMOS	4.62	9.10	18.22	36.77
ULPFA	5.1	10.23	19.71	40.71
LPHS FA	3.38	7.12	NA	NA
Bhattacharyaa's	2.56	4.55	NA	NA
Mirzaee's	4.82	9.77	18.92	35.22
Parameshwara's	2.59	5.88	NA	NA

Shoba's Design 1	3.10	6.23	NA	NA
Shoba's Design 1	4.77	9.03	18.44	33.99
Shoba's Design 1	3.67	7.45	15.99	31.79
Sanapala's	2.93	6.09	NA	NA
Proposed Design	3.54	6.25	14.11	27.41

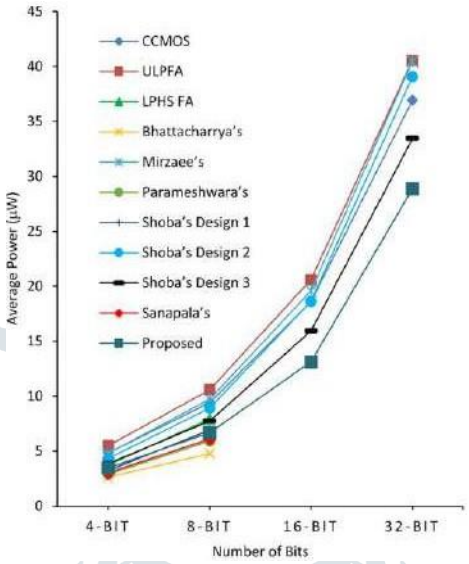

Figure 4 Average power of the FAs operating in cascade

Figure 4 shows the FAs after they have been expanded to 32 bits. When compared to other current FAs, the proposed FA has the lowest average power possible. Thus, it has a lower energy consumption and a high speed/low delay operation, the Full adder is used to calculate 32-bit addition results in one cycle of operations. The Full adder is a combinational logic block , which calculates addition of two n-bit binary numbers. The purpose of this part is to calculate the sum output by full adder is high or low, with a given carry input and a given set of inputs.

Table 3: Observation of Propagation delay

Full Adder	**Number of bits**			
	04	08	16	32
C-CMOS	0.21	0.49	1.109	2.25
ULPFA	0.32	0.62	1.619	2.41
LPHS FA	0.45	3.07	NA	NA
Bhattacharyaa's	0.78	3.21	NA	NA
Mirzaee's	0.22	0.52	1.118	2.21
Parameshwara's	0.25	1.49	NA	NA
Shoba's Design 1	0.29	1.32	NA	NA
Shoba's Design 1	0.15	0.37	0.76	1.3
Shoba's Design 1	0.20	0.42	0.91	1.7
Sanapala's	0.41	3.7	NA	NA
Proposed Design	0.14	0.33	0.701	1.41

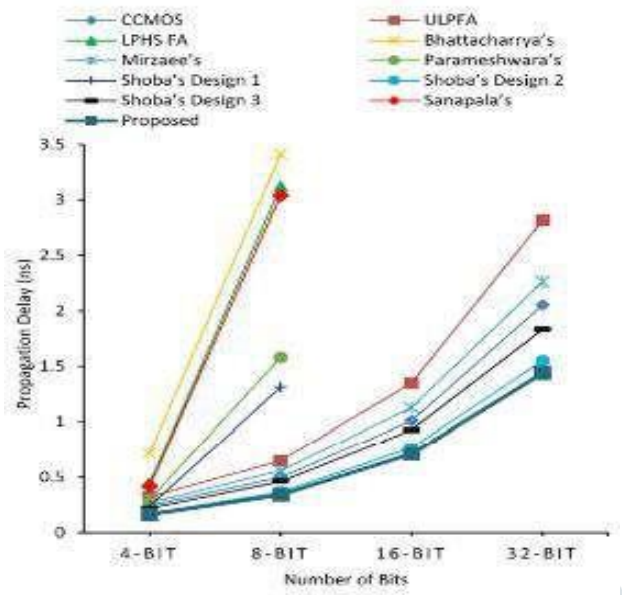

Figure 5 Propagation delay of the FAs operating in cascade.

Figure 5 shows the FAs after they have been expanded to 32 bits. When compared to other current FAs, the proposed FA has the lowest propagation delay possible. The proposed FA has the lowest power delay for two reasons. First, the use of a synchronous design allows power to be cut off sooner after an error if the current FA is not correct, thus saving energy consumption.

The second reason is that all cells perform the same function and are therefore easier to compute than FAs with a wider range of functions. In order to show the ease of computation, Figure 5 shows graphical representation of the proposed FA after extended to 32 bits with minimum propagation delay.

Hybrid Full Adder requires energy to drive the input and output signals. This energy is obtained from a power source and is generally distributed through the whole circuit. Hence from the observations obtained the proposed design has lowest power delay and consumes less power as possible. The proposed design uses the minimum number of components which are the silicon p-channel field effect transistors (p MOSFETs) and silicon n-channel field effect transistors (n MOSFETs). Source, drain, gate and substrate of the p MOSFETs are configured as a voltage source to supply a voltage drop at the output node. The configuration of gate, source and substrate of an n MOSFET is opposite to that of a p MOSFET. Hence the use of the Gate diffusion input technique has the approach to reduce the power consumption

Table 4 Observation of Power delay

Full Adder	**Number of bits**			
	04	08	16	32
C-CMOS	1.09	4.21	18.22	74.4
ULPFA	1.72	6.87	27.91	113.9
LPHS FA	1.79	24.72	NA	NA
Bhattacharyaa's	1.26	16.23	NA	NA
Mirzaee's	0.88	5.47	21.64	1.02

Parameshwara's	0.73	9.41	NA	NA
Shoba's Design 1	0.716	9.13	NA	NA
Shoba's Design 1	0.82	3.24	13.44	63.05
Shoba's Design 1	1.30	3.63	5.05	61.26
Sanapala's	1.4	18.12	NA	NA
Proposed Design	0.55	2.29	9.04	40.9

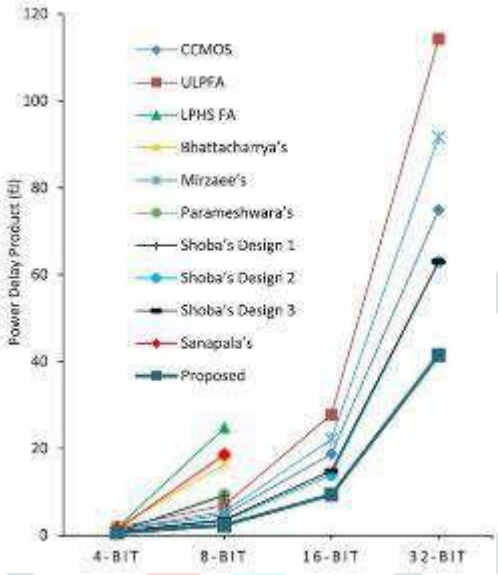

Figure 6:PDP ofthe FAs operating in cascade

CONCLUSION:

This function displays GDI FA Cells and Logic-based CCMOS with high performance restrictions. The proposed adder's design is differentiated to 10 different other designs in the Cadence simulation domain. FAs were also given to assess the appropriateness of a wide range of adders for all active computer systems. When compared to existing modern art designs, the suggested GDI-based GDI design performs exceptionally well and effectively as a single cell and in cascade mode. With the installation of CCMOS-based inverters, difficulties such as power outages, voltage deterioration, and limited driving capacity of GDI gates have been rectified. The suggested FA design offers a wide range of adders because to its great performance attributes and compatibility for usage in a wide range of adders. The proposed FA design is a great option for creating computer units for the most complex computer systems and every digital appliance.

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