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Modelling, Characterization and Optimization of a Delta-Sigma ADC for Audio Codec Applications

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Abstract: **In this work, single bit modulator and decimator filter for audio codec applications is described as a MATLAB® SIMULINK® model. Together with the different non-idealities and noise models related to the modulator, the delta-sigma ADC is constructed. For Audio Codec applications that demand great precision at the required input frequency, this kind of modulator is created. At an output data rate of 48 KS/s, the targeted SNR in this case is a minimum of 100 dB. A 4th order 1-bit CIFF Modulator structure is the Simulink® model that is being presented. The performance of ideal modulators can be impacted by a variety of non-idealities, such as practical GBW, switch noise, clock jitter, and finite DC gain; hence in this work, the non-idealities have been added for all stages and optimized them for achieving the 10dB Dynamic Range with practical conditions. In order to achieve the 10dB Dynamic Range under realistic circumstances, non-idealities have been included for all stages and optimized.**

Index Terms – ***Sigma-Delta Modulator (ΣΔ Modulator), GBW (Gain Bandwidth product), TF (Transfer Function), BW (Bandwidth), SR (Slew rate), SNR (Signal to Noise Ratio)***

I. INTRODUCTION

Today's businesses and academia prefer converters with high resolution and accuracy because they meet the demands of data converters and sensors. This paper discusses a discrete-time (DT) ΣΔ modulator, a CIFF single bit, as well as numerous non-idealities and noise. Model design with MATLAB® Simulink®. Due to its inherent linearity and meticulous analogue design, the ΣΔ Modulator is the ideal option for small- to medium-frequency high-resolution applications. [1]. Due to their circuitry's low power consumption, ΣΔ ADC-type data converters are appropriate for battery-operated devices. With balancing between the speed and accuracy, the ΣΔ Modulator can be used for the high-frequency applications at lower sensitivity without trimming the components' parameters. The ΣΔ Modulator loop can be implemented in four ways.

1. Low Order Single Loop Architecture
2. High Order Single Loop Architecture
3. Multiloop architecture
4. Multibit Architecture

We have shown the optimum set of parameter values to get a substantial-resolution with switched capacitor circuit at higher input frequencies. Good SNR can be achieved from the ideal simulation model parameter coefficient, but during the actual implementation of the model, various design factors were encountered that needed to be properly optimized, including switch noise, clock jitter, slew rate, GBW, and DC gain of the modulator. Because of the modulator's mixed-signal operating behavior, which is a non-linear circuit, the estimation of its performance presents a substantial challenge because the sole method for analyzing nonlinearity and performance deterioration caused by non-idealities is through behavioral simulation. In contrast to earlier works, which define discrete modulators [1], non-idealities [4], and decimators [5], our study offered the whole flow of behavioral design starting with modulators and decimators as well as non-idealities. The presented work is the designing and analysis of the fourth-order ΣΔ Modulator and Decimator. The order and topology of the ΣΔ modulator must first be determined in order to construct the ΣΔ modulator. These parameters include the required SNR and the maximum permitted OSR. This can analyse easily by the SNR approximation formula [1]or the MATLAB® tool provided by Richard Schreier [2].

TABLE I. ΣΔ MODULATOR SPECIFICATIONS

Parameter	Values
Full-Scale Input	2V
Topology of the Modulator	CIFF
Order of the Modulator (L)	4
Over Sampling Ratio (M)	128
Sampling Frequency (f_s)	6.144 MHz
Output Data Rate	48KHz
Signal to Noise ratio (SNR)	100 dB
Input Frequency	18.09KHz

The order of ΣΔ Modulator is L and M is OSR ($M=F_s/2B$). F_s denotes the sampling Frequency of the ΣΔ Modulator and 2B is denoting the NR of an input signal, an input signal having bandwidth B. The targeted SNR is greater than the 100dB. In Section II Modulator Design, Section III Decimator Design, and in section IV Simulation results are described.

II. ΣΔ MODULATOR DESIGN

The oversampling theory underlies how the ΣΔ modulator functions. The Modulator can be implemented in two different ways: either using the Sampled Data approach or in the continuous-time domain [4]. As a result of its usage of switched capacitor circuits, which are effectively achieved with the aid of current CMOS technology, the sample data-based procedure is the most often utilised technique. The fundamental benefit of employing a one-bit quantizer is that it is linear by nature, and it is also simple to construct. We concentrated on a one-bit quantizer method to prevent instability in this work. Lee's Rule must be taken into account. This suggests that the NTF's maximum amplitude should be smaller than 1.5 [3]. Dynamic range scaling can be utilised, in which the coefficient of the feed-forward path and the gain of the integrator can be altered [1], if it is necessary to scale the coefficient for changing the output of the Integrator to prevent the saturation of Op-amps used in the Integrator.

A. ΣΔ Modulator Topology

There are mainly four topologies are used for designing the ΣΔ Modulator. [3]

a. Cascaded Integrators feed-forward topology (CIFF)
b. Cascaded Integrators feedback topology (CIFB)
c. Cascaded Resonators feed-forward topology (CRFF)
d. Cascaded Resonators feedback topology (CRFB)

CIFB and CIFF are the two primary topologies utilized to realize cascaded integrators. While in CIFB the final output is driven to each integrator's input with the aid of DAC feedback, in CIFF the integrator output is immediately pushed into the 1-bit comparator through the feedforward path. The output of each integrator's swing in CIFF is low due to the signal's feedforward, and because of the low swing of the integrators, the requirements for voltage headroom and slew rate are relaxed. If the voltage swing is low, the power consumption is also reduced. In CIFF, the voltage swing is lower as a result of which the analogue designing complexity is lower. Only the STF is impacted by the various Modulator structures, while the NTF is constant across all structures. The output signal is fed into the integrator's input in a CIFB multiple. Multiple feedback in the CIFB architecture ensures excellent stability.

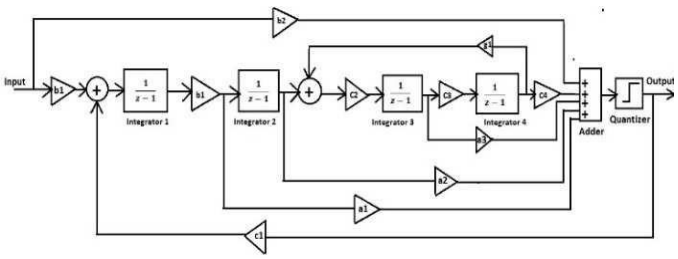

Fig. 1. Fourth Order CIFF Delta-Sigma Architecture

B. ΣΔ Modulator Coefficient Determination

The next step after determining the topology of a modulator is to discover its coefficients. Richard Schreier's MATLAB® tool can be used to get these coefficients [3]. Installing the Modulator exchange, which is available on the MATLAB Files [2] exchange, can be done in order to execute numerous basic simulations, such as NTF, STF realisation, and coefficient realisation. The coefficients are obtained by completing numerous simulations and analyses, but because mixed-signal circuits are nonlinear, the nonlinearity analysis is crucial for the precise estimation of various parameters.

TABLE II. FOURTH ORDER CIFF ΣΔ MODULATOR COEFFICIENT

Parameters	Value
a1	0.58058
a2	0.3082
a3	0.0644
a4	0.0060
b1, b5	1
b2, b3, b4	0
g	6.9627×10^{-5}

C. MSA Determination

It is essential to analyse the Maximum Sampling Amplitude (MSA) for the stable output of the Modulator before analysing the fourth-order ADC for the desired SNR value. When the input signal's amplitude is high, the total of the input signal and noise is a much larger value than the MSA, which causes the Quantizer to become saturated. A steadily changing ramp input signal is used to determine the MSA of the modulator.

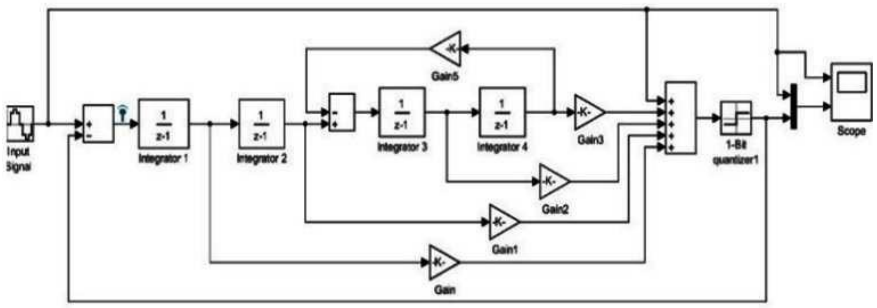

Fig.2. 4th Order ΣΔ Modulator Structure

The Maximum Sampling Amplitude can be calculated after analysing the MSA configuration of the Modulator's output pattern by multiplying the input slope by the modulator's saturation time.

D. SNR Analysis

Due to its low power consumption and suitability for usage with battery-operated devices, the single loop Modulator topology is preferred over the cascaded Modulator alternative [7]. The setup for the ideal 4th order Modulator is built using the above-obtained Modulator coefficients [Table 2]. The analysis in this study is conducted using a sinusoidal input signal.

III. DECIMATOR DESIGN

The oversampling theory underlies modulator operation. The noise is shaped and shifted upward in the frequency spectrum. In order to get the output data rate to Nyquist Rate, it must therefore reduce the frequency by a factor called OSR. By lowering the data rate, the digital filter's main task is to remove the modulator's output noise. Due to its straightforward design and minimal memory requirements, the CIC filter is the perfect option for this purpose. The Cascaded Integrator and Comb Filter is known as a CIC filter. Because of their symmetrical construction, CIC filters are easy to implement. Digital Integrators and Differentiators with TF are used in equal quantities to make CIC filters [8].

IV. SIMULATION RESULTS

A. MSA Determination

A slow input ramp signal with a high slope of 10 is used to determine the MSA. The output clearly shows that the Modulator becomes saturated with time. The MSA can quickly calculate the time until saturation by multiplying the slope of the input signal by the output analysis. The obtained MSA value in the work being given is 0.6 V, but the audio codec's modulator's maximum input amplitude is 1 V, thus a few coefficients have been changed to offset the MSA's impact on input amplitude.

B SNR Determination

The ideal SNR is produced after altering the 4th order single bit, discrete-time CIFF, modulator model in accordance with the discovered MSA. The output data rate is 48 KHz, which is the usual number for Audio Codec Applications, and the sinusoidal input signal has a frequency of 18.09375 KHz. The sampling frequency is 18.09KHz, and the OSR is 128. The Digital Decimation Filter is also interfaced in this configuration, as seen in fig. 3. SNR and other frequency domain parameters are

observed in this work using two spectrum analyzers at the outputs of the modulator and the decimator filters. Fig 4 displays several output spectrums and output plots based on observations of ideal modulator and decimator filters.

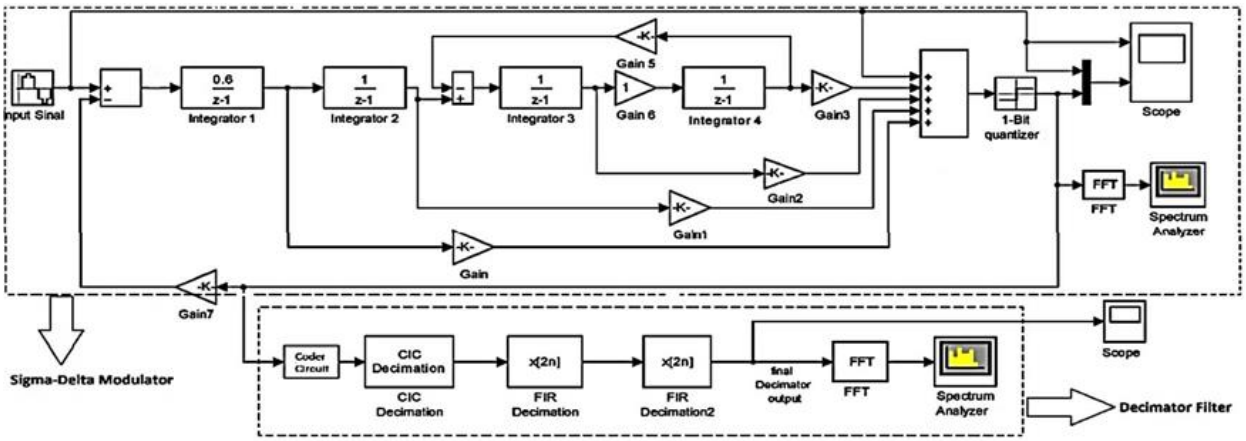

Fig.3. Ideal 4th Order CIFF ΣΔ Modulator and Decimator

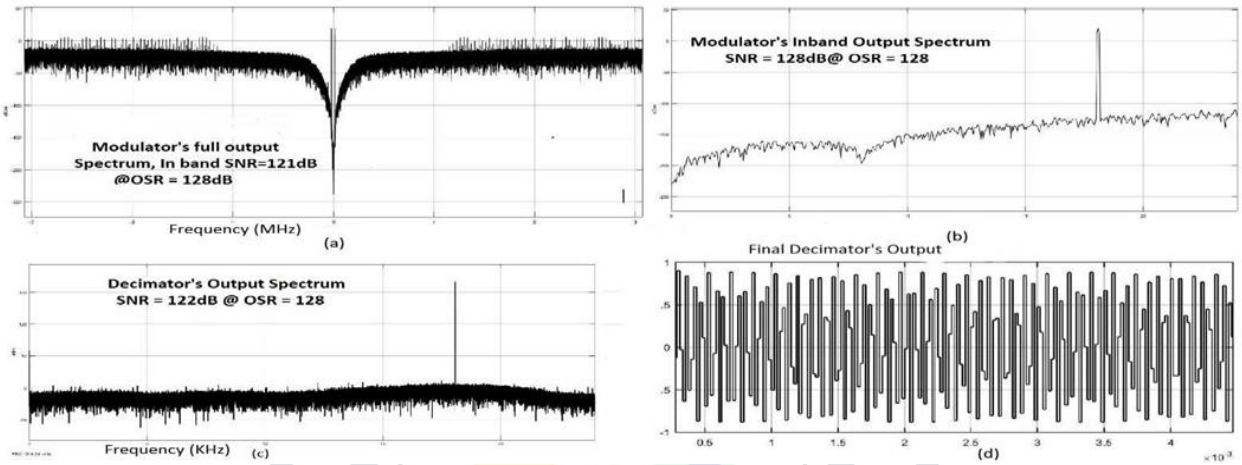

Fig.4. Output PSD of ideal ΣΔ Modulator, (a) Full Output Spectrum of ΣΔ Modulator, (b) In-band Output Spectrum of ΣΔ Modulator, (c) output spectrum Of Decimator, (d) Output of Decimator

TABLE III: SIMULATION RESULTS

Sr. No.	Parameter of ∑Δ Modulator	SNR
1	Sampling Jitter (r = 0.78ps)	115dB
2	Switch noise (Cs=2 pF)	115dB
3	Finite DC Gain ($H0 = 10^3$)	117dB
4	Finite GBW (TABLE 3)	105dB
5	Slew Rate (TABLE 3)	105dB

V. CONCLUSION

Here, a model for the Delta-Sigma ADC and nonidealities of the Modulator has been presented using MATLAB® SIMULINK®. Before implementing with actual circuit components in CADENCE-type software, it is possible to quickly analyse and visualise the circuit performance for various operating conditions in MATLAB® SIMULINK®. This allows for the appropriate designing of Modulator circuit. It is simple to configure the various design parameters, such as GBW, Slew rate, etc., thanks to the concept of Modulator non-idealities. When the various types of non-idealities and other factors are taken into account, the resultant SNR is 103-104dBc.

REFERENCES

[1] Simona Brigati, Fabrizio Francesconi, Piero Malcovati, Franco Maloberti, "A Fourth-Order Single-Bit Switched-Capacitor ΣΔ Modulator for Distributed Sensor Applications"2004
[2] R. Schreier. Sig Del. [Online]. Available:
http://www.mathworks.com/matlabcentral/fileexchange/index.jsp
[3] R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters. New York: Wiley-IEEE Press, 2004.
[4] Shashant Jaykar, Prachi Palsodkar, Pravin Dakhole, Shashant Jaykar, "Modeling of Sigma-Delta Modulator Non-Idealities in MATLAB/SIMULINK" July 2011.
[5] Khalid K. Mohammed, "Design and Implementation of Decimation Filter for 15-bit Sigma-Delta ADC Based on FBGA" April 2014.
[6] Anna S. Kuncheva, Thibault Mougel, Lukas Fujcik, Blagomir Donchev, Marin Hristov, "Design of a Decimation Filter for Novel Sigma- Delta Modulator" July 2006.
[7] Youngkil Choi, Jeongjin Roh, Hyungdong Roh, Hyunseok Nam, "A 99-dB DR Fourth-Order Delta–Sigma Modulator for 20-kHz Bandwidth Sensor Applications" Fab 2009.
[8] https://inst.eecs.berkeley.edu/~ee247/fa08/files07/lectures/L15_f08.pdf
[9] J. S. Wilson, Sensor Technology Handbook. New York: Elsevier, 2005