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Area Delay Analysis of CMOS Reversible Gate based Add-Sub Circuit for VLSI Application

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Abstract : Full Adder is the heart of any central processing unit that is a core component employed in all the processors. The approach to minimize power loss from digital devices made researchers to focus on reversible logic. This paper presents area delay analysis of CMOS reversible gate based add-sub circuit for VLSI application. This design is compared with existing designs on some selected performance parameters such as total number of reversible gates, garbage outputs and quantum cost. The proposed design for 8-bit adder-subtractor circuit using reversible approach simulated using Modelsim tool and synthesised for Xilinx ISE 14.7.

IndexTerms **–** Adder, Xilinx, Reversible Realization, Delay, components, Gates**.**

I. INTRODUCTION

The reversible logic operations can't erase information and dissipate zero heat. The circuit actually operates in a backward operation, allows reproducing the inputs from the outputs and consumes zero power. As the basic elements of any logic circuit, logic gates are used to realize Boolean functions. A Reversible Logic Gate should produce one-to-one map-ping between Inputs and Outputs, so that reversibility is maintained. That is Reversible Gate is Injective between Inputs and Outputs. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Additional inputs or outputs can be added so as to make the number of inputs and outputs equal whenever necessary. This also refers to the number of outputs which are not used in the synthesis of a given function. In certain cases these become mandatory to achieve reversibility. Inputs + Constant Inputs = Outputs + garbage figure 1 shows a n-input and n-output Reversible Logic Gate and is called as n*n Reversible logic gate, where n^{th} input of logic gate is given by In and n^{th} output is given by On.

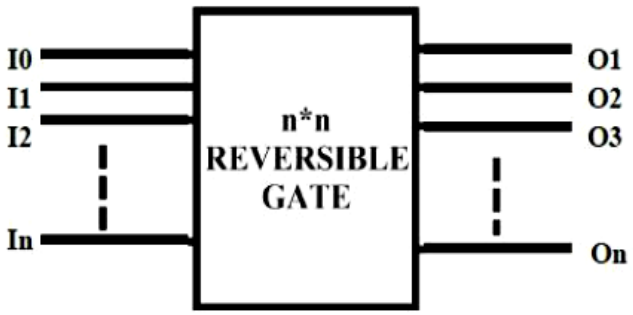

Figure 1: n*n Reversible Logic Gate

There exist many reversible gates in the literature. Among them 2*2 Feynman gate (shown in Fig. 2), 3*3 Feynman Double Gate is the most preferred. The Feynman Gate shown consists of two inputs A and B, two outputs P(= A) and Q(= A B).

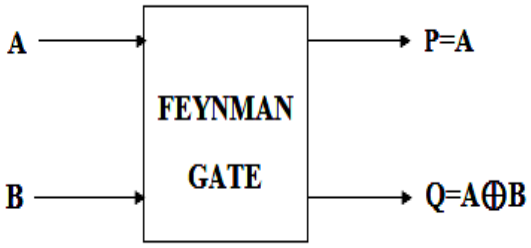

Figure 2: Feynman Gate

The simplest Reversible gate is NOT gate and is a 1*1 gate. Controlled NOT (CNOT) gate is an example for a 2*2 gate.

II. PROPOSED METHODOLOGY

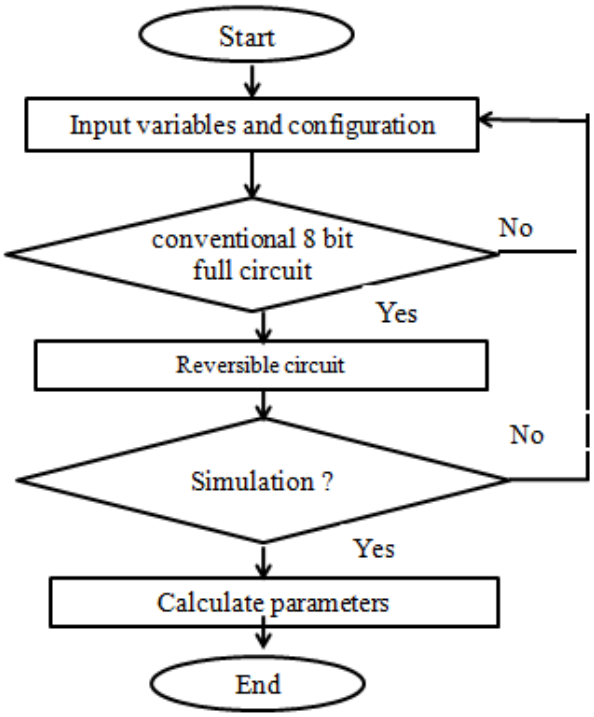

Figure 3: Flow Chart

The 8-bit adder/subtractor computes the sum or difference of two 8-bit numbers, A and B. This uses our 8-bit carry look ahead adder with 2's complement or and multiplexer to implement subtraction. If the enable bit is set low, then the mux lets through input B and the result is A+B. If the enable bit is set to high, then the mux lets through the output of the complement or, so the adder adds A and the 2's complement of B, which is equivalent to A-B.

When performing addition 10100010 + 11100011 (enable set low) the worst case delay on the MUX for the schematic is 0.02975 ns. Add this to the delay needed for the clock of the 8-Bit adder to get a total clock delay of 0.02975ns + 0.110126 ns = 0.139876 ns. So the earliest the schematic clock can switch for addition is 0.14 ns after the inputs are set.

For layout this delay was 0.12012 ns. Add this to the delay from the 8-bit adder to get a total clock delay of 0.12012 ns + 0.259166 ns = 0.379286 ns. So the earliest the extracted clock can switch for addition is 0.38 ns after the inputs are set.

When performing subtraction 10100010 – 00000001 (enable set high) the worst case delay for the complementor for the schematic is 0.74565 ns. The worst case delay for the mux for the schematic is 0.05439 ns. So together they create a total delay of 0.80004 ns. Adding this to the delay of the adder gives a total clock delay of 0.910166 ns. So the earliest the schematic clock can switch for subtraction is 0.92 ns.

Reversible full adder gate namely Peres Full Adder Gate (PFAG), the gate is achieved by cascading two 3*3 Peres gate. The quantum realization cost of this gate is 8 since it includes two 3*3 Peres gates. The gate can work singly as a reversible full adder circuit when its fourth input is set to zero (D=0). This gate requires only one clock cycle and produces no extra garbage outputs.

Feynman gate (FG) also called Controlled-NOT (CNOT) gate, is two input–output reversible gates, with QC equals 1. The relationship between the inputs and outputs are related to and Q = A x B When A = 0 then Q = B, when A = 1 then Q = B'. The Feynman Gate can be used as a fan-out/copying gate or an XOR gate.

III. RESULT AND ANALYSIS

The implementation and simulation of the proposed algorithm is done over Xilinx 14. The behavioral modeling style and Isim simulator is adopted for simulation. RTL and synthesis results are also generated.

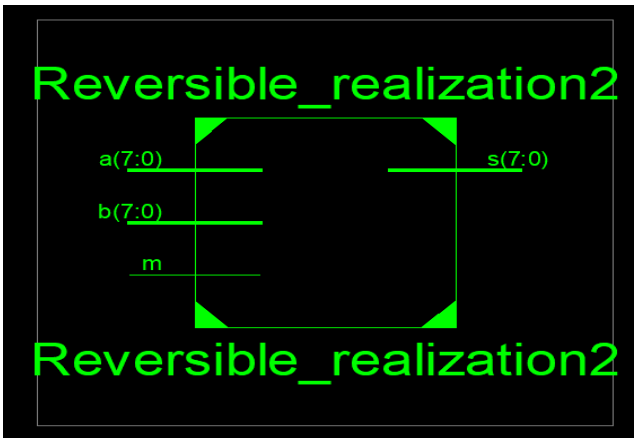

Figure 4: Proposed Top module

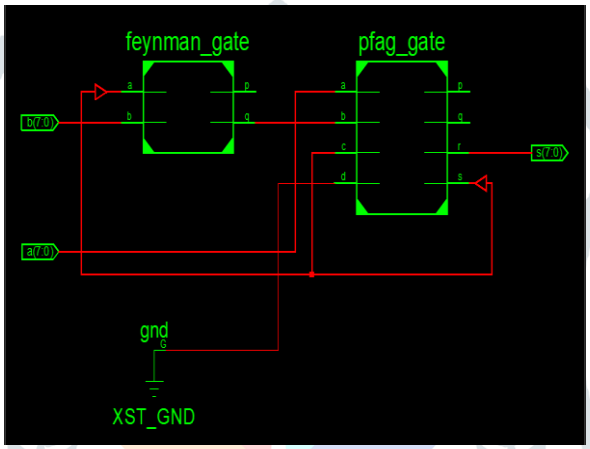

Figure 5: Proposed Reversible circuit using Feynman and Pfag Gate

In figure 5, showing reversible circuit using Feynman and pfag gate in which, Only PFAG has been realized in NMR nanotechnology. The quantum cost of PFAG is 10, It has also been observed that PFAG is better than TSG, MKG and HNG in terms of hardware complexity. It includes 4 PFAG and requires 4 constant inputs. The quantum realization cost of the proposed implementation is 32 and the design produces 10 garbage outputs.

Figure 6: Result in test bench Conventional 8 bit full adder/Subtractor

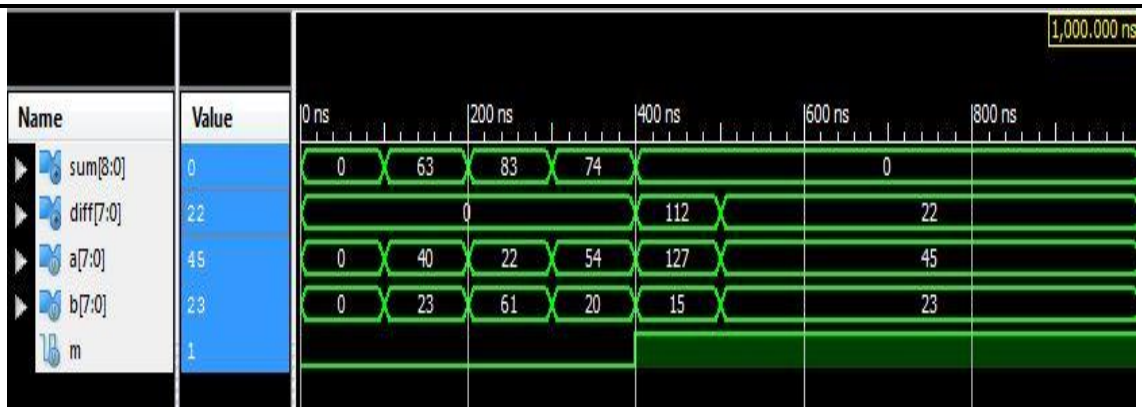

Figure 7: Result in test bench reversible 8 bit full adder/Subtractor

Table 1: Result Comparison-1

Sr no.	Parameter	Previous work [1]	Proposed work
1	Delay	5 ns	2.526ns

Table 2: Result Comparison-2

Sr no.	Parameter	Previous work [5]	Proposed work
1	Number of Gates	16	8
2	Garbage Output	17	10
3	Quantum Cost	72	46

The optimization is achieved on some selected factors such as number of gates, garbage outputs and quantum cost as compared to the existing designs. This proposed adder-subtractor circuit is designed using only 8 gates, generates 10 garbage outputs and total quantum cost of the circuit is equal to 46. This adder-subtractor circuit may be utilized in various computational devices for designing low power loss electronic systems.

IV. CONCLUSION

The final entity was then tested by choosing cases which would show what the 8-bit adder/subtractor can successfully add/subtract, and for what values it produces results which are not meaningful. These limitations imposed by the design were outlined. By comparing the output timing diagrams in ModelSim against an arithmetically constructed truth table, finally it is verified the accuracy of our verilog code in correctly representing the 8-bit adder/subtractor network.

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