JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

Performance Analysis of 7T SRAM Cell IOT-based devices using Anti Body Bias Technique

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Abstract: Static Random-Access Memory (SRAM) with ultra-low power consumption is required in Internet of Things (IoT) devices to ensure long battery life. The current work employs the Cadence Virtuoso tool for the execution of 7T SRAM cell methods, & all considered methodologies' read & write operations have been carefully monitored. The goal of this work is to decrease 7T SRAM cell power while maintaining industry-leading performance. Microprocessors, Cache memories, & portable devices are just a few examples of the many applications where SRAM is crucial. Leakage power is the main issue with SRAM cells when it comes to low-power applications as the node of the technology is scaling down. Consequently, low power appropriate memory design is required. The key to using the anti-body bias approach to a 7T SRAM cell is to lower the bulk voltage, low power, & leakage current. This reduces process variation. We look into anti-body biassing as a means of controlling the bulk voltages of transistors, and we demonstrate that it works especially well in sub-threshold circuits and can completely remove performance differences and weak power.

Key Words: SRAM, CMOS, Cadence, 7T SRAM Cell, Leakage Power.

I. INTRODUCTION

Sensor nodes, remote sensing, and other IoT-based devices have experienced tremendous expansion. SRAM, which takes up a significant amount of system-on-chip space, is used in these devices to store information. SRAM dominates a significant portion of the system's energy, becoming the primary source of power dissipation. Low-power SRAM cell design is a major challenge for these applications, which require long battery life. Semiconductor SRAMs are widely utilised in modern equipment that is based entirely on computers, systems on chips (SoCs), & microprocessors. Memory is made up of 70 to 80% of the processors' available locations, which means it takes up a lot of space in the system. That is to say; it will utilise more electricity and waste more electricity due to leakage [2,3]. SRAM and DRAM both store information; however, their operational approaches vary. SRAM doesn't have this issue; however, DRAM expects the information to be refreshed or kept after a specific amount of time. SRAM no longer needs to be refreshed repeatedly. Because SRAM is inherently unpredictable, it cannot store information in terms of zeros and ones when the supply is totally shut off. Additional networks are needed to continuously update the DRAM, which makes it stable and bulky [4,5]. A more significant issue with DRAM is that memory consumes more electricity than SRAM does. Therefore, DRAM is less recommended as compared to SRAM. Due to its high speed and ease of usage, SRAM is widely employed in SoCs for the reasons mentioned above. There are numerous types of SRAMs available on the market, including conventional 6T to 9T SRAM cells. Caches that are based on SRAM cells are well known in the industry. The IoT includes sensors, wireless technology, microcontrollers, and SRAM. Because IoT devices are lightweight & portable, battery life is a key consideration; thus, we must concentrate on low-power usage SRAM cells [6,7].

II. 7T SRAM Cell

Memory cells are primarily categorised for CMOS memory applications by (1) Number of elementary devices, (2) Data types, (3) Featured operating modes, (4) Logic system, (5) Radiation hardness, (6) Access mode, (7) Storage media, (8) Storage mode, and (9) Storage operation, In this study, memory cells are used in arrays, and all other memory circuits fulfill the purposes of memory cell arrays.

Write operation and read operation. Instead of having to independently store relevant information in different named memory regions, this study suggests the deployment of 7T SRAM, which is superior in terms of Q. Each element that is added to an array is automatically saved in a memory location nearby. Even during the standby cycle, more power will be used because the memory's leakage current grows with capacity. Many schemes are used to reduce power; here, we try to save power to write and by power dissipation. 2nd transistor M7 serves as feedback for the 2nd inverter, causing the

1st inverter's value to rise disproportionately. The transistor NM4 is switched off at the start of the writing process and remains so during the whole write operation. The read cycle can be improved by analysing the NM3 and NM4 transistors [1, 2].

The average power consumption decreases as a result of this impact's reduction in the dissipation of dynamic and static power [6,8,9]. Figure 5 displays a new approach diagram for 7T SRAM cells (see below). New 7T SRAM cell methodology for 90 nm technology has been introduced using Cadence Virtuoso. While the new 7T SRAM cell has improved read speed and power efficiency, it has sacrificed very little write stability in the name of improved read performance. 8-bit cells are used to store 8 bits at a time and produce one output at a time. Here 7T is used to store single bit. Before & after each read/write operation, BL and BLB are both highly recharged. Write operation is done when center NMOS is OFF, but here this NMOS is getting DT and ON, so it reads at the same time and initially, it generates garbage value. By asserting Word line DT high, BLB receives the complement of the data that will be written to node Q, as well as the corresponding NMOS, turned on. The write operation is not engaged by BL or its access transistor. Both access transistors are turned off during standby mode by using a negative DT pulse. At the next positive pulse of DT as center, NMOS is ON and reads previously stored data.

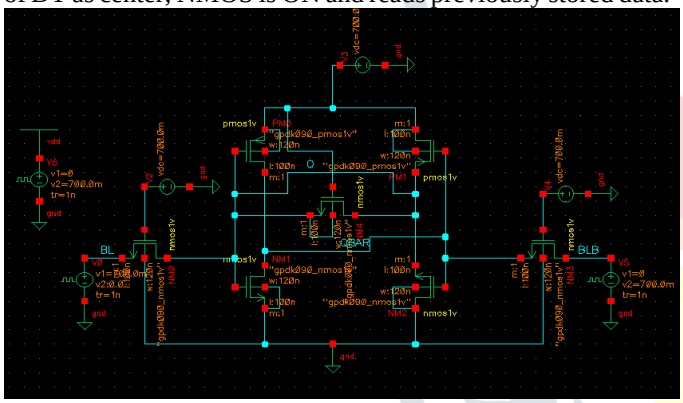

Figure.2 7T SRAM Cell schematic

During reading operation, sense amplifier receives BLB & BL & read data when word line DT is off. 3-to-8 Decoder is used to select to write one of all cells. In 8x8 bit, array Read operations are back and forth between 8x8 bit cells. Both sense amplifiers 1 and 2 produce the data of ST1 and ST2, respectively, at different pulse times.

III. Sense Amplifier

Key components in determining the functionality and environmental tolerance of CMOS memories are sense amplifiers and memory cells. To increase a memory's speed performance and to deliver signals that meet the specifications for operating peripheral circuits inside the memory, we built a sense amplifier [4].

Sense amplifiers must function in a circuit's environment. The easiest place to gather the basic requirements for sense amplifier & sense circuit operations is the operation margins of potential sense circuits. Figure 3 shows the Sense Amplifier Circuit; during reading operation sense amplifier receives BLB & BL and reads the data when word line DT is off. 3-to-8 Decoder is used to select to write one of all cells. In 8x8 bit, array Read operations are back and forth between 8x8 bit cells. Both sense amplifiers 1 and 2 produce the data of SA1 and SA2, respectively, at different pulse times.

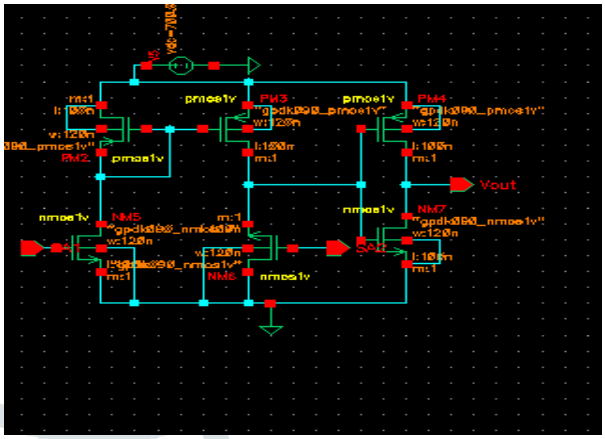

Figure.3 Sense Amplifier

IV. Simulation Results and Discussion

7T SRAM with a nominal supply voltage of Vdd = 0.7 V and 90nm technology, cell simulation has been performed on a cadence tool. At 27 °C, gate leakage is the only predominant mechanism. Read and Write Cell Data.

Writing Data into the Cell

To make sure the write circuitry functions properly, several 1 and 0 sequences were written into the memory array. A "1" & "0" were written into the memory cell, and the resulting waveforms are shown in Figure 7. Q rises to Vdd whereas Q drops to Gnd as soon as the write signal is asserted, as well as the word line is pulled high, as can be seen, while data "1" is writing. After a user requests a write, the amount of time it takes for the memory to actually perform the write is known as write access time (WAT). This was calculated from simulations to be 21.1ns, as illustrated in Figure 7.

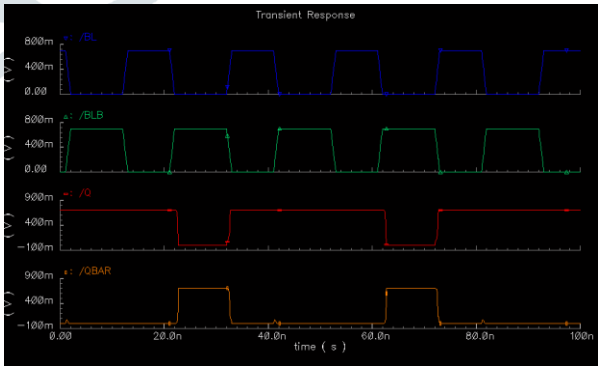

Figure.7 Write waveform of 7T SRAM Cell

Reading Data from the Cell

The replica bit line circuit must enable the sense amplifier circuits in order for them to read out information kept in the memory array. There is danger that data will be lost while being read. The waveforms derived from the simulations are shown in Figure 8. The voltage at nodes SA1 & SA2 rises up to 700mV & produces output Vout, as can be seen, while reading

data with logic '0' or '1' from the memory array. However, this is insufficient to flip the information in the memory cell in Figure 8.

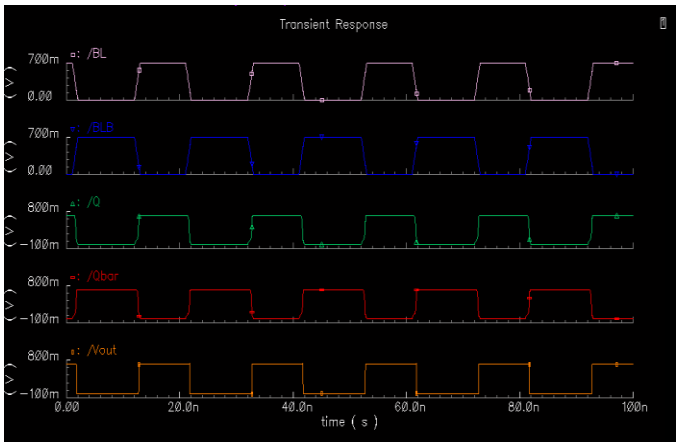

Figure.8 Read waveform of 7T SRAM Cell

V. Proposed Anti Body Bias Technique applied on CMOS 7T SRAM Cell

7T SRAM Based on CMOS is displayed in figure 2. When we applied Body bias technique on CMOS Based 7T SRAM Cell, then two additional inverters were connected in 7T SRAM Cell based on CMOS which is shown in figure 9. While using more area, this method for CMOS-based SRAM cells still functions at lower supply voltages. Consequently, it reduces utilisation of power.

On CMOS-based 7T SRAM Cells, the body-biasing technique is employed to reduce the effect of process variation. To control the bulk voltages of 7T SRAM Cell, 2 inverters are added to the basic SRAM cell. Value of bulk voltage is dependent on the value provided on SRAM cell. Output Waveform of CMOS Based 7T SRAM Cell with Body Bias Technique is displayed in figure 10.

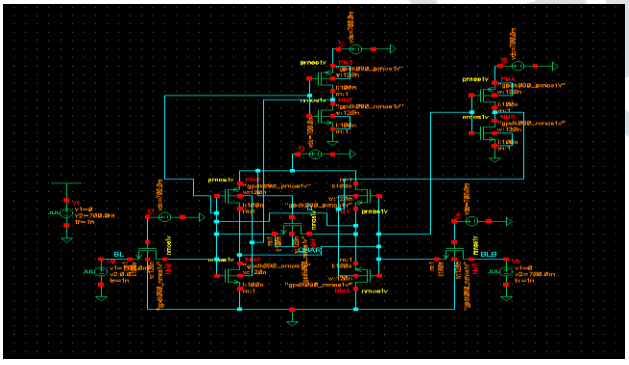

Figure.9 Schematic of 7T SRAM Cell using Anti body bias technique

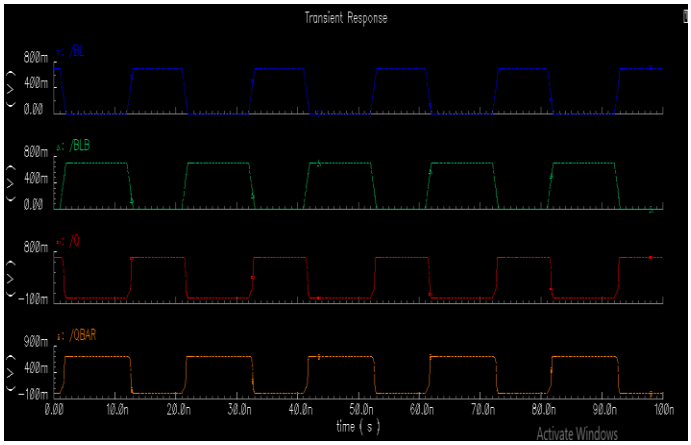

Figure.10 Output waveform of 7T SRAM Cell using Anti body bias technique

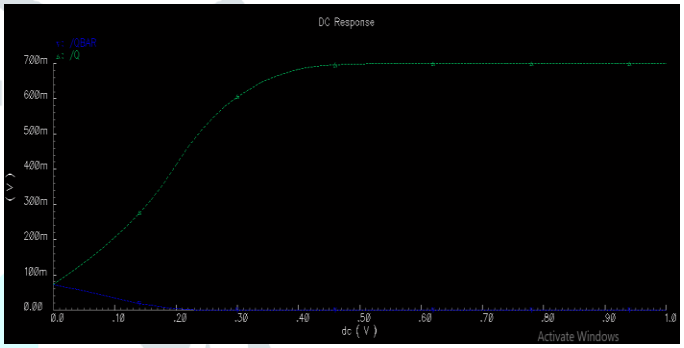

Figure.11 DC response of 7T SRAM Cell using Anti body bias technique

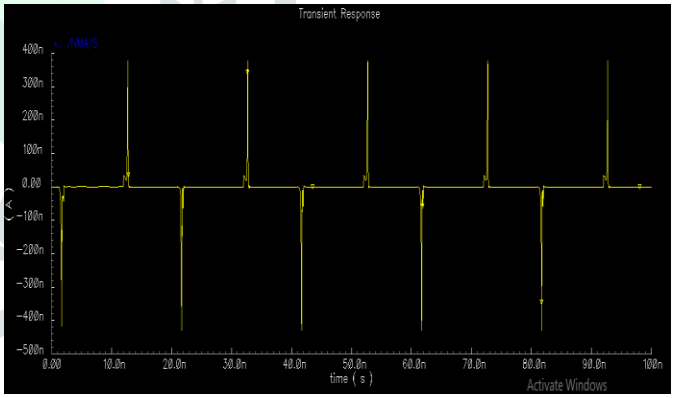

Figure.12 7T SRAM Cell Leakage Current Utilising Anti-Body Bias Technique

Table 1 below displays the 7T SRAM Cell Results Summary.

Table 1 Simulated Result Summary

S.no	Performance Parameter	CMOS 7T SRAM Cell	CMOS 7T SRAM Cell using Anti body bias technique
1.	Supply Voltage	0.7V	0.7
2.	Leakage Power	8.2nW	6.1nW

3.	Leakage current	6.3nA	4.4nA
5.	Read Access time	22.1ns	18.2ns
6.	Write Access time	18.5ns	16.4ns

Conclusion

In our investigation, the CMOS Based 7T SRAM have taken for comparison with the help of 90nm technology. In the realisation of a pass transistor multiplexer, the benefit of having the same functionality with a small number of transistors will be helpful. Thus, CMOS Based 7T SRAM using Anti body bias technique is suitable for implementation, which is characterized by high speed with minimum leakage current, low power compared with 7T SRAM. The purpose of applying the anti-body bias approach to the 7T SRAM is to lower the bulk voltage, low power, and leakage current. We investigate the application of anti-body biassing to manage bulk transistor voltages and demonstrate that it is particularly useful in low-power sub-threshold circuits for eradicating performance fluctuations. Comparisons are made between the amounts of power used for leakage, read & write access times, and & used leakage power.

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