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DESIGN AND OPTIMIZATION PROBABILITY-DRIVEN MULTI BIT FLIP-FLOP WITH CLOCK GATING TECHNIQUES

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Abstract
These two small design approaches, data-driven clocking and multi-bit flip-flops, use a common clock controller to drive several FFs at the same time. Separately, these are usually applied by VLSI designers. MBFF utilization in RTL, gate-level, and their arrangement have been the focus of previous studies. There were tensions and contradictions between different aspects of a project that were all studied together as a whole. Internal circuit diagram, its multiplicity and synergy with FF data flashing chances have not been examined thus far. This paper proposes a DDCG and MBFF combination algorithm based on the data-to-clock toggling ratio of Flip-Flops (FFs) in order to maximize energy savings. According to the results, the MBFFs should be arranged in order of increasing of activity to save the most electricity possible. It is possible to reduce the amount of power consumed by a device by employing a power-saving model that makes use of MBFF algebraic expressions and FF toggling probabilities. By using the Xilinx ISE tool, we were able to save between 17% and 23% of power in comparison to design with conventional Flip-Flops, which was around 39%.

Key words: Flip-Flops, MBFF,2-bit MBFF, k –MBFF, pCQ t.

1. Introduction

Multi-Bit Flip-Flops (MBFFs) have lately been highlighted as a design concept that can significantly reduce the power consumption of digital devices. Flip-Flops (FFs) are commonly used in digital systems to store data, and each FF has its own body clock driver. A coalesced master and slave latch, powered by clocks CLK and CLK, is shown in Fig. 1 in a 1-bit FF that is edge-triggered. The majority of the FF's energy is spent by its circadian rhythm drivers, which are important contributors to the overall power consumption. Flip-flops (FFs) are utilized to store data in digital systems, each with its own body clock driver. A multibit FF (MBFF) is a module that stores the clock drivers for all the underneath FFs in an effort to decrease the clock power. A k-MBFF is used to denote the combination of kFFs it in to an MBFF. A preliminary investigation Digital Signal Processors (DSP) was used in the past to regulate SMPS digitally (DSP). The control system algorithm, housekeeping, supervisory tasks, and communicating were all attempted to be performed using DSPs. Due to its many shortcomings and restrictions, this method is appropriate for most industrial applications. Control

bandwidth is constrained by the use of a single arithmetic unit that restricts computation speed; excessive delays in a multi-converter scenario; a lack of ability to generate non-sequential pulses as might be required in non linear control; limited functionality to achieve high magnification output driving signals; and other shortcomings.

In Fig. 1, two 1-bit FFs are grouped into a 2-bit MBFF, which is also known as a dual-bit FF. Clustered of Lol in 4-bit and floating point MBFFs is also feasible in the same way. After that, k -MBFF is used to represent a k-bit MBFF. MBFF does more than only reduce clock tree-driven gate capacitance. Because only one clock wire is needed for numerous FFs, the capacitive load on the wiring is minimized as well.. The clock tree's depth, buffer size, and number of subtrees are all reduced as a result. These characteristics not only save on clock power, but they also take up less semiconductor space.

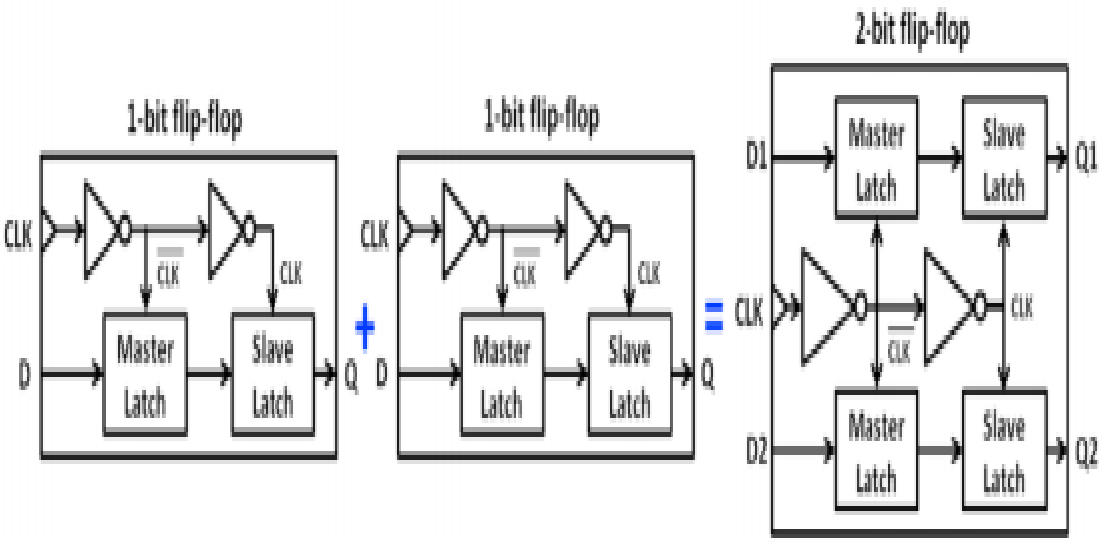


Fig 1. 1-bit FF and 2-MBFF.

Front-end design issues for MBFF multiplication and grouping have received scant attention. MBFF breaking should be based on logic, structure, and activity factors.

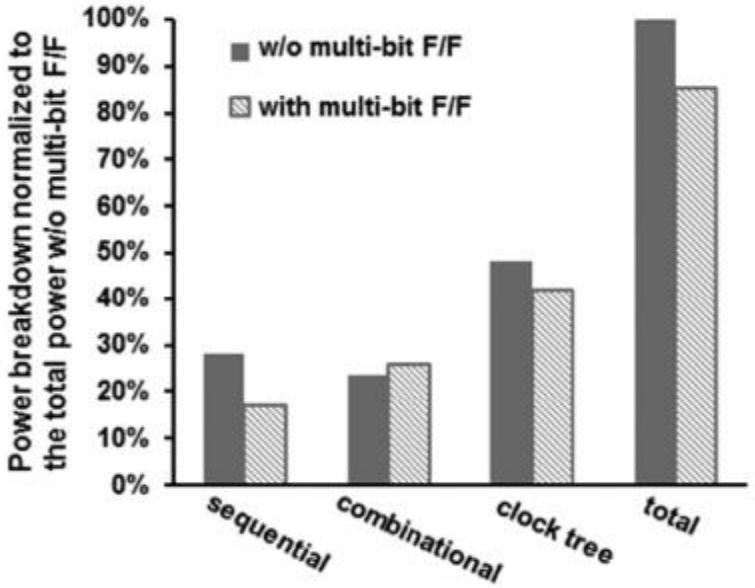


Fig 2: Power breakdown of MBFF compared to ordinary 1-bit FFs.

In a report, 92% of said FFs were bunched into MBFFs, the significant proportion of these were 4-MBFFs, whereas the reset were 2-MBFFs.. Fig. 2 illustrates the energy break - down of MBFF comparison to the 1-bit FF design. The power consumption is compared to that of a 1-bit FFs core (memories and IOs excluded). The air mass flow power has been reduced by 15%. Because the number of timer's drivers and wire load attached to the Manchester internal drivers was reduced, sequential logic and clock tree power decreased as expected. In

order to compensate for the increase in pCQt, some circuitry has been re-engineered. We propose introducing MBFF now at RTL design level to prevent the timing degradation caused by an increase in pCQ t. preventing timing issues will be easier if the embedded scripting and layout design stages are aware of pCQ t. A logic synthesis design involving the MBFF was presented, Here's a breakdown of the power savings, as shown in Table 1. A dynamic power decrease of 13% has been demonstrated. This is not a surprise, given that power reductions were achieved at the expense of timing loss, which was remedied by inserting low wattage threshold (LVT) cell on essential links.

		Single bit	Multi bit	Difference [%]
Number of FFs	1-bit	29437	5267	
	2-bit	0	1860	
	4-bit	0	5216	
Total FF area [u^2]		394047	402955	+2.26
FF's threshold type [%]	Standard	11.5	49	
	High	88.5	51	
Clock buffers in tree		934	624	-33.4
Skew [pSec]		249	176	-29.4
Seq. CKT power [mW]	dynamic	145	104	-28.16
	leakage	4.55	9.89	+117
Combinational power [mW]	dynamic	134	117	-12.4
	leakage	28.9	28.8	-0.35
Clock Tree (sinks incl.) [mW]		195	134	-31.4
Total dynamic power [mW]		446	388	-13.0
Total chip power		682	629	-7.77

Table 1. Power reduction obtained by MBFF design

2. Literature survey

[2.1] Digital Systems Power Management for High Performance Mixed Signal Platforms

High-performance mixed-signal (HPMS) platforms have stringent control of various and module performance requirements.. Designing reduced power systems is widely used in a variety of technologies such as mobile devices and identification systems. Microcontrollers also benefit from this capability. There are several problems and opportunities in industrial research environments when it comes to designing low-power devices. The study provides a variety of low-power solutions, ranging from power-performance optimization scenarios for active and standby modes to the construction of multi-core architectures that can operate at low voltages.

[2.2] The Optimal Fan-Out of Clock Network for Power Minimization by Adaptive Gating

VLSI chip designers are increasingly using clock signal gating to reduce switching power consumption. Probabilistic models of the clock-gating network allow us to estimate projected power savings and overheads, which are outlined in this study, The ideal gater fan-out for a gated clock tree is computed based on flip-flop toggling probabilities and process technology factors. The overall clock tree switching power is reduced by 10% as a result of the developed clock gating technology. When the planned gating scheme takes effect, it is discussed. The idea of combining FFs for a single clocked gating is also brought up. The study and results are in line with the experimental data acquired for a 65-nanometer 3-D graphics processor and a 16-bit microcontroller.

3. Concept of clock gating flip-flops

In fact, flip flops are logic gates in disguise. Memory can be created with the use of Boolean logic. RAM can be thought of as having its roots in flip-flops. If the gates are properly built, they will remember and execute a certain input value. A higher applicability of flip flops is helpful in building better electronic circuits Flip flops are most typically utilized in the design of a control circuit. To create a memory, flip flops can indeed be employed because they are based on the feedback notion.

3.1Multi-bit flip-flops

Because they contain a sharing inverter inside the flip-flop, multi-bit flip-flops are able to reduce their power usage. At the same time, the skew in the clock is minimized. The clock condition for both single- and multi-bit flip-flops is the same. The set and reset conditions are the same as well. Fig. 1 shows a multi-bit flip-flop example. In order to create a 2-bit flip-flop, you must first merge a single 1-bit flip-flop. The clock buffer is shared, resulting in a reduction in power consumption.

3.2 Algorithms

The algorithm is broken down into three steps: First, the merged flip-flops are identified. The combinational table can be constructed in the second phase using the overlapping region from the first. The combinational table can be constructed in binary tree form for ease of representation. The combinational table is used to merge flip flops in the third stage.

3.3 combinational table.

The combinational table is what we use to make the procedure as efficient as possible. A combination table is necessary for effective merging of flip-flops because mergeable flip-flops are not in intersection values. The initialization value of the library is used to create a combinational table. Flip-flops can be constructed using the values in the library. The combinational table is referred to as T, while the library's initializations are referred to as L. The bit width b (ni) and the one combinational ni are used to identify the initializations in T. Because we are merging the number of one-bit flip-flops, the minimum size is 1 bit and the minimal library size is initialised by library. As depicted in Figure 3.1, this cell is capable of holding two bits. In addition to the two data inputs and 2 data output pins, the device has one clock pin and one reset pin. Dual-bit flipflops use less power than single-bit flipflops and have essentially no additional costs. The truth table of a dual-bit flip-flop cell is shown in Figure 3. Clock values Q1 and Q2 pass to D1 and D2 when Clock is high, or Q1 and Q2 remain the same.

3.4 Identification of merge able flipflop

Flip-flops utilised in merging are identified using the digital circuits' flip-flops. Each pair of flip flops has its own unique timepiece for identifying purposes.

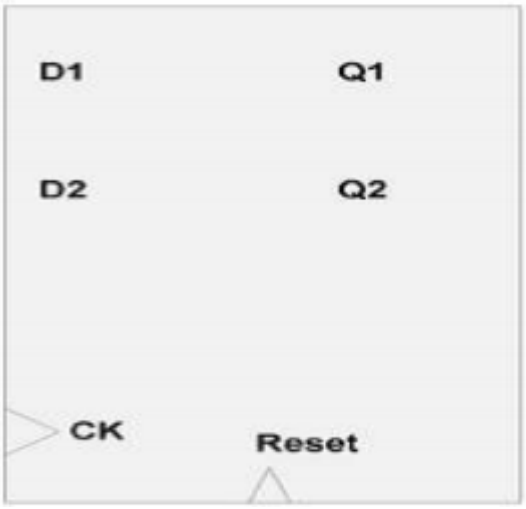


Figure 3: A dual-bit flip-flop cell

Table2: The true table of dual-bit flip-flop cell

CK	D1	Q1	D2	Q2
↑	L	L	L	L
↑	L	L	H	H
↑	H	H	L	L
↑	H	H	H	H
↓	X	D1	X	D2

4. Proposed system

It is possible to reduce the overall number of inverters by using multi-bit Flip-Flops. Using data-driven clock gating, unnecessary clock pulses can be reduced. Further power savings can be achieved by combining a multi-bit flip-flop with data-driven clock gating. This proposed system is implemented using the Xilinx software tool. In this study, we examine data-driven clock gating at the circuit levels, that is the most aggressive. To prevent the clock signal from interfering with the FF's state, the FF's gate is disabled (gated). Overheads in terms of space and power are being incurred as a result of data-driven gating. When many FFs are brought together, a single clock signal can be created by bringing their respective enabling signals together. The debilitating effectiveness may, however, be reduced. As a result, it is advantageous to group FFs that flip frequently in order to derive a common enabling signal. According to a recent research, data-driven gating is dependent on the switching activity of the individual FFs that make up a network.Power reduction became one of the more important design goals for system on chips (SOCs), as transistor integration increases the power budgets available. Increases in system costs and decreased product lifespan and dependability are both impacted by a SOC's high power dissipation. Many design techniques, such as the introduction of multi-supply-voltage (MSV) designs and the replacement of quasi cells with their high-voltage (Vt) counterparts, have been introduced to optimise energy usage in electrical and physical design. An ARM 1136JF-S processor IC in 90-nm standard CMOS is given with a physical and electrical mains power optimization method and design techniques. A multi-VDD domain design with different supply voltages can benefit from design technology and technique advances such as a single-pass RTL synthesis, leakage and clock rate optimization, VDD selection, power optimization, timing and electrical closure. Under normal conditions, a 40% decrease in dynamic power consumption and a 46% improvement in leaky power consumption have been achieved. The first silicon chip met all of the technical and electrical design requirements. Since technology scales down, power dissipation is indeed one of the most critical issues in nanoscale IC design, as leakage increases rapidly. However, optimising for both power and time might be a challenge. In this study, we present a new approach to optimising total power while still meeting performance goals.

4.1Introducing clock-gating into MBFF

An un-gated clock signal was used to drive the MBFFs detailed thus far. In the figure, the DDCG is shown embedded in a K-MBFF. A library cell holds all of the darkened circuits. According to [2,] the problem can be solved by choosing a group size k that saves the most energy for a given activity p. The clock generator loads of an Edf a latch, respectively, are represented by CFF and Clatch, respectively. Table 2 shows the answer to (4) for various CFF and Clatch actions.

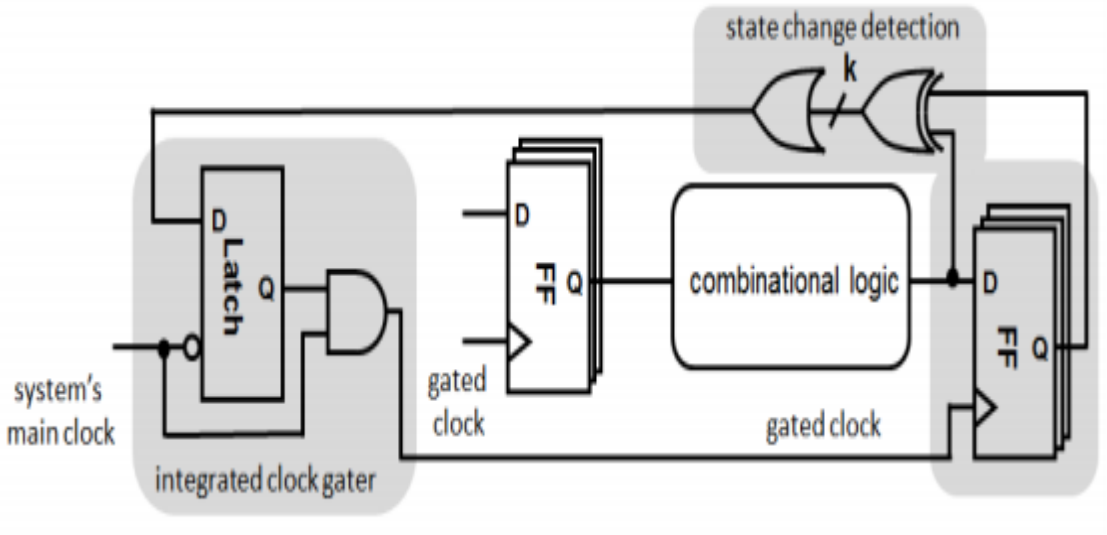


Fig 4: DDCG integrated into k -MBFF.

p	0.01	0.02	0.05	0.1
k	8	6	4	3

Table3: Dependency of the optimal MBFF multiplicity on toggling probability

.

Except where noted, all MBFFs in the sequels are DDCG. SPICE was used to simulate Fig. 4 for various behaviors p and multiplicities 2, 4, and 8 in order to better understand the power savings that can be achieved using DDCG in a k -MBFF. This graph displays the 2-MBFF's power usage in kilowatts. When two 1-bit FFs are driven independently of one another, the power consumption is shown in line (a). The switching of the clock controller at each FF consumes the 3.8 W power even when there is no activity, and this is always the case. Line (b) represents the ideal situation in which the two FFs switch at the same time. If this is the case, the internal gate in Fig. 5 disables the shared clock driver for the sake of both FFs or toggles it for them both. When comparing to two 1-bit FFs, the power consumption is practically halved when there is no activity. Due to the gating circuit's power consumption being proportional to activity, as activity increases, (bpower)'s grows quicker than (a's).Well beyond 0.17 activity road junction, where power starts to be lost.

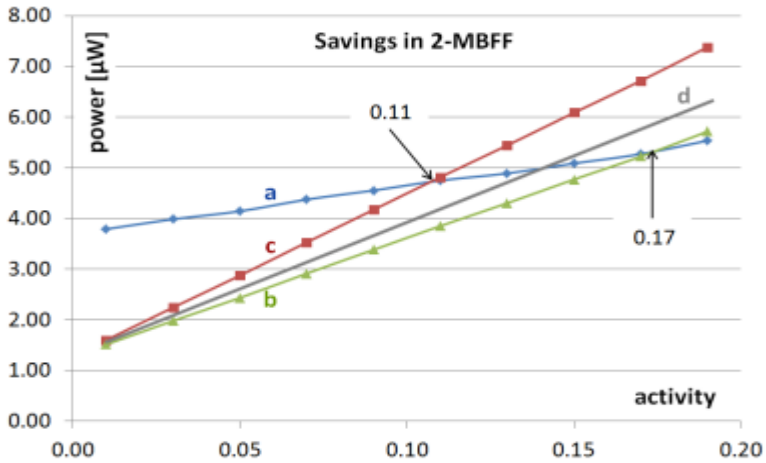


Fig 5: Power consumption of 2 FFs vs. 2-MBFF.

5. Results

Fig 5 Entity diagram:

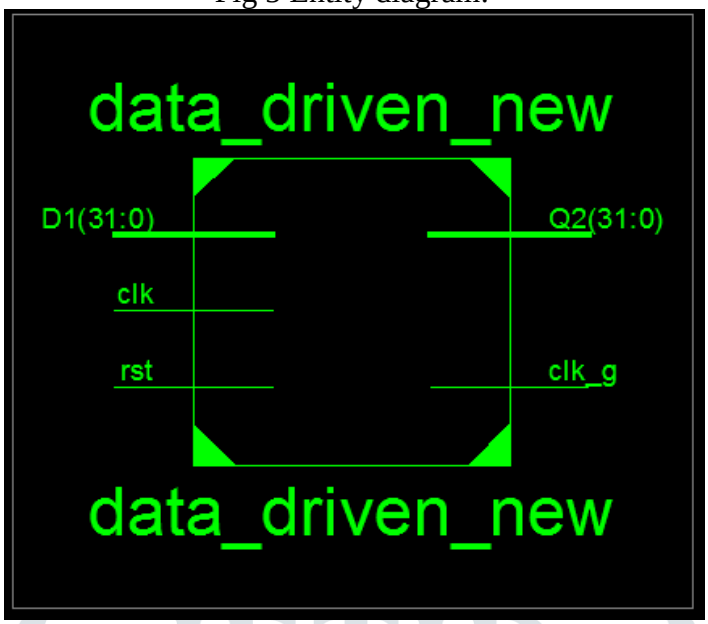


Fig 5 RTL schematic:

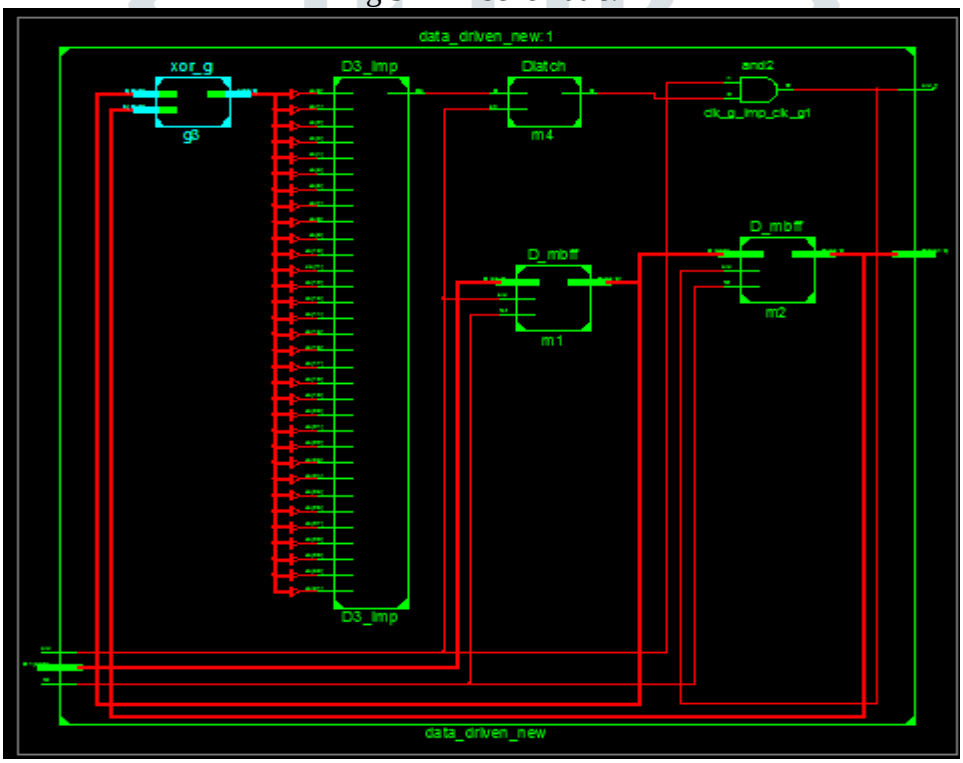
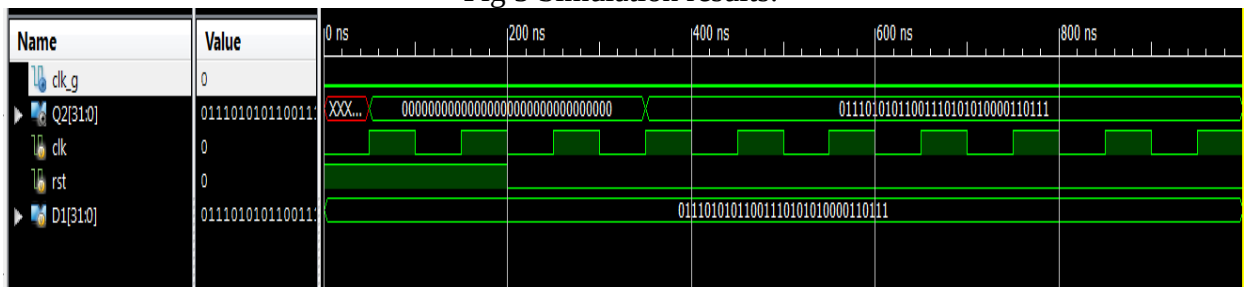


Fig 5 Simulation results:



6. Conclusion

FIFOs employ clock gating to lower their power usage. Clock gating & multi-bit flip flops in sequential circuits are utilised to reduce power consumption. Typical clock gating is a power saving technique. but it leaves behind more redundant pulses when using the clock gate. The power consumption of a multi-bit flip-flop can also be reduced. Multi-bit Flip-Flop decreases the total number of inverters by exchanging the

inverters between flip-flops. Further power savings can be achieved by combining a multi-bit flip-flop with data-driven clock gating. This proposed system is implemented using the Xilinx software tool. MBFF and data-driven gating are being used in tandem to see if we can save even more power.

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