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Abstract

In this study, a number of different types of transistors, such as MESFETs, MOSFETs, FinFETs, and SOI-FinFETs, are covered. We examined all of the devices and analysed their designs, drain current and voltage characteristics, operating speed, drain-induced barrier reduction, and latency. Because of this analysis, we are in a position to determine which pieces of machinery are superior in terms of the attributes they possess.

1 INTRODUCTION

Today's world is one where new technology are developing at an astoundingly fast rate. Fundamentally and significantly dependent on the underlying structure is this maturing process. The terms "bi-polar junction transistors" (BJTs) and "field effect transistors" (FETs) refer to the two most popular types of transistors (Field effect transistor). There are two separate kinds that make up the BJT: a Npn type and a Pnp type. In addition to BJT and FET transistors, there are also MOSFET, FinFET, IGFET, and MESFET. FinFET stands for silicon on insulator, while IGFET and MESFET stand for insulated gate and metal oxide semiconductor, respectively (Metal Semi-Conductor FET). For your viewing pleasure, the following picture depicts these categories (a). Every device has advantages and disadvantages; for example, both BJT and FET have a number of shortcomings, which led to the development of MOSFET as a remedy. Even while lowering the channel length led to a decrease in the number of nanometers, MOSFETs eventually encountered a number of issues, including as the short channel effect, parasitic capacitance, and others. To address these technological shortcomings, FinFET is used. DIBL, which stands for "Drain Induced Barrier Lowering," is one of the shortcomings of the FinFET design. The SOI-FinFET design has a problem with this. Both traditional FinFET and other kinds of devices cannot compete with SOI-threshold FinFET in terms of swing performance. The DIBL rate of SOI-FinFET is much lower as compared to FinFET. Because of its shorter short channels, SOI-FinFET has a significantly less impact when compared to FinFET and other technologies. Systems that are typically low-tech may benefit from the advantages of SOI-FinFET usage. When a transistor is placed in a region that blocks its output, it is said to be in a "OFF state." The transistor is not letting any current to pass through it, as seen by this(Karsenty and Chelly, 2015). Area Saturated When a transistor is in the saturation area, it is said to be in the on state and to be operating as a closed switch. Alternatively called the saturation region, this area is. shows that a significant quantity of current is being applied to the transistor. While the transistor is engaged in the circuit's active region, amplification is accomplished.

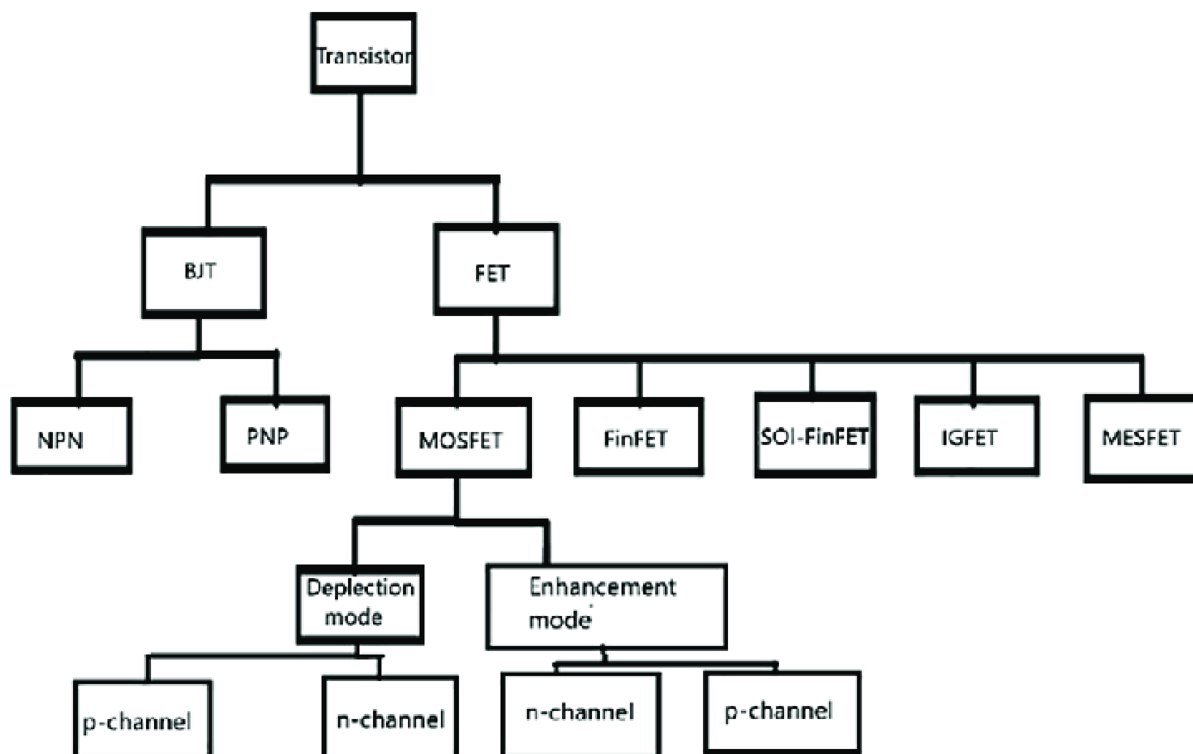

Figure1: Transistor architecture

2. Theory

2.1 MOSFET

The MOSFET has four terminals, which are known as the Source, Drain, Gate, and Body. In certain sectors, this device is also known as an insulated gate FET. The MOSFET's source and body terminals are constantly connected. As a result, it produces three terminals, similar to a FET. The metal oxide semiconductor field effect transistor, or MOSFET, is a kind of transistor that is utilised in both digital and analogue circuits. It is a voltage regulator. The gate of a MOSFET is the component that regulates the direction and quantity of current that flows between the source and the drain. MOSFETs may function in either the Depletion Mode or the Enhancement Mode. These two modes are distinguishable by their names. Depletion mode is distinguished by the existence of an inversion layer in the absence of a voltage applied to the gate terminal. When the gate voltage is equal to zero, the current flow between the Source and the Drain is at its maximum. This is because the drain terminal carries the highest charge. If the gate voltage is not "0" or gradually increasing, the current flow between Source and Drain is not "0" or gradually decreasing. This is because the two nodes are linked in series(Carmichael, 2017). Aside from that, it seems to be increasing gradually. When the device is in Enhancement mode and the gate voltage is not provided, there is often no inversion layer present. If the gate voltage remains constant, the amount of current flowing from the Source to the Drain will rise. If no voltage is provided to the gate terminal, no current will flow between the source and drain terminals. MOSFET nanoscale technology is shrinking, however the short channel is having a growing influence. This technology consumes much more electricity than FinFET. When compared to FinFET, the manufacturing stages are much more difficult. Current leakage and Drain Induced Barrier Lowering occur much more often than FinFET.

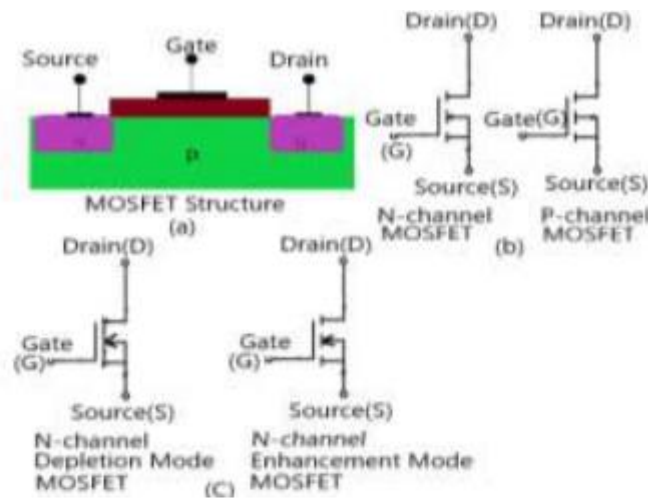

Figure 2: (a) Structure of MOSFET. (b) N, P-channel MOSFET symbols. (c) N-channel Depletion mode and Enhancement mode MOSFET symbols.

2.2 FinFET

Although they are both kinds of transistors, MOSFET and FinFET are quite different from one another. In a FinFET device, the source and drain structures are shaped like a fin, and the following image illustrates how the fin is inserted into the substrate. The gate stretches all the way around the canal, covering the outer surface on both sides. I wanted to be well-versed in the channel's fundamentals. It is essential that the gate has substantial control over the channel(Kundan, 2019). When compared to MOSFET devices, the doping of impurities in FinFET devices is much lower. FinFET is used to establish direct connections between the source, drain, and substrate. There is a certain degree of leakage as a result of these connections. Leakages have been greatly reduced as a direct consequence of the gate terminal's excellent channel control. There are two different methods that may be used to increase a FinFET device's driving current. One technique for increasing the channel's width is to build and connect several fins. You have another another choice, which is this. Because of the reduced doping and enhanced gate control, the short channel effect (SCE) is reduced even more. When compared to SOI-FinFET, FinFET has inferior SCE, DIBL, leakages, power consumption, and output current characteristics.

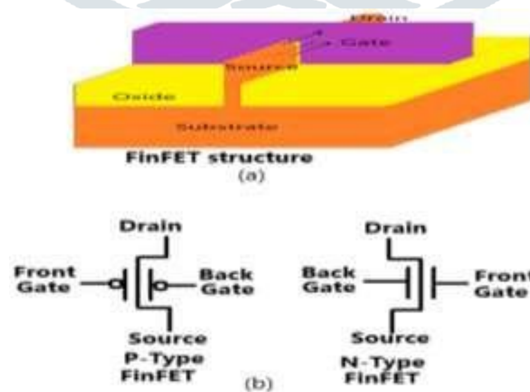

Figure 3: (a) FinFET Structure. (b) FinFET Symbols

2.3 MESFET

Field-effect transistor with a metal semiconductor (MESFET). Consumption mode MESFETs are widely and often used by circuits in a number of applications. There is no oxide layer anywhere between the gate and the substrate in a MESFET. The Schottky junction has recently taken the place of the oxide junction. The Schottky metal gate is in charge of regulating the flow of electrons from the source to the drain. Figure 4 depicts a MESFET with a conducting channel running between its source and drain. MESFET carriers have an edge over MOSFET carriers in terms of channel mobility. Silicon makes up MOSFET substrates, but MESFET substrates may be made of silicon carbide, indium phosphate, or gallium arsenide (GaAs). This demonstrates that MOSFET substrates are made of silicon since a MESFET substrate is a semi-isolating substrate. The aim of this work is to investigate a semi-insulating GaAs substrate. When compared to Silicon substrates, using GaAs substrates has two benefits. First off, the electron mobility at ambient temperature is more than five times larger than it is at higher temperatures. Second, it is feasible to develop a substrate composed of semi-insulating GaAs that, due to free carrier absorption, fixes the issue of the substrate absorbing microwave power. altering the depletion area to exert control over the current flow(Lin, Tao and Wu, 2019). The depletion area thus assists to distinguish the surface carriers. Schottky diodes turn on when the voltage hits 0.7V. The increased width of the depletion area results in a decrease in the amount of current that flows between the source and the drain when the gate voltage is raised.

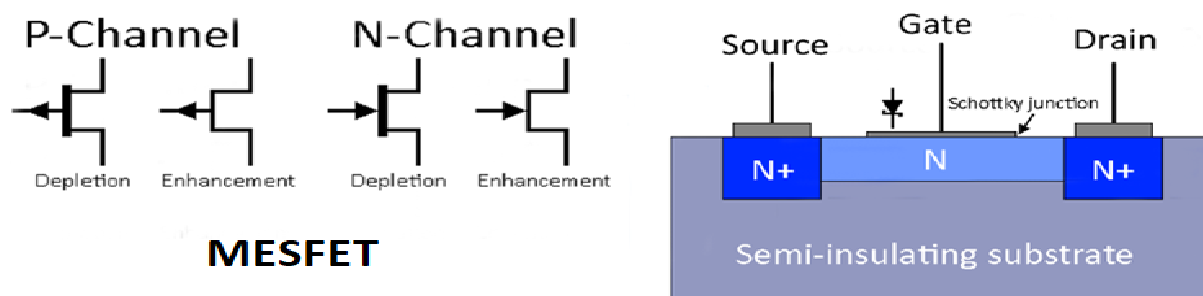

Figure 4: (a) MESFET structure. (b) MESFET symbol.

2.4 SOI-FinFET

When it comes to functional capabilities, SOI-FinFET and FinFET are essentially equivalent. The main difference between the two is that the oxide layer, sometimes referred to as the buried oxide layer, fully covers the substrate in SOI-FinFET (BOX). FinFET, on the other hand, does not only have a direct coupling between the source and drain and the substrate but also does not have an oxide layer in between the source and drain. The BOX layer will have much reduced leakage compared to MOSFET, FinFET, and MESFET(Krishna, Gaillardon and Bojnordi, 2019). SOI-FinFET switches significantly more quickly than other devices like MOSFET, FinFET, and MESFET. When compared to MOSFETs, FinFETs, and MESFETs, respectively, the DIBL has a lower threshold. The gate terminal offers a higher level of channel control in comparison to the MOSFET, FINFET, and MESFET. In contrast to MOSFETs, FinFETs, and MESFETs, the drain current is drawn more often at the output, and the quantity of doping impurities is much lower. More steps are required in the production of MOSFETs, FinFETs, and MESFETs than in the production of MESFETs.

3. RESULTS AND DISCUSSION

3.1 Drain Induced Barrier Lowering

Due to the short channel effect, DIBL will undoubtedly occur. The transistor would malfunction and become unusable if we increased the voltage at the drain terminal to the point where it exceeded the voltage at the gate. The connection between the source and the drain that has always existed is beginning to unravel. The DIBL value of an SOI-FinFET is lower when compared to other devices of an equal design. The three different kinds of transistors are MOSFET, FinFET, and MESFET. because an SOI-FinFET device has far less doping impurities than MOSFET, FinFET, or MESFET devices. The values of the MOSFET, MESFET, FinFET, and SOI-FinFET are presented in the next section in tabular and graphical form, respectively.

Table 1: Comparison DIBL value of different devices.

S.NO	Devices	DIBL (mV)
1	MOSFET	47
2	MESFET	120
3	FinFET	0.000053
4	SOI-FinFET	0.00005

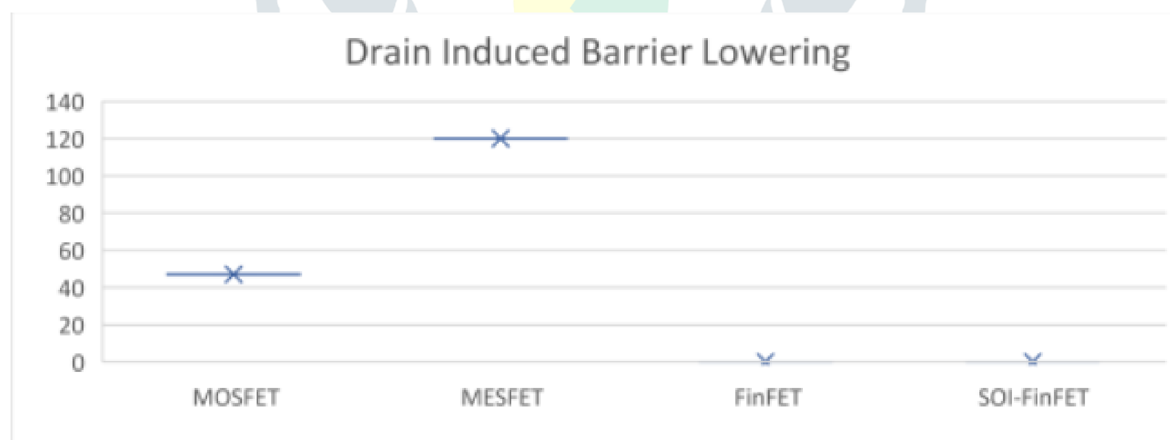

Figure 6 Graphical representation of DIBL of different devices is shown in above.

3.2 Leakage Current

The bulk of the current leakage that occurs between the source and drain occurs while the device is in the OFF state. FinFETs and SOI-FinFETs have substantially lower current leakage than MOSFETs and MESFETs. The SOI-FinFET has a leakage value of 7.77 x 10-8 nA, whereas the leakage value of the FinFET is around 8.62 x 10-8 nA. The current leakage that may be anticipated from MOSFETs, MESFETs, FinFETs, and SOI-FinFETs is shown in the accompanying table.

Table 2: Comparison of current leakages of different devices.

S.No.	Devices	Leakage Current
1.	MOSFET	High
2.	MESFET	High
3.	FinFET	Less
4.	SOI-FinFET	Very Less (7.77x10^-8 nA)

3.3 Short Channel Effect

When nanoscale technology is scaled down, the effects of having short channels will become more obvious. When the MOSFET's nanoscale size is reduced, the SCE increases extremely quickly(Mari, 2022). To get around this problem, FinFET is employed. SCE has been significantly reduced as a consequence of FinFET adoption, and the nanoscale size is also decreasing. On the other side, the SOI-FinFET has a lower SCE count than the FinFET. due to the much reduced level of doping pollutants in SOI-FinFET. The comparison table that follows offers a SCE study of a variety of electrical equipment kinds.

Table 2: Comparison of current leakages of different devices.

S.No.	Devices	SCE
1.	MOSFET	High
2.	MESFET	High
3.	FinFET	Less
4.	SOI-FinFET	Very Less

3.4 Subthreshold Slope

The subthreshold slope is an enhanced swing that more accurately assesses the device's performance than any other metric. When a MOSFET is tested at room temperature, its subthreshold slope is 70 millivolts per degree. The gadget switches between its ON and OFF states extremely fast, which is strongly suggested by the slope's steepness in the subthreshold area. A FinFET device typically has a subthreshold slope of 0.982, but an SOI-FinFET device has a subthreshold slope of 0.062, making the SOI-FinFET device preferable to the FinFET device. MESFET The subthreshold voltage between the SOI-FinFET and

the MOSFET is the same; neither one is superior than the other. Comparison of the Subthreshold slope of different devices is shown below tabular form. (Peterson, 2022)

Table 4: Comparison of subthreshold slope of different devices is shown below.

S.No.	Devices	S.S V/dec
1.	MOSFET	0.70
2.	MESFET	~0.60
3.	FinFET	0.982
4.	SOI-FinFET	0.062

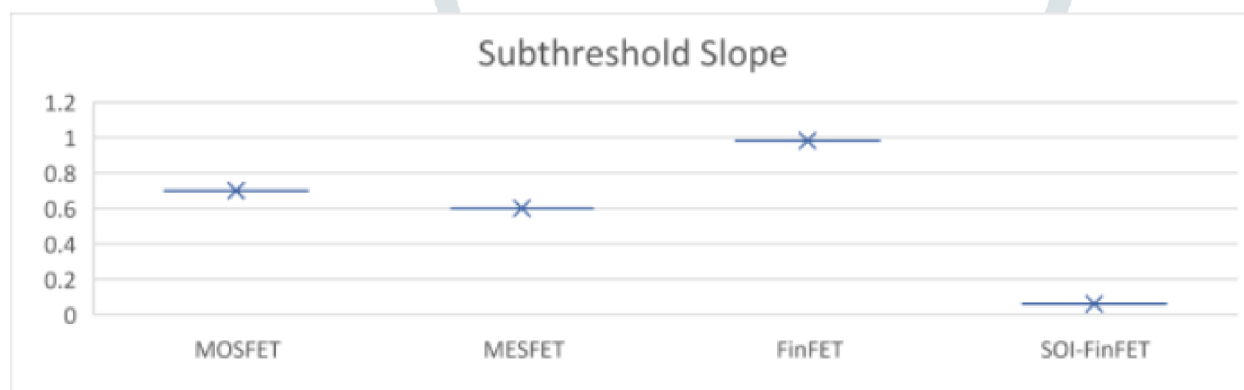

Figure 7: Graphical representation of Subthreshold slope of different devices is shown above.

IV. Conclusion

When the results of every study are combined, SOI-FinFET outperforms MOSFET, MESFET, and FinFET in terms of parameter values. The SOI-FinFET performs better in terms of subthreshold inclination compared to MOSFET, MESFET, and FinFET. The contribution of SOI-FinFET to DIBL is substantially less when compared to MOSFET, MESFET, and FinFET. The SCE of SOI-FinFET is substantially lower than that of any of the other two technologies when compared to MOSFET, MESFET, and FinFET. The switching speed of SOI-FinFETs is much faster than that of MOSFETs, MESFETs, and conventional FinFETs. Soi-FinFET has substantially reduced current leakage and power dissipation when compared to MOSFET, MESFET, and FinFET.

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