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HIGH PERFORMANCE BIT-PLANE DECOMPOSITION MATRIX-BASED VLSI INTEGER TRANSFORM ARCHITECTURE FOR HEVC

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Abstract

VLSI integer transform structure for High Performance Video Coding (HEVC) processor is proposed in these brief Signed bit-plane transform matrices (SBT) formed from bit-plane decomposition method of integer transform matrices (HEVC) are used to create the architecture. The binary weighted sum of numerous SBT matrices that are simply composed of binary 0 or 1 can be equivalently written as an integer transform matrix. They are relatively simple and have a lesser bit width than that of the original arithmetic transform in form, which is why they are more efficient. There are a lot of zeros in the SBT matrices as well. Using the sparseness of SBT grids is a great way to reduce the number of addition operators. An SBT matrix can be used to transform video data instead of just the original integer transformation in high bit width, as shown here. Thus, the suggested SBT reduces the transform unit circuit's delay greatly. Furthermore, we suggest an adder reuse method for our transform scheme based on the redundancy element character of SBT multipliers, in which the parts are either 0 or -1. Simulated findings suggest that a VLSI transform architecture may be synthesised in a suitable area with a high operating frequency and low latency by utilising the methodologies that have been proposed. The architecture is capable of supporting all real-time HEVC encoders for ultra-high-definition video.

Key words: Bit-plane matrix, High Efficiency Video Coding (HEVC), integer transform, ultra high definition (HD), very-large-scale integrated (VLSI) architecture

1. Introduction

This new standard, HEVC, was created in order to provide double the compression ratio of H.264 / AVC. Video compression efficiency statistics vary according to the type of information and the codec settings, however HEVC is often twice as efficient as AVC at normal consumer media distribution bit rates. The Discrete Wavelet Transform (DCT), commonly used in image and video compression formats including JPEG, MPEG-2/4, and

H.263, can benefit end users in two ways: either directly or by combining both of these techniques. Because of its capacity to transform spatial data into frequencies, it has become a popular tool. After being converted, data will be much more compact and superfluous data will be eliminated. Compared to the K-L transform, this DCT is considered the most appropriate energy compression transform. DCT's matrices, on the other hand, contain real numbers represented by a finite amount of bits, making drift inevitable (mismatch between the decoded data in the encoder and decoder). Before the introduction of H.264, a number of strategies were used to limit the buildup of drift of video encode standards. In contrast, H.264 is extremely sensitive to drift because of its heavy use of prediction. [2] The latest video standards, such as H.264, VC-1, and AVS, are beginning to use integer transforms to avoid encoder and decoder mismatches and to promote low-complexity implementations. For high - quality video processing, HEVC (High Efficiency Video Coding) is the latest standard. H.265 is viewed as H.264's heir apparent. According to its official mission statement, HEVC intends to improve on H.264's coding efficiency by 50%. HEVC employs a wide range of cutting-edge coding techniques, including 4/8/16/32 integer transforms. Compared to H.264, the size of both the matrices themselves and the elements in the matrices grows. As a result, both hardware & software implementation becomes extremely difficult. This paper presents a fast HEVC 8x8 integer transform technique that can be implemented in hardware or software. Because graphical interface of the signal is more resilient than the analogue counterpart when it comes to long-distance processing, subterfuge, storage, recovery, and transmission through communication networks, today we are discussing digital networks, digital representations of images, movies, video, television, voice, and a digital library. As digital computers have become more powerful, they have made major advances in the processing of still picture, video, pictures, speech, and audio information. Information in the form of image, video and audio files as well as text files has the ability to be reduced to the status of data. In both academia and industry, the development of efficient picture compression algorithms remains a major challenge. Later, in order to save space, ROM-based DA was used to create DCTs, rather than multiplier-based ones. As a result, DA-based multiplication using ROMs were created to yield partial products, along with adders that tallied up these partial products. Using DA-based ROM in DCT core design allows us to reduce the amount of space needed for the chip. DCT translation and parallelism DA construction can be be employed to reduce the size of the ROM, as well. Architectures that don't require the use of ROM have recently been introduced. New DA was constructed using a bit-level sharing mechanism devised by Shams et al (NEDA). With 35 adders and 8 shift addition elements replacing the ROM, the butterfly-adder-matrix was compressed. Due to space constraints, the cyclic form and ALU were used in DCT design in order to reduce area costs, but the processes of serial switching and add after the DA-computation have a limited performance. There is a concurrent shift and addition of partial product words in DA-based computing. There was, however, a very huge truncation error.

We must minimize the truncation error that results from removing the smallest possible segment of the input data. Several error compensating bias methods based on statistical examination of the relationship entre data block and multiplier-multiplicand have been given in order to lessen the influence of truncation error. It is possible to lower the complexity of the hardware by minimizing truncation errors. Truncating the truncation part (TP) in linear moving and addition operations, also know as the direct termination (Direct-T) method, generally reduces hardware costs. As a result, the TP to Basic Part carry propagation is neglected, resulting in a substantial truncation error (MP). To disguise multiplications, a bit-level reorganisation of a multi accumulate is used in distributed arithmetic. Reduce the size of a concurrent hardware multiply accumulate using this effective strategy, which works well with FPGA designs. Images can be compressed by employing the Discrete transform (DCT) in digital image processing, particularly in image discrete cosine transform. In contrast to the majority of them, a handful of them are truly suited for VLSI implementation. Because of its simplicity, cyclic convolution is widely used in digital signal processing. Numerous convolution algorithms have been discovered and can be implemented with ease using modules & modular technology such as distributive arithmetic and syntactic array (DAS) units. The efficiency of a transform employing the DA is mostly determined on the method of data transport.

2. Literature survey

The Joint Cooperation Team on Video Processing (JCT-VC) of the ITU-T Video Compression Advisory Council (VCEG) and indeed the ISO/IEC Motion Picture Specialists Group (MPEG) standards organizations has developed the High Endurance Video Coding (HEVC) standards [1]. ITU-T and ISO/IEC are both anticipated to publish an aligned text during the first generation of such HEVC standard in January 2013. Extensions to the

standard are intended to accommodate a variety of new application scenarios, such as scalable video coding, 3-D/stereo/multi-view audio video coding, and extended-range usage with improved precision and colour format support. When the HEVC standard is adopted by ISO/IEC and ITU-T, it is expected to become Video compression Part 2 (ISO/IEC 23008-2) & ITU-T Recommendation H.265.
The creation of a well ITU-T and ISO/IEC guidelines has largely been responsible for the evolution of video coding standards. For example, the ITU-T generated H.261/MPEG-2 Video and H.264/MPEG-4 AVC, whereas ISO/IEC produced MPEG-1 Visual and MPEG-4 Visual, respectively. Our daily lives have become progressively enriched by products incorporating the seven principles that were jointly developed. It has been an ongoing effort to enhance compressed ability and boost other qualities such as information leakage robustness while keeping in mind the computation time that were viable for usage in value at the time of planned deployment for each standard. After the development of H.264/MPEG-4 AVC between 1999 and 2003 and subsequent extensions from 2003 to 2009, HEVC emerged as the dominant video coding standard. For digital video, H.264/MPEG-4 AVC has always been a game-changer in nearly every area where H.262/MPEG-2 Video had previously failed to deliver, and it has mostly superseded the older standard in those areas where it still finds use. Satellite, cable, and mobile TV broadcasts, video content gathering and editing systems (camcorders), security applications, Blu-ray Disc playback (as well as real time conversational applications like video chat) are just a few of the many uses for high definition (HD) video. An ever-increasing variety in services, the rise of HD video, or the rise of beyond HD forms (such as 4k2k or 8k4k quality) are producing even higher demands for component superior to H.264/MPEG-4 AVC's capabilities. When stereo or multi-view capture and presentation are combined with increased resolution, the requirement becomes even more pressing. As a result, today's networks are being strained to their limits by the volume of video traffic generated by mobile and tablet PC apps and video-on-demand services. Mobile applications are also seeing a rise in demand for better quality and resolutions.

2.1 Overview of the H.264/AVC video coding standard.
The ITU-T Video Compression Experts Council and the International organization for standardization Moving Picture Experts Group have just released H.264/AVC, their newest video coding standard. Enhancing compression performance and providing a "network-friendly" video representation for "conversational" (video telephony) and "non-consensual" applications are at the heart of the H.264/AVC standardisation effort. In comparison to previous standards, the rate-distortion efficiency of H.264/AVC has improved significantly. We'll take a look at the history of H.264/standardization AVC's process, as well as its key technical characteristics, profiles, and applications, in this post. Thomas Wiegand holds a PhD in electrical science from the University of Tübingen and a Dipl.-Ing. in power electronics from the National University of Hamburg-Harburg. Image Communication Group Head, Fraunhofer–Institute for Telecommunications–Heinrich Hertz Institute (HHI) in Berlin, Germany, where he works. While at Stanford University in 1997 and 1998, he was a Senior Researcher and a Consultant at 88, Inc., Santa Monica, CA. He was a visiting lecturer at Kobe University in Japan from 1993 to 1994. In the University of San Barbara in 1995, he was really a Visiting Scholar and began his study on compression techniques and transmission. His contributions to the standardisation efforts of ITU-T, ISO/IEC, and the Joint Video Team have made him a well-known figure in the field of video coding, and he has numerous patents in this area. As an Affiliated Reader of the ITU-T VCEG (Oct 2000), he was also designated the Affiliated Public prosecutor of the JVT that was founded by ITU-T VCEG / ISO/IEC MPEG for a finalisation of H.264/AVC video standard (December 2001). (February 2002). At the University of Louisville in Louisville, KY in 1982, Gary J. Sullivan (S'83–M' 91–SM'01) earned a B.S. and an M.Eng. in power electronics before moving on to the California state University, Los Angeles, where he earned his Ph.D. and an Eng. in electrical engineering. ITU-video T's coding experts group and ISO/moving IEC's picture experts group collaborated on the H.264/MPEG4-AVC next-generation video coding standard, and JVT Chairman He is responsible for overseeing the progress of the JVT (MPEG). For the past six years, he has been the ITU-T Chair of Advanced Video Coding (VCEG). He has also served as the Video Liaison Member of the ITU-T to MPEG (ISO/IEC JTC1/SC29/WG11), serving as the MPEG's video chairman from 2001 to 2002. DirectX® Video Acceleration API/DDI, part of the Windows® operating system, was invented by him and he continues to serve as lead engineer in the eHome A/V Platforms Group at Microsoft Corporation in Redmond, WA. Previously, he was the President of Telecommunications Core Study at PictureTel Company, a former leading country in videoconferencing communication. Prior to joining Texas Instruments, he served as a Jack Hughes Fellow and a member of something like the technical staff at Hughes Aircraft Corporation's Sophisticated Technology Division. Video and image compressing, rate-distortion optimization, motion modeling, scalar and vector

quantization, or delivery services and packet-loss-resilient video coding are a few of his field of study and areas of publishing. Physical science doctorate conferred on Gisle Bjntegaard in 1974 by University of Geneva, Oslo, Norway. He worked in Telenor Research & Innovation in Oslo, Norway, as a Leading Scientist from 1974 to 1996. His research specialties included the design and construction of reflector antennas, digital signal processing, and the construction of video compression technologies. Telenor Internet Services, Oslo, Norway, employed him from 1996 to 2002 as a Group Manager for point-to-point communication systems and digital television platform development. A Chief Engineer at Tandberg Telecommunication, Lysaker, Norway has been working on clip development and implementation since 2002, when he joined the team. He has actively led to the advancement of the ITU video requirements H.261, H.262, H.263, & H.264, as well as ISO/IEC MPEG2 and MPEG4. Ajay Luthra (S'79–M'81–SM'89) earned his B.E. (Hons.) from BITS Pilani, India, in 1975, his M.Tech. in information and communication construction from Iit Bombay, Delhi, India, in 1977, and his Ph.D. While at Interspec in Philadelphia, he worked on biomedical applications of digital digital signal processing from 1981 to 1984, as a senior engineer. In the years 1985-1990, he served as manager of the Integral Form and Picture Processor Group at Tektronix, Beaverton, OR, and in the years 1990–1995, he directed the Communication systems Systems Research Lab. Senior Executive in Advanced Technology Firm at Motorola (formerly General Instrument) in San Diego, CA, he is involved in developing advanced digital sharing content and computation, video files, interactive TV, cable nose system design, as well as advanced set-top-box architectures in the area of digital video compression. This MPEG committee member has chaired many technical subgroups during the last decade. A member of the Joint Video Team, which includes Astm and ITU-T/H.26L professionals working on the next generation of visual coding standards, he serves as an associate rapporteur and co-chair. When he was not working on his dissertation, Dr. Luthra served as a guest editor for the International Journal of computer on Devices and Circuits for Video Technology as well as a former editor (2000-2002). (March 2001).

3. Functional modules

3.1 HEVC description

This new standard, HEVC, was created in order to provide double the compression ratio of H.264 / AVC. Video compression efficiency statistics differ based on the type of material and the encoding settings, however HEVC is often twice as efficient as AVC at general consumer digital streaming bit rates. There are two ways that greater compression efficiency can benefit end users (or some combination of both)

3.2 Types of compressions

Depending on the type of compression, there are two options.

1.Compression that does not lose any data.

2.Lossy compression

The signal is discarded if it contains elements that are recognized to be unnecessary. In this way, the signal is transformed from the input.

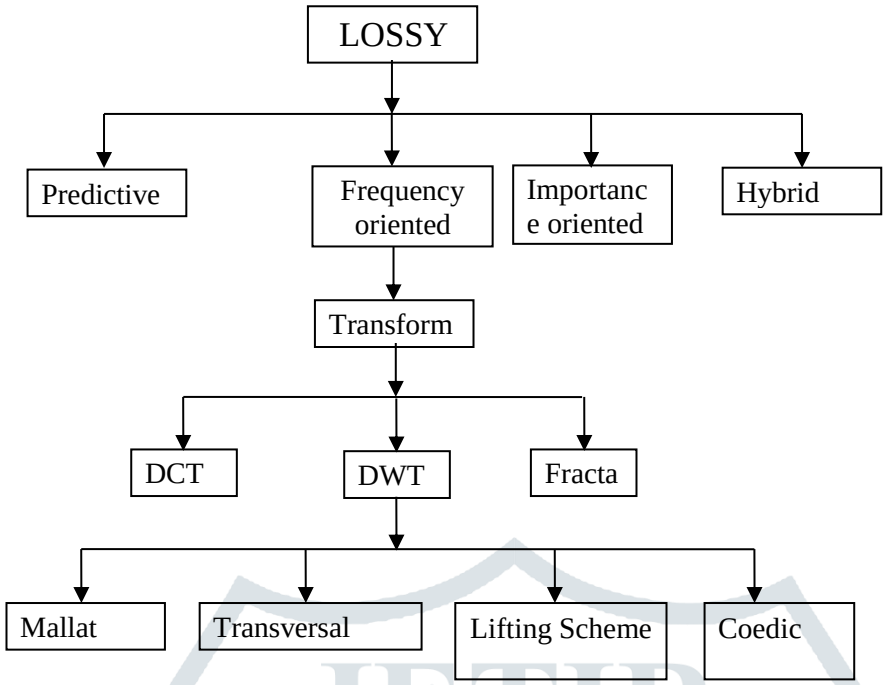


Figure 1 Different Types of Lossy Compression Techniques

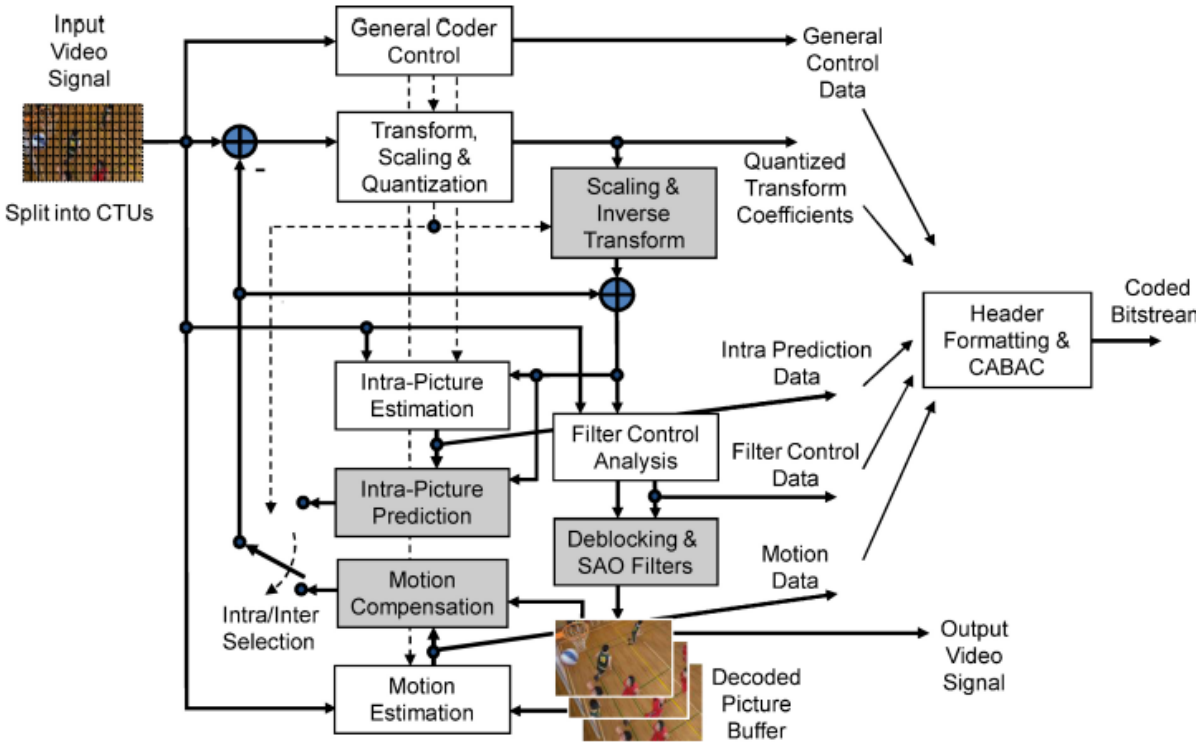
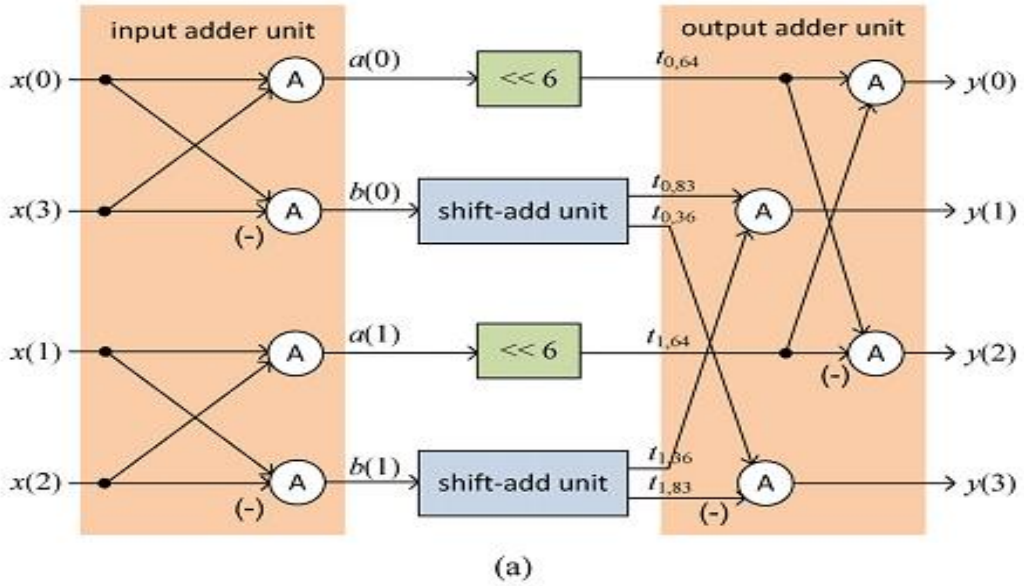


Fig. 2. Block Diagram of HEVC

3.3 Architecture for Four-Point Integer DCT:

Figure 3 depicts the suggested architecture for a four-point integer DCT. IAU, SAU, and OAU are the three main components of this system (OAU). The IAU calculates a(0),a(1),b(0), & b(1) so according Table I's STAGE-1 procedure. Two SAUs do the evaluations of ti,36 & ti,83 in STAGE-2 of the procedure. To compute t0,64 and t1,64 in hardware, no logic is required because shift operations can be rewired. Stage 3 of the method adds the SAU outputs to the OAU outputs.



(a)

Figure 3 Architecture for Four-Point Integer DCT

4. Proposed system

4.1 Signed bit matrix-based transform algorithm.

Decomposition of the Integer Transform in Bit-Planes Our proposed bit decomposition approach reduces the bit breadth of transitional converted data by decomposing the integer transformation matrix into many SBT matrices. Diaj is the ith row and ith column of DN's integer transform matrix, which is di,j=DN=N=N=N=N (di,j). If di,j is optimistic, the binary formulation of di,j is (bK1,i,j,..., b1,i,j b0,i,j)2, bk,i,j = 0, 1 for bK,i,j. Then there's the linkage issue.

$$d_{i,j} = \sum_{k=0}^{K-1} \left(\mathrm{sgn}(d_{i,j}) b_{k,i,j} 2^k\right), \; b_{k,i,j} \in \{0,1\} \qquad (1)$$

the kth binary significant bit of element di,j is denoted by the notation "bk,i,j," and the function sgn() is the sign signaling function which takes 1 for a positive value and 0 for a negative value, which is expressed as "sgn(x)=[1,x>0@-1,x0]". As a result, (1) can be written as well.

$$d_{i,j} = \sum_{k=0}^{K-1} (b_{k,i,j} 2^k), \; b_{k,i,j} \in \{0, \mathrm{sgn}(d_{i,j})\} . \qquad (2)$$

Signed integer binarization is the result of Equation (2). The kth bit planes, which is written as N N SBT matrices BN,k = (bk,i,j), is created by binarizing all di,j elements in integer transform matrices DN and all the kth bits of every binary di,j, bk,i,j, 0 I j N.

$$D_N = \sum_{k=0}^{K-1} (B_{N,k} 2^k) \qquad (3)$$

A bit width K is defined as K = log2 max(di,j) for the largest member in the DN matrix. BN,k, which has only entries with values of 0 or 1, is the SBT matrix. When a matrix is decomposed, it produces K SBT matrices. A N N integer transformed matrix DN is decomposed into K N N SBT matrices (equation (3)) using the bit-plane decomposition method. Using the bit-plane decompose (3), the sum of K SBTs can be used to represent the integer transform as follows:

$$D_N X_N = \sum_{k=0}^{K-1} (B_{N,k} 2^k X_N) = \sum_{k=0}^{K-1} (B_{N,k} X_N 2^k) \quad (4)$$

And BN,k XN is just the kth SBT with input feature XN.. As seen in Equation (4), K SBTs can take the place of the integer transform. The ultimate result of something like the integer change can be obtained by multiplying the bitstreams of each SBT by 2k and accumulating it, as explained in the article (4). As compared to DN, the SBT matrices are simple and simply have 0 and -1 elements. Figure 1 depicts an illustration of the HEVC 8-by-8 integer transition D8 or its fifth SBT matrix B8,6

$$D_8 = \begin{pmatrix} 90 & 87 & 80 & 70 & 57 & 43 & 25 & 9 \\ 87 & 57 & 9 & -43 & -80 & -90 & -70 & -25 \\ 80 & 9 & -70 & -87 & -25 & 57 & 90 & 43 \\ 70 & -43 & -87 & 9 & 90 & 25 & -80 & -57 \\ 57 & -80 & -25 & 90 & -9 & -87 & 43 & 70 \\ 43 & -90 & 57 & 25 & -87 & 70 & 9 & -80 \\ 25 & -70 & 90 & -80 & 43 & 9 & -57 & 87 \\ 9 & -25 & 43 & -57 & 70 & -80 & 87 & -90 \end{pmatrix} \quad (5)$$

$$B_{8,6} = \begin{pmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & -1 & -1 & -1 & 0 \\ 1 & 0 & -1 & -1 & 0 & 0 & 1 & 0 \\ 1 & 0 & -1 & 0 & 1 & 0 & -1 & 0 \\ 0 & -1 & 0 & 1 & 0 & -1 & 0 & 1 \\ 0 & -1 & 0 & 0 & -1 & 1 & 0 & -1 \\ 0 & -1 & 1 & -1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & -1 & 1 & -1 \end{pmatrix}. \quad (6)$$

5. Results

Fig4:Entity diagram:

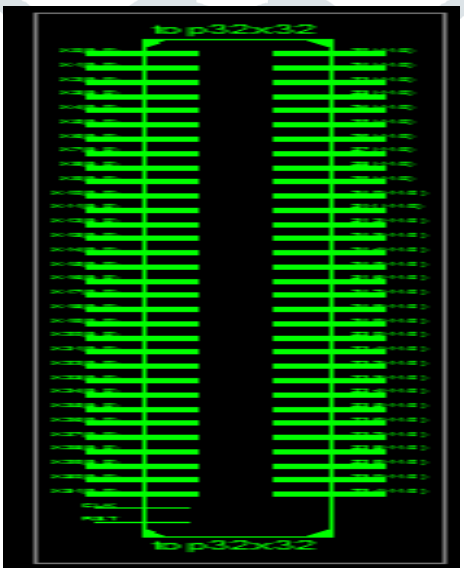


Fig5:RTL schematic:

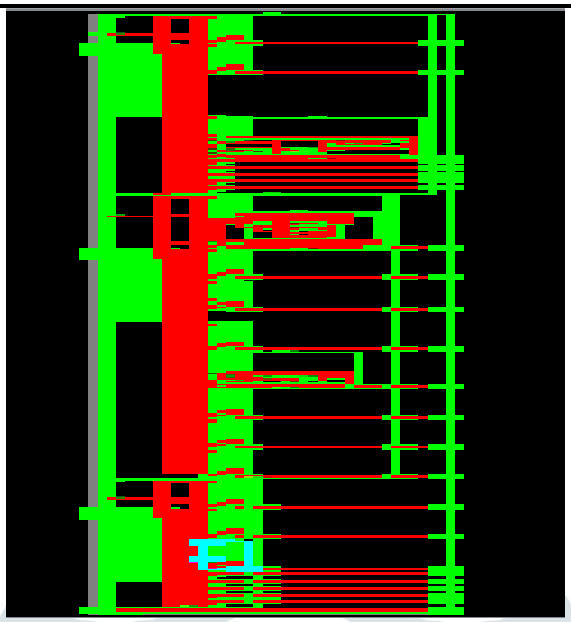
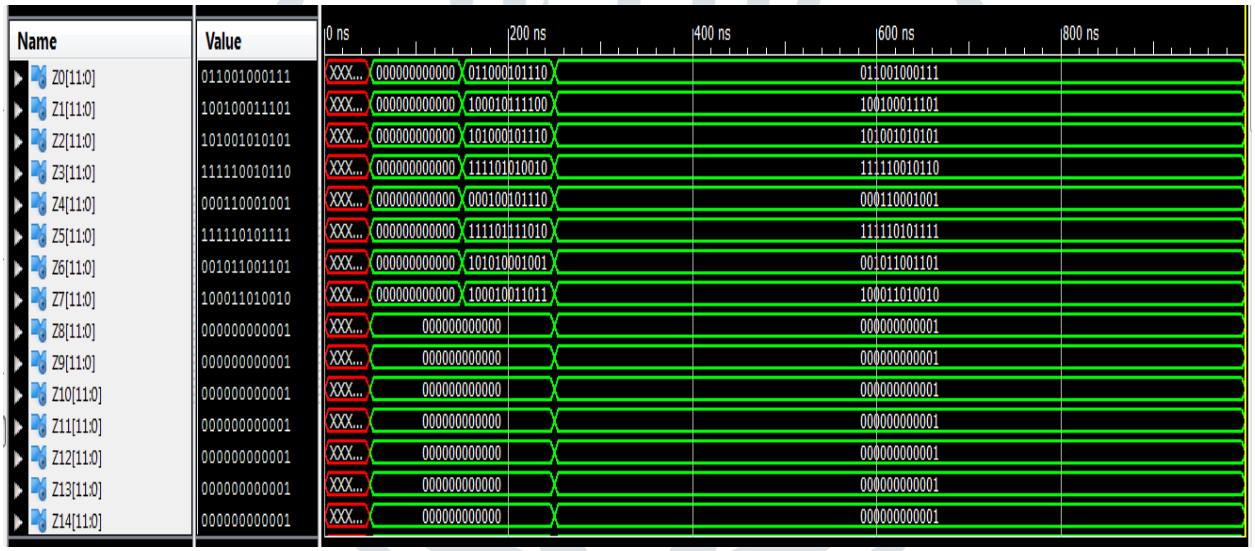


Fig6:Simulation results:



6. Conclusion

Integer to float conversion In order to adapt to the HEVC standard for ultra HD video coding, a VLSI engineering-based insufficient SBT has been proposed. The bit breadth of the numerical change framework is increased in the suggested VLSI architecture because of its impact on circuit delay. Lattice bit plane deterioration is used to reduce the number change lattice to a few SBT crystal lattice with low-piece-width components using the proposed technique. For low-piece width calculations, the change engineering with SBT calculation can be more productive. The SBT's suggested circuit reuse mechanism is designed to reduce the number of ripple carry adder in the VLSI design. The proposed network reuse technique saves a significant number of ripple carry adder for the SBT. It is possible to process video data at a faster rate and in a more efficient manner using the suggested transform hardware design.

7. References

[1] N. Ahmed, T. Natarajan, and K. R. Rao, “On image processing and a discrete cosine transform,” IEEE Trans. Comput., vol. C-23, no. 1, pp. 90–93, Jan. 1974.
[2] G. K. Wallace, “JPEG still image data compression standard,” Commun. ACM, vol. 34, no. 4, pp. 30–44, Apr. 1991.
[3] “Generic coding of moving pictures and associated audio information Part 2: Video ITU-T and ISO/IEC

JTC1," in ITU-T Recommendation H.262, ISO/IEC 13818-2 (MPEG-2), Nov. 1994.
[4] "Video coding for low bit-rate communication Version 1," in ITU-T Recommendation H.263, Nov. 1995.
[5] T. Wiegand, G. Sullivan, G. Bjontegaard, and A. Luthra, "Overview of the H.264/AVC video coding standard," IEEE Trans. Circuits Syst. Video Technol., vol. 13, no. 7, pp. 560–576, Jul. 2003.
[6] L. Yu, S. Chen, and J. Wang, "Overview of AVS-video coding standards," Signal Process., Image Commun., vol. 24, no. 4, pp. 247–262, Apr. 2009.
[7] G. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, "Overview of the high efficiency video coding (HEVC) standard," IEEE Trans. Circuits Syst. Video Technol., vol. 22, no. 12, pp. 1649–1668, Dec. 2012.
[8] W.-H. Chen, C. H. Smith, and S. C. Fralick, "A fast computational algorithm for the discrete cosine transform," IEEE Trans. Commun., vol. COM-25, no. 9, pp. 1004–1009, Sep. 1977.
[9] A. Ahmed, M. U. Shahid, and A. ur Rehman, "N-point DCT VLSI architecture for emerging HEVC standard," VLSI Design, vol. 2012, 2012, Art. no. 752024.
[10] Y. Arai, T. Agui, and M. Nakajima, "A fast DCT-SQ scheme for images," Trans. IEICE, vol. E71, no. 11, pp. 1095–1097, Nov. 1988.
[11] K. M. Tsui and S. C. Chan, "Error analysis and efficient realization of the multiplierless FFT-like transformation (ML-FFT) and related sinusoidal transformations," J. VLSI Signal Process. Syst., vol. 44, no. 1–2, pp. 97–115, Aug. 2006.
[12] S. H. Zhao and S. C. Chan, "Design and multiplierless realization of digital synthesis filters for hybrid-filter-bank A/D converters," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 10, pp. 2221–2233, Oct. 2009.
[13] P. K. Meher, S. Y. Park, B. K. Mohanty, K. S. Lim, and C. Yeo, "Efficient integer DCT architectures for HEVC," IEEE Trans. Circuits Syst. Video Technol., vol. 24, no. 1, pp. 168–178, Jan. 2014.
[14] W. Zhao, T. Onoye, and T. Song, "High-performance multiplierless transform architecture for HEVC," in Proc. IEEE Int. Symp. Circuits Syst., May 2013, pp. 1668–1671.
[15] A. D. Darji and R. P. Makwana, "High-performance multiplierless DCT architecture for HEVC," in Proc. IEEE Int. Symp. VLSI Design Test, Jun. 2015, pp. 1–5.