Performance Analysis of a Low Power and Area 8-Bit Carry Select Adder

V.Venkata Ramanamma,

Department of Electronics and Communication Engineering
ISTS Womens Engineering
College
Andrapradesh, India.

Mr.J.Kiran Chandra Sekhar, Ass Professor,

Department of Electronics and Communication Engineering ISTS Womens Engineering College
Andrapradesh, India.

***Abstract*—In microprocessors, DSPs, different kinds of arithmetic building blocks such as adder, subtractor, multiplier and divider are required to compute binary data. The priority of data path can be operation speed, low power consumption, area or design time. The most important design goals in many cases are area and low power consumption. The basic structure in any arithmetic block is an adder circuit. Hence, by optimizing the adder circuit, area and low power consumption can be achieved. Several kinds of adders have been proposed to reduce the worst-case propagation delay from Least significant bit(LSB) to Most significant bit(MSB). The Carry select adder is one of the adder architectures that reduces the carry propagation delayby grouping sub-block of adders. Many techniques can be used to improve the CSA performance as proposed by researchers in previous work that is, by using BEC-1(Binary to eccess-1 converter), using D-Latch etc. In this work, the CSA is designed using GDI(Gate diffusion input) technique and using both GDI and MTCMOS D-Latch to achieve better performance as compared to previous work. Tanner and Mentor Graphics 250nm CMOS Technology is used for simulation. The design of CSA using GDI logic achieved a tremendous improvement in power consumption and Transistor count of 99.45% and 58.85% respectively as compared to theconventional CSA.**

***Keywords*—CSA, MTCMOS D-Latch, GDI, Low Power, High Speed**

I. INTRODUCTION

Over the last few decades, phenomenal growth has occured in the electronic industry mainly due to rapid advances in the large-scale system design and integration technologies [1]. For high-performance and other scientific and engineering applications, digital CMOS ICS have been the driving force behind very-large-scale-integration(VLSI) [1]. The use of integrated circuits in high-performance computing, consumer electronics and Telecommunications has grown at a very fast pace. The driving force for the fast development of this field is typically, the required information and computational power of these applications. Although the Ripple carry adder is the simplest multi-bit adder architecture, the carry signal delay will increasesignificantly when the number of bits is increased to 32 or 64 bits [1].

The Ripple Carry Adder(RCA) is the less complex in terms of area but the slowest adder circuit and the Carry Look Ahead Adder(CLA) has opposite characteristics ie it is the fastest adder circuit but a complex structure in terms of area [2] [3]. A compromise between the high speed Carry Look and the simple and less complex Ripple Carry Adder results in the Carry Select adder(CSA) which plays a very important rolein different processing systems fort faster and area efficient applications. The traditional CSA consists of two identical adders(RCA) with different carry inputs, respectively 0 and 1 [4] [5]. For each block, the carry output signal pair is calculated in advance using both inputs carry of 0 and 1.With a 2:1 MUX, the sum of each block is selected usingthe output carry of the previous block as control signal [6] [7] [8]. As two sets of RCA are used in parallel, this configuration results in a high delay and has more area. Hence, there is need of new technique to reduce the delay, area and even the power consumption. Among the new Techniques proposed by Researchers are: replacing the RCA with input carry of 0 or1 by a Binary to excess-1 converter(BEC-1) or use a D-Latch instead of BEC-1.

To get more speed a Multiple-Threshold CMOS (MTC-MOS) D-Latch can be used to replace RCA with Cin=0. [2] [9].

In previous work, Carry select adder was designed using D-Latch and then using MTCMOS D-Latch to get good operation speed but both techniques focus more on the operation speed rather than both operation speed and low power consumption [2]. Hence, there is a need of a new technique which would minimize the propagation delay and minimize the power consumption. To meet this requirement, in this paper, Gate diffusion input(GDI) Technique and the use of both GDI and MTCMOS D-Latch are proposed and achieves the best performance in terms of operation speed and low power consumption as compared to other methods. The above explained in detail in subsequent sections.

GDI BASIC FUNCTIONS

GDI Technique primarily improves the power consumption, speed and the area of the Carry Select adder [10] when compared to the existing Techniques.

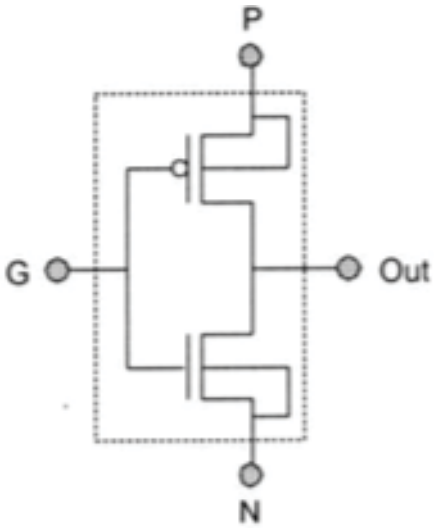

Fig. 1. GDI basic cell

The basic GDI cell consists of two transistors As shown in Fig 1. the GDI basic cell has two transistors and has 3 inputs: G, P and N. One can use this inputs to easily implement any expression with minimum number of Transistors.

II. 8 Bit CSA using GDI Technique

The conventional Carry select adder uses a 28 transistors full adder as basic adder cell and 12 Transistors MUX whereas [2] [11], the GDI technique uses a 8 Transistors full adder consisting of two 3 Transistors EX-OR gate and one 2 Transistors MUX as shown in Fig.2, Fig.4, Fig.5, Fig.6 and Fig.7

III. 8 Bit CSA using GDI and MTCMOS DLATCH

A. MTCMOS D-Latch

A traditional D-Latch based on Nand gate is shown in Fig.8. MTCMOS D-Latch is designed as shown in Fig.9, When Enable signal is low, the output signal follows the input signal. When Enable signal is high, the previous value of the output is held in the Latch and retained [2]. Internal circuit is in direct contact with VDD and grounding when Sleep Transistors are turned on; when they are off(stand-by mode) internal circuit draws power from virtual power supplies [2] [3].

B. CSA Using GDI and MTCMOS Logic

In this proposed structure, a new design technique which consists of combining both GDI and MTCMOS Technique to achieve high speed operation and Low power consumption fora CSLA adder circuit is studied. [2] [9]. The circuit diagram is shown in Fig.10

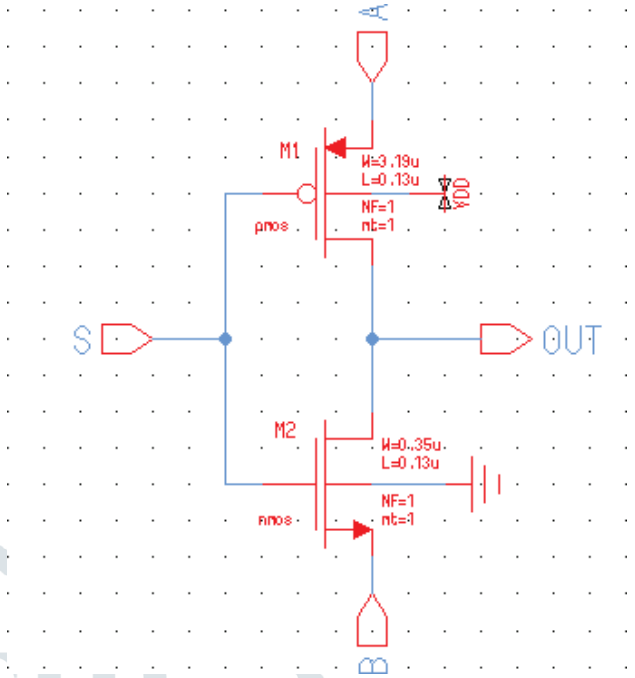

Fig. 2. 2 to 1 MUX using GDI

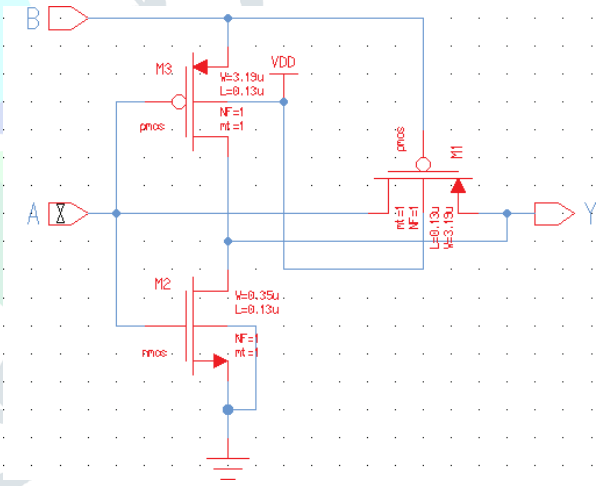

Fig. 3. 3 Transistor EX-OR Gate

IV. Simulation Results and Comparison

The functional response of the Carry select adder is studied by analyzing the simulation results obtained using Tanner Mentor Graphics 250 nm CMOS Technology and different performance parameters are measured such as Area, Power consumption, etc. The supply voltage used is 2.5 V. Here, 2 input bit streams A= 00001000 and B= 000000000 AND cin=0 are considered to study the fuctionality of the proposed CSA. The input A and B are shown in Fig.11 and Fig.12.

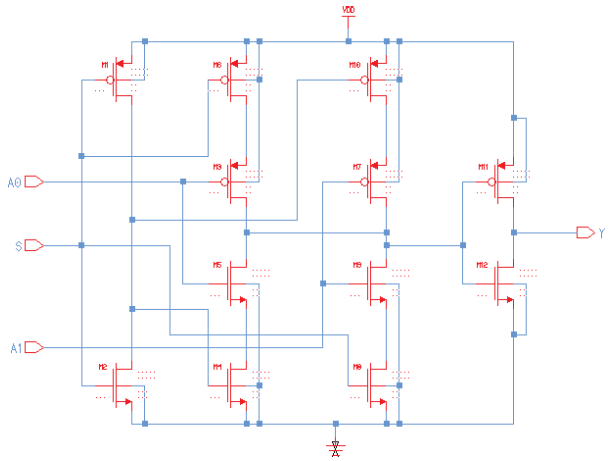

Fig. 4. Traditional mux

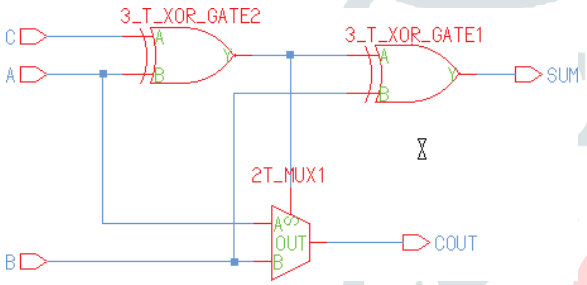

Fig. 5. 1 Bit Full Adder using GDI

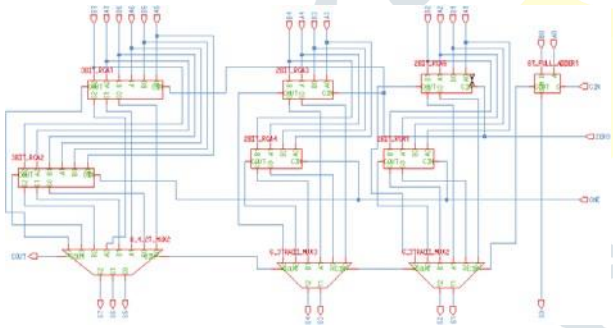

Fig. 6. 8 Bit CSA using GDI

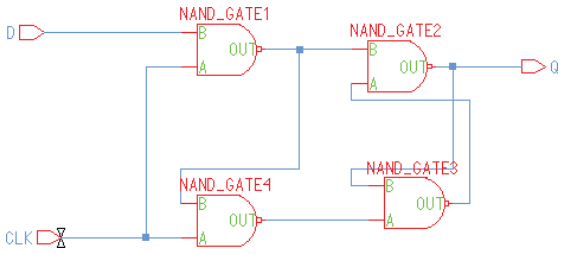

Fig. 7. Traditional DLatch

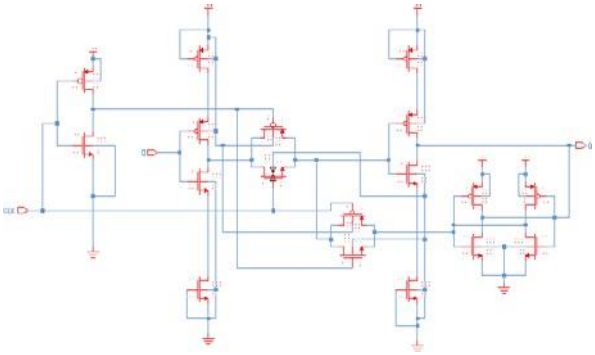

Fig. 8. MTCMOS Dlatch

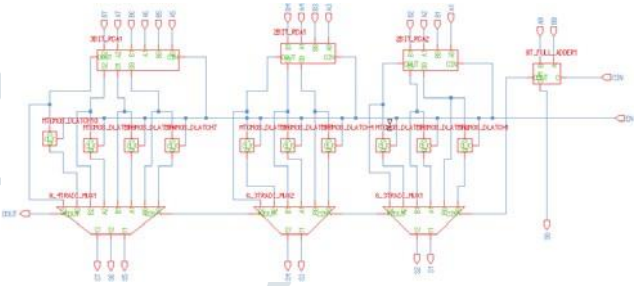

Fig. 9. 8 Bit CSA usinG both GDI and MTCMOS logic

1) 8 Bit CSA using GDI Technique: Using the GDI Technique, the output bitstream sum= 00111111 as it should be. The correspoding waveforms are shown in Fig.13.

2) 8 Bit CSA using GDI and MTCMOS Dlatch: Using both Gdi and MTCOS Technique, we get the same sum result and the waveforms are shown in Fig.14

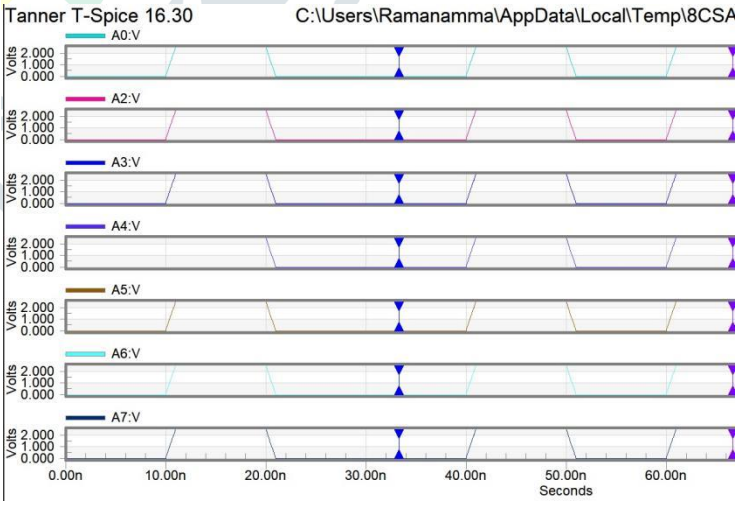

Fig. 10. A inputs

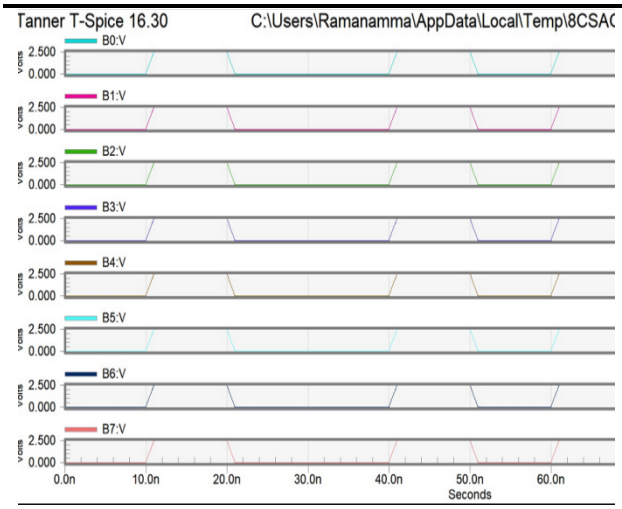

Fig. 11. input B

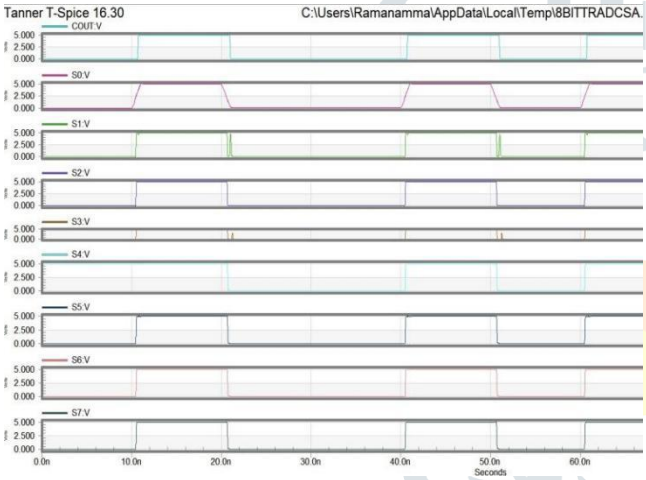

Fig. 12. Output Sum

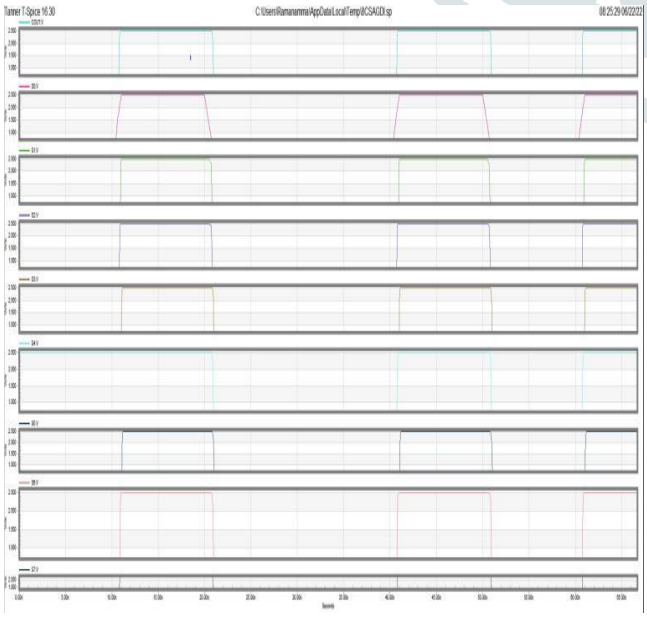

Fig. 13. Output Sum

Comparison and Discussion

The Performance comparison of different Techniques used to design the Carry select adder is shown in Table 1 and in a chart in Fig.15. The GDI Technique achieves the lowest power consumption and has less Transistor count when compared to other Techniques and the combination of both GDI na MTCMOS achieves the highest speed but when the Power- Delay-Product (PDP)is calculated, the last Technique offers better perfomance with a PDP of 0.76824 whereas GDI has a PDP of 1.433.

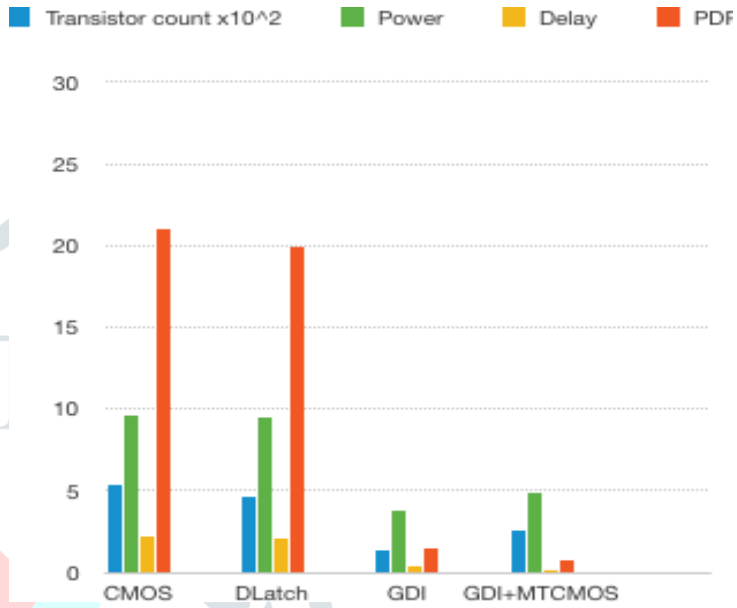

Fig 14:8 Bit CSA Graphical Analysis

Fig. 14. 8 Bit CSA Graphic Analysis

TABLE I
COMPARISON AND DISCUSSION

Bit Size	Type of adder	Transistor count	Average Power consumed(mW)
8	Conventional CSA	520	0.56
8	CSA Using DLatch	484	0.3
8	CSA using GDI MTCMOS	364	1.1
8	CSA Using GDI	240	0.16
8	CSA Using MTCMOS	504	1.51

CONCLUSION

In the existing work, the Carry select adder circuit was modified and the improvement in power and transistor count was 0.5% and 15% respectively. In this paper, 2 techniques are modified. The first is GDI Technique where the CSA is designed and as result the Power consumption and Trasistor count are improved respectively by 75% and 60%. To improve further these design parameters, another Technique combining both GDI and MTCMOS was modified. The design of CSA using this Technique achieved a tremendous improved in power and Transistor count of 75% and 58.85% respectively as compared to the conventional CSA. Eventhough, very good results are obtained in term of Power, and Area; research need to be done for improving the signal degradation observed.

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