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A Low Power 6T SRAM usingSleep Power Reduction Technique

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***Abstract*—**

Static Random Access memory (SRAM) is a memory component. Due to its unique capability to retain data, there is a large demand for SRAM in SOC with large usage. This memory component became a research subject to meet future demands With increase in SRAM density, significance of the power leakage has increased in chip design. In recent years, power reduction in SRAM is undergoing tremendous advancement Mary techniques have been devised to achieve active and standby reduction in both dynamic and static power. Performance in terms of speed and power dissipation is the major concern in today's memory technology. Keeping this in view, this paper emphasizes a low power SRAM using hybrid sleep transistor technique which is compared in terms of delay: power dissipation and power delay product(PDP) to that of conventional SRAM. This technique reduces both delay and power consumption of SRAM. Whole work is done on the TANNER MENTORGRAPHICS 250nm technology parameter & stimulated are IV supply voltage.

***Index Terms*—SRAM, System on chip(Soc), MTCMOS, Scaling.**

I. INTRODUCTION

Recently, there is an increase in demand for battery operated high speed portable devices like notebook, laptops, personal digital assistants, mobile phones, etc. These devices require a primary memory that responds faster. Refreshing is not needed always. Power dissipation is the major issue in high speed SRAM. It reduces battery backup life of portable devices significantly. So, SRAM design which has low power dissipation is recommended. To maintain the power consumption within limit, supply voltage is scaled but scaling of supply voltage is limited by high performance requirement. So, not only the supply voltage scaling may be sufficient to maintain power consumption within limits that is required for power sensitive applications. Circuit techniques and system level techniques are also required along with supply voltage scaling for low power designs[1].

From the following graph, the quantity of power leakage increases when technology scales down[2] Mobile multimedia applications have two operation modes, active mode and standby mode. For example, a mobile has low activity factor where the idle time is larger than active time. In ideal time, these devices are affected by the power leakage which reduces the battery service time.

To address this leakage, different optimization techniques have been developed. There are four main sources of leakage current in a CMOS transistor [10].

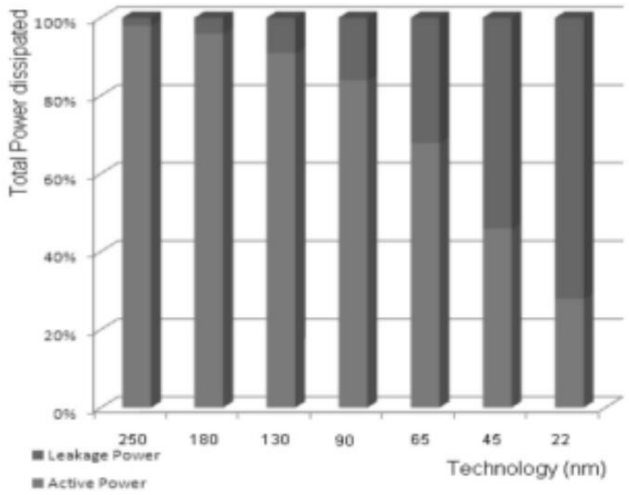

Fig 1: Power dissipation in various technologies

The sub threshold leakage current is a result of low threshold voltage, whereas the gate leakage current is a result of ultra thin oxide and tunneling leakage is due to heavily doped profile. Increasing the threshold voltage is one of the ways to reduce leakage current. Now the factors that impact tunneling current heavily are, gate to source and gate to drain overlap currents, direct tunneling current which is also known as gate to channel current and gate to substrate current[7].

This paper is motivated towards developing a low power memory cell. In this paper a new low power technique based

on sleep transistor for SRAM cell is designed to reduce the power dissipation and experimental results shows the effect of voltage scaling for commercially available lónm CMOS technology.

The rest of the paper is organized as follows. Section II describes the conventional SRAM structure and its operation of read, write and hold. Section III describes the proposedcharacteristics of various existing logic styles are compared circuit. Section IV shows the simulation results. Finallyconclusions are made in section V.

II.CONVENTIONAL 6T SRAM CELL

The conventional 6T memory cell consists of 4 NMOS and 2 PMOS transistors which can be visualized as of two CMOS inverters cross coupled with two pass transistors connected to a complementary bit lines as shown in figure below. The leakage power consumption of the memory cell will be limited to relatively small leakage currents of both CMOS inverters. The only drawback of using the cross coupled inverters, is slightly larger area than resistive load and depletion-load NMOS SRAM Cell[6]. There are 3 states in SRAM cell.

• Write

• Read

• Hold

2.1 HOLD STATE:

In hold state, circuit will be idle & the word line is not asserted. The transistors Ml & M which connects to bitlines are turned off. During hold state, the cell cannot be accessed. Thus, cross coupled inverters continues to feedback each other as long as they are connected to supply voltage. The data will be held in the latch during hold state.

2.2 READ STATE:

Read operation starts with pre-charging Bit and Bit bar to high. Within the memory cell M3 and M6 are ON. Asserting the word line, turns ON the MI and M. The values of Q and Q' are transferred to bit-Lines. No current flows through M, thus M and M6 pull Bit bar up to VW, i.e., Bit bar="1" and Bit line discharges through MI and M3.

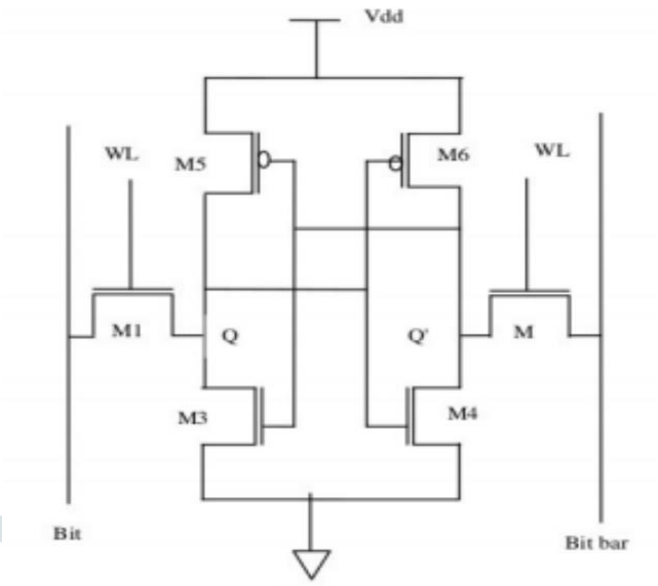

Fig 2: Conventional 6T SRAM cell

2.3 WRITE STATE

The write operation begins by forcing a differential voltage (VDD and 0) at the bitline pairs (BLB and BL). This differential voltage corresponds to the data to be written at the storage nodes (O and O') and it is controlled by the write drivers. The WL is then activated to store the information from the bit-line pairs to corresponding storage nodes. Assume, the nodes Q and Q' initially store values l' and '0' respectively. When the WL is asserted the access transistor (MI) connected to BL (at '0') is turned on. a current flows from V DD to BL through M3 and Ml. This current flow lowers the potential at node 0. The potential at the node O has to go below the trip point of the inverter (M6 & M4) for a successful write operation and this depends on the ratio of pull-up transistor (M3) between the access transistor (MI). This ratio is referred to as the pull-up - ratio.

From the working of 6T SRAM cell explained above, it is observed that power dissipation in SRAM can be divided into two parts. The first one is dynamic power, due to reading and writing of data, switching activity of transistors and charging and discharging of bit and bit-bar lines [3]. Second is when the cells are in steady state, because of leakage current of the MOS transistors.

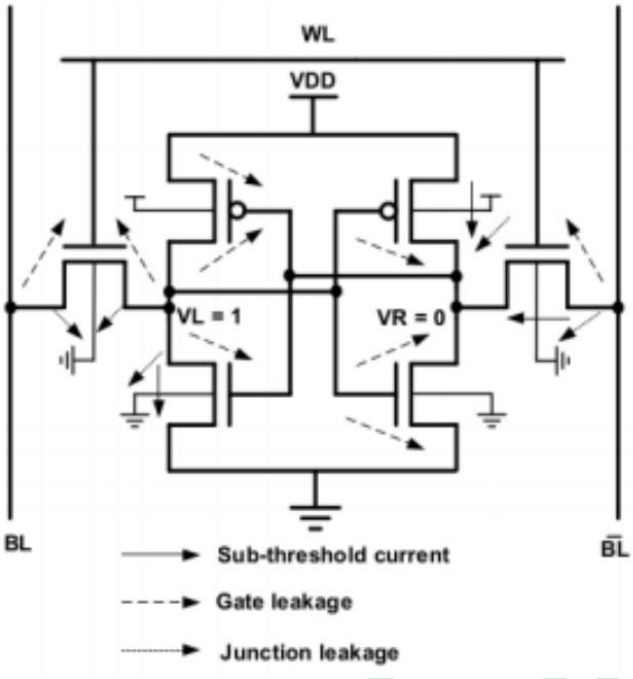

Fig 3: Leakage currents in 6T SRAM

III. SLEEP TRANSISTOR TECHNIQUE

Among the low power design techniques of 6T SRAM, sleep transistor design technique dissipates less power [9]. The sleep transistor technique uses two sleep transistors at different positions. One Pmos and one Nmos transistors are connected in series with the cell. Pmos is connected between Vd and pull-up transistors. Nmos is connected between pull-down transistors. These sleep transistors forms virtual V, and virtual ground. When the circuit is on; sleep transistor gets activate so that the working of the circuit remains retained whereas in off state; the sleep transistor gets off so that source node of the gate gets float because of this leakage path gets cut off. There are two main reasons for power reduction one is stacking of transistors and other is low sub-threshold leakage current of high V.

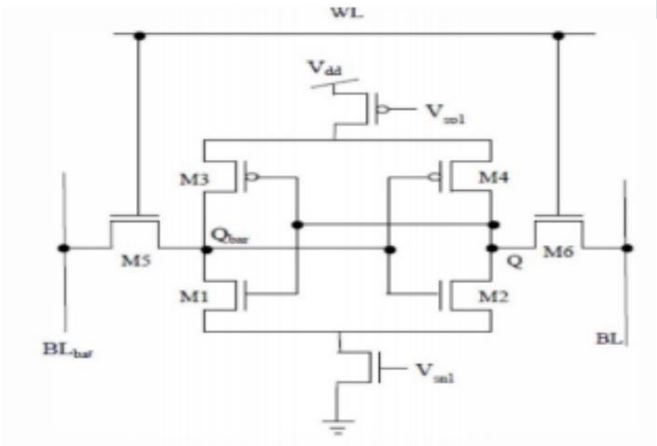

Fig 4: SRAM using Sleep Transistor Technique

VI. MODIFIED DESIGN

MTCMOS technology has been adopted to achieve balanced design parameter such as cell stability, performance, write margin. SRAM power consumption is determined by supply voltage along with device selection [4]. Hybrid MTCMOS is similar to MTCMOS. In this the PMOS sleep transistor is stacked and low threshold voltage is used. In the proposed design, the PMOS sleep transistor is turned ON and NMOS sleep transistor is turned OFF. Use of both negative & positive voltage reduces the power dissipation exponentially [5].

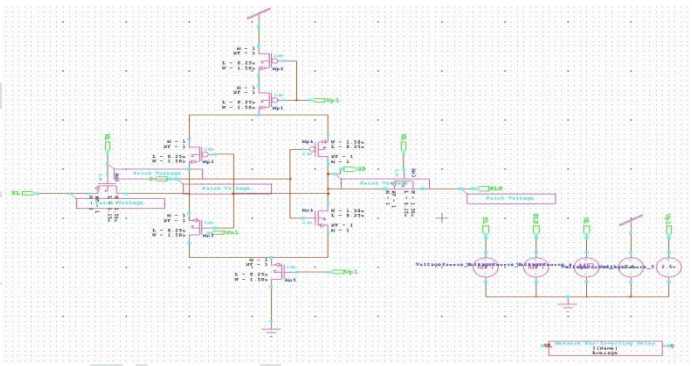

Fig 5: Modified design

Here the most important point is the transistor sizing. The sizing of transistor directly affect the read stability and write ability of the SRAM cell[6]. For better stability (width of pull-down transistors)far greater than (width of access transistors) greater than (width of pull-up transistors) [8]. The width of sleep transistors should be as of pull-down transistors in this design. From fig 3 it is clear that PMOS sleep transistor width should be halved of that NMOS sleep transistor width. Here Vpl is common for both PMOS and NMOS sleep transistors.

V. SIMULATION & RESULTS

The comparison has been carried out between conventional 6T SRAM and proposed SRAM in terms of power and delay. All the simulations in this work are done using 250nm technology in TANNER Mentor Graphics tool. The output wave form is as shown in figure for the proposed design.

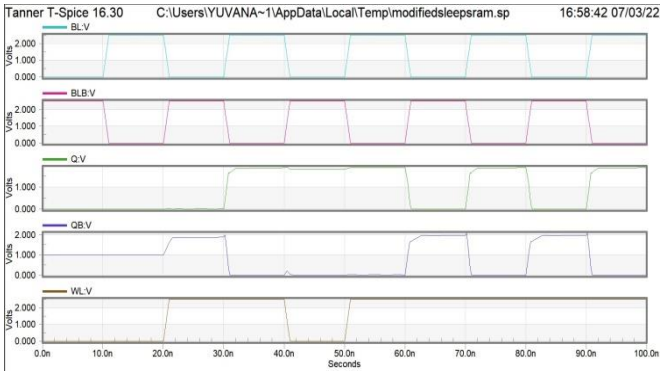

Fig 6: Simulation Waveform of modified design

Table 1: Avg Power Consumption and Delay report of different SRAMs.

Vdd=Vgs=2.5v	Avg power consumption	Delay (in Ns)
SRAM 6T CONVENTIONAL	1.958×10^{-4}	15.1319
SRAM FORCED STACK	1.27×10^{-5}	15.0851
SRAM SLEEP	7.598×10^{-8}	15.0344
DTMOS SRAM 6T	2.287×10^{-4}	15.1413
DTMOS FORCED STACK	1.085×10^{-5}	15.0303
DTMOS SLEEP	2.7157×10^{-11}	15.1505
VTMOS SRAM 6T	8.65×10^{-5}	19.2338
VTMOS FORCED STACK	6.7131×10^{-6}	14.7376
VTMOS SRAM SLEEP	4.563×10^{-13}	15.0822
MODIFIED SLEEEP	4.875×10^{-8}	15.0345

VI. CONCLUSION

In this paper, we have implemented a hybrid and VTMOS sleep technique for SRAM for low power applications. Our design drastically reduces power consumption and power dissipation and power delay product. It is found that proposed design consumes 60%less power than conventional SRAM whereas 2% less in terms of delay. Sleep based SRAM (VTMOS,DTMOS,MODIFIED) gives less power consumption than remaining SRAMs.

ACKNOWLEDGMENT

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